SONY

CXG1130AER

Triple Low Noise Amplifier/Dual Mixer

Description

The CXG1130AER is a triple low noise amplifier/dual mixer. This IC is designed using the Sony's GaAs J-FET process.

Features

- Single 3V power supply operation
- 2-pin control by the on-chip logic circuit
- High gain: Gp = 16.5dB (LNA typ.)
  Gc = 10dB (MIX typ.)
- Low noise figure: NF = 1.5 to 1.6dB (LNA typ.)
  NF = 4.5dB (MIX typ.)
- Low LO input power operation
- 24-pin VQFN small package

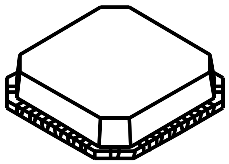
Applications

800MHz/1.5GHz Japan digital cellular phones (PDC)

Structure

GaAs J-FET MMIC

24 pin VQFN (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	4.5	V
• Input power	P_{IN}	+13	dBm
• Current consumption	I_{DD}	15	mA
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

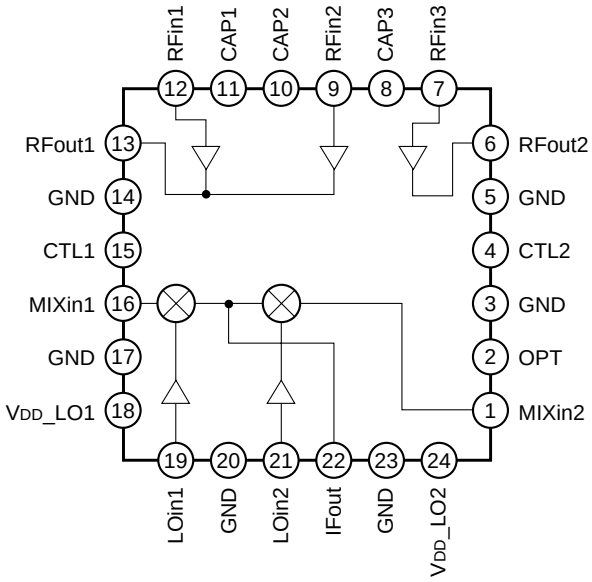
Recommended Operating Conditions

• Supply voltage	V_{DD}	2.7 to 3.3	V
• Control voltage	V_{CTL} (H)	2.4 to 3.3	V
	V_{CTL} (L)	0 to 0.3	V

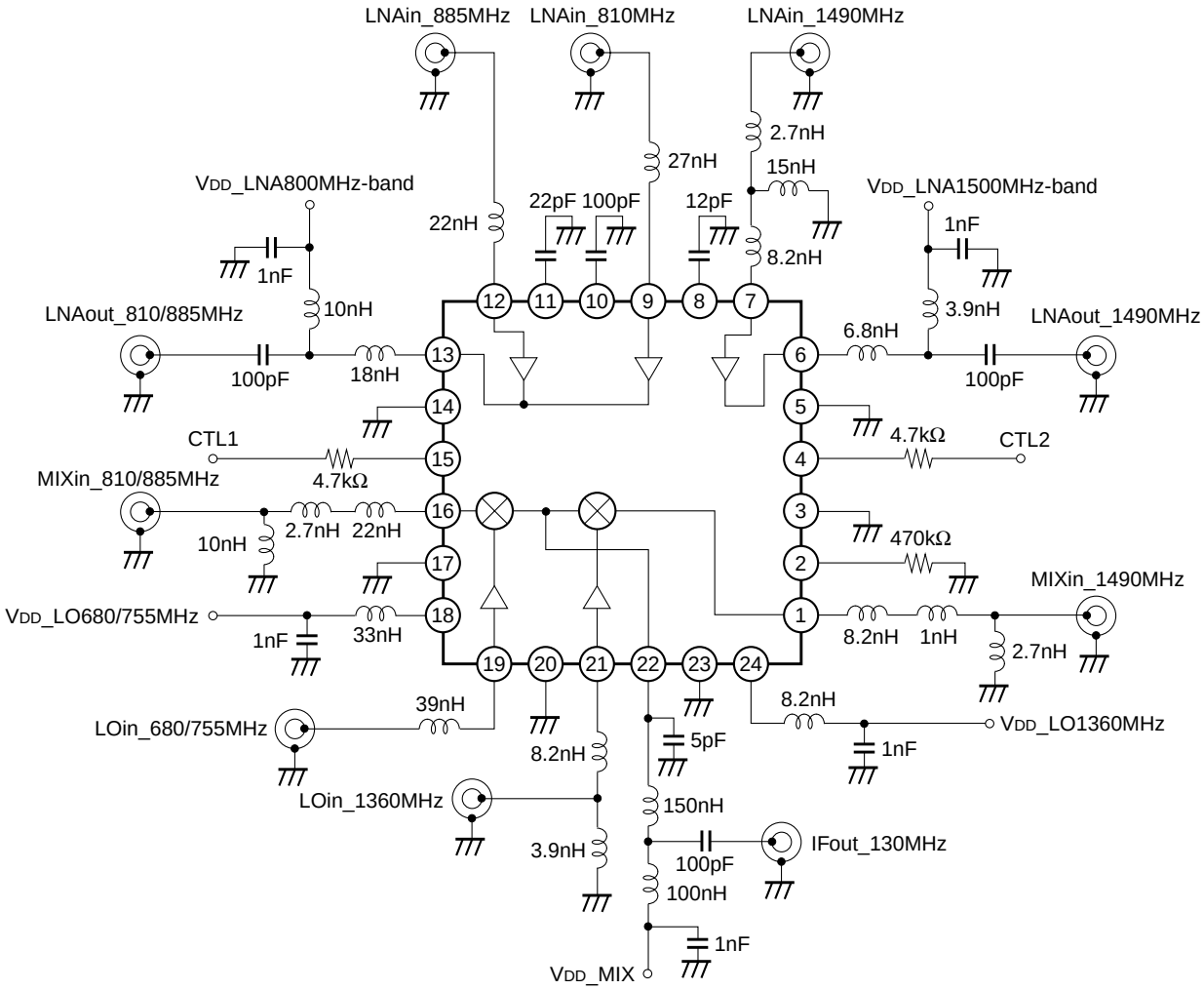
GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E01827-PS

Block Diagram and Pin Configuration



Recommended Evaluation Circuit



Electrical Characteristics

The normalized values are those when the Sony's recommended evaluation board is used.

800MHz Band Low Noise Amplifier

Conditions: Unless otherwise specified, V_{DD} = 3.0V, V_{CTL} (H) = 3.0V, V_{CTL} (L) = 0V, $f_{RF}1$ = 885MHz, $f_{RF}2$ = 810MHz

(Ta = 25°C)

Item	Symbol	Path	Frequency	$V_{CTL}1$	$V_{CTL}2$	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD}	—	—	H	L	—	2.0	2.65	mA	When no signal
			—	L	L	—	2.0	2.65		
Control current	$I_{CTL}1$	—	—	H	L	—	60	90	µA	
			—	L	L	–5	0	5		
Power gain	Gp	$RF_{IN}1 \rightarrow RF_{OUT}1$	$f_{RF}1$	H	L	14.5	16.5	18.5	dB	When a small signal
				L	L	—	–20	–15		
		$RF_{IN}2 \rightarrow RF_{OUT}1$	$f_{RF}2$	H	L	—	–25	–20		
				L	L	14.5	16.5	18.5		
Noise figure	NF	$RF_{IN}1 \rightarrow RF_{OUT}1$	$f_{RF}1$	H	L	—	1.3	2.0	dB	
		$RF_{IN}2 \rightarrow RF_{OUT}1$	$f_{RF}2$	L	L	—	1.5	2.0		
Input IP3	IIP3	$RF_{IN}1 \rightarrow RF_{OUT}1$	$f_{RF}1$	H	L	–10	–6.5	—	dBm	*1
		$RF_{IN}2 \rightarrow RF_{OUT}1$	$f_{RF}2$	L	L	–11	–8	—		
Isolation	I_{SO}	$RF_{OUT}1 \rightarrow RF_{IN}1$	$f_{RF}1$	H	L	22	26	—	dB	When a small signal
		$RF_{OUT}1 \rightarrow RF_{IN}2$	$f_{RF}2$	L	L	18	22	—		

*1 Conversion from the IM3 suppression ratio for two-wave input: f_{RF}offset = 100kHz, P_{RF} = –30dBm.

1.5GHz Band Low Noise Amplifier

Conditions: Unless otherwise specified, V_{DD} = 3.0V, V_{CTL} (H) = 3.0V, V_{CTL} (L) = 0V, $f_{RF}3$ = 1490MHz

(Ta = 25°C)

Item	Symbol	Path	Frequency	$V_{CTL}1$	$V_{CTL}2$	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD}	—	—	—	H	—	2.9	3.7	mA	When no signal
Control current	$I_{CTL}2$	—	—	—	H	—	90	120	µA	
Power gain	Gp	$RF_{IN}3 \rightarrow RF_{OUT}2$	$f_{RF}3$	—	H	14	16	18	dB	When a small signal
Noise figure	NF	$RF_{IN}3 \rightarrow RF_{OUT}2$	$f_{RF}3$	—	H	—	1.6	2.1	dB	
Input IP3	IIP3	$RF_{IN}3 \rightarrow RF_{OUT}2$	$f_{RF}3$	—	H	–9	–6	—	dBm	*1
Isolation	I_{SO}	$RF_{OUT}2 \rightarrow RF_{IN}3$	$f_{RF}3$	—	H	20	23	—	dB	When a small signal

*1 Conversion from the IM3 suppression ratio for two-wave input: f_{RF}offset = 100kHz, P_{RF} = –30dBm.

800MHz Band Mixer

Conditions: Unless otherwise specified, V_{DD} = 3.0V, V_{CTL} (H) = 3.0V, V_{CTL} (L) = 0V,
$f_{RF}1$ = 885MHz, $f_{RF}2$ = 810MHz, $f_{LO} = f_{RF} - 130$MHz, P_{LO} = –15dBm
(Ta = 25°C)

Item	Symbol	RF frequency	$V_{CTL}1$	$V_{CTL}2$	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD}	—	—	L	—	5	6.5	mA	When no signal
Control current	$I_{CTL}2$	—	—	L	–5	0	5	µA	
Conversion gain	Gc	$f_{RF}1$	—	L	9	10	11.5	dB	When a small signal
		$f_{RF}2$	—	L	8.5	9.5	11		
Noise figure	NF	$f_{RF}1$	—	L	—	5	6.5	dB	
		$f_{RF}2$	—	L	—	4	5.5		
Input IP3	IIP3	$f_{RF}1$	—	L	–1	+2	—	dBm	*1
		$f_{RF}2$	—	L	–0.5	+2.5	—		
LO → RF leak	Plk	$f_{RF}1$	—	L	—	–21	–18	dBm	f_{LO} = 755MHz
		$f_{RF}2$	—	L	—	–24	–21		f_{LO} = 680MHz

*1 Conversion from the IM3 suppression ratio for two-wave input: f_{RF}offset = 100kHz, P_{RF} = –25dBm.

1.5GHz Band Mixer

Conditions: Unless otherwise specified, V_{DD} = 3.0V, V_{CTL} (H) = 3.0V, V_{CTL} (L) = 0V,
$f_{RF}3$ = 1490MHz, f_{LO} = 1360MHz, P_{LO} = –15dBm (Ta = 25°C)

Item	Symbol	RF frequency	$V_{CTL}1$	$V_{CTL}2$	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD}	—	—	H	—	5.5	7.5	mA	When no signal
Control current	$I_{CTL}2$	—	—	H	—	90	120	µA	
Conversion gain	Gc	$f_{RF}3$	—	H	9	10	11.5	dB	When a small signal
Noise figure	NF	$f_{RF}3$	—	H	—	4.5	6	dB	
Input IP3	IIP3	$f_{RF}3$	—	H	–1	+2	—	dBm	*1
LO → RF leak	Plk	$f_{RF}3$	—	H	—	–24	–21	dBm	f_{LO} = 1360MHz

*1 Conversion from the IM3 suppression ratio for two-wave input: f_{RF}offset = 100kHz, P_{RF} = –25dBm.

Operation Logic

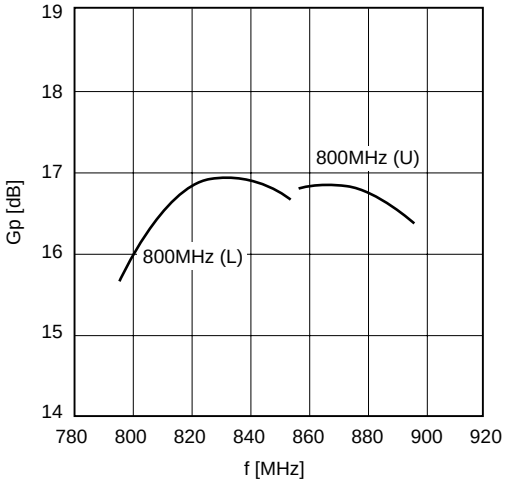
$V_{CTL}1$	$V_{CTL}2$	LNA1 (800MHz_U)	LNA2 (800MHz_L)	LNA3 (1.5GHz)	MIX1 (800MHz)	MIX2 (1.5GHz)
H	L	ON	OFF	OFF	ON	OFF
L	L	OFF	ON	OFF	ON	OFF
—	H	OFF	OFF	ON	OFF	ON

Example of Representative Characteristics

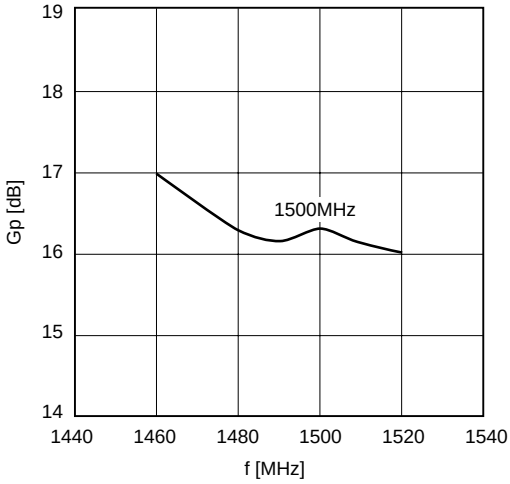
1. CXG1130AER frequency characteristics of main items in LNA block (25°C)

[Condition] V_{DD} = 3V, 800MHz_L (Pin 9 input → Pin 13 output): $V_{CTL}1$ = 0V, $V_{CTL}2$ = 0V,
800MHz_U (Pin 12 input → Pin 13 output): $V_{CTL}1$ = 3V, $V_{CTL}2$ = 0V,
1500MHz (Pin 7 input → Pin 6 output): $V_{CTL}2$ = 3V
Gp and NF are those when a small signal is input. The input IP3 is converted from the IM3 suppression ratio for two-wave input: f_{RF}offset = 100kHz, P_{RF} = –30dBm.

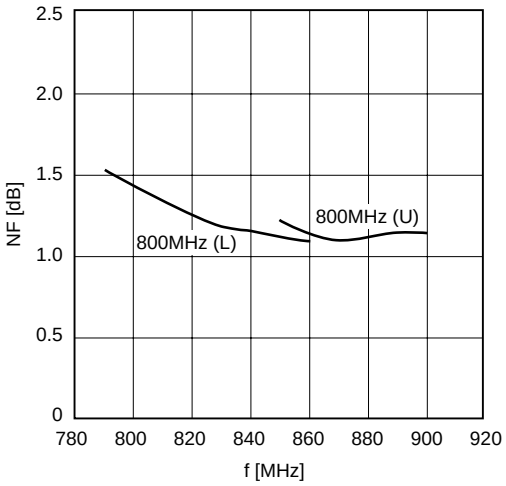
Power gain Gp



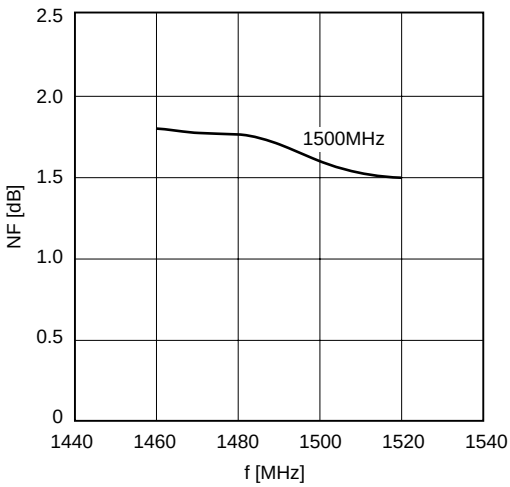
Power gain Gp



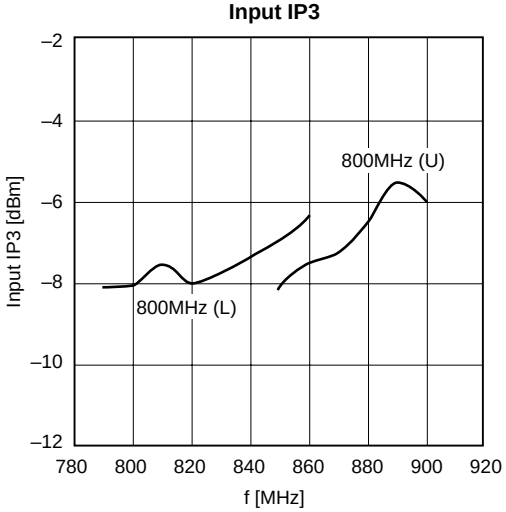
Noise figure NF



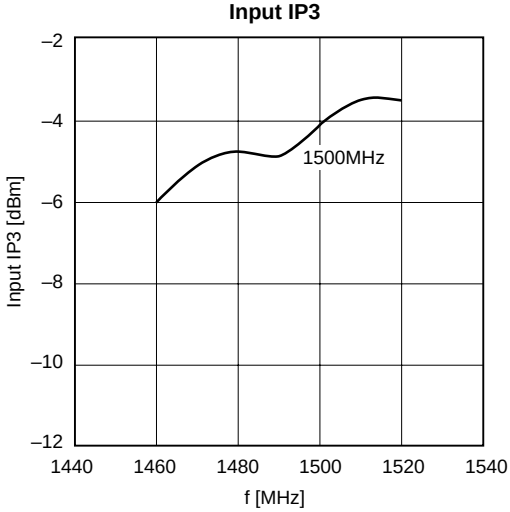
Noise figure NF



Input IP3



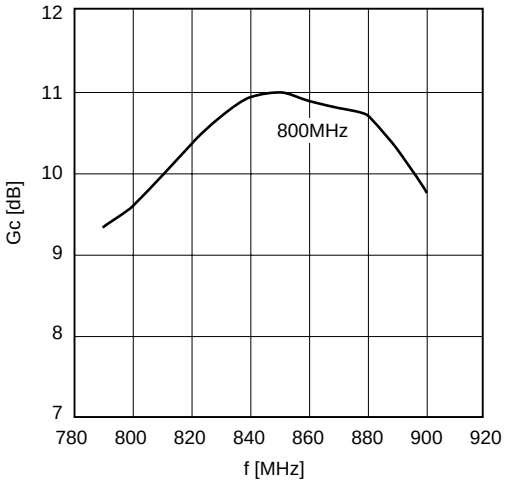
Input IP3



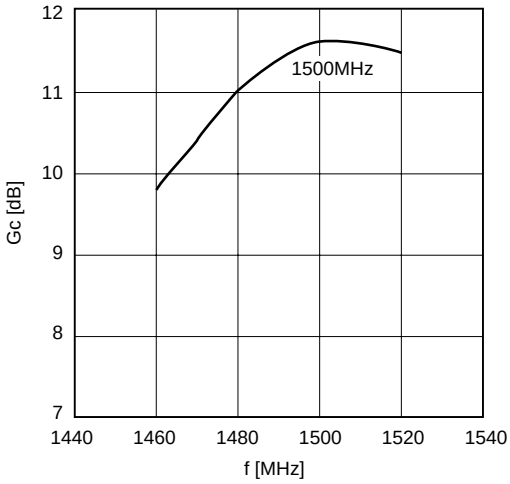
2. CXG1130AER frequency characteristics of main items in MIX block (25°C)

[Condition] V_{DD} = 3V, $f_{LO} = f_{RF}$ – 130MHz, P_{LO} = –15dBm, 800MHz: $V_{CTL}2$ = 0V, 1500MHz: $V_{CTL}2$ = 3V
Gc and NF are those when a small signal is input. The input IP3 is converted from the IM3 suppression ratio for two-wave input: f_{RF}offset = 100kHz, P_{RF} = –25dBm.

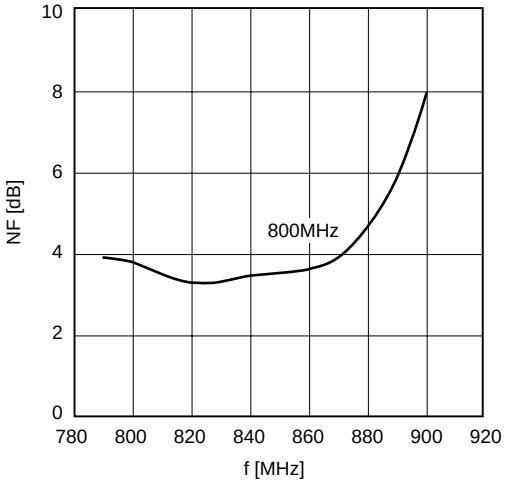
Conversion gain Gc



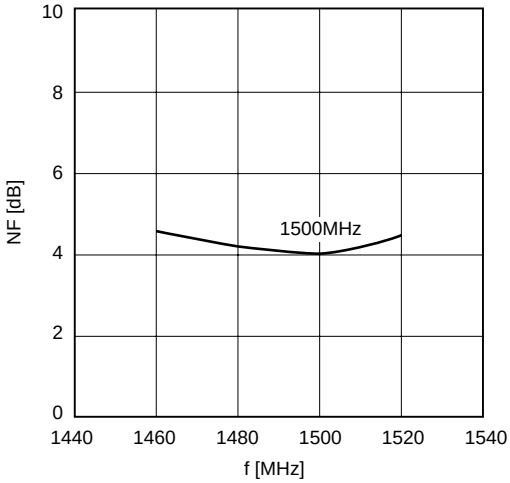
Conversion gain Gc



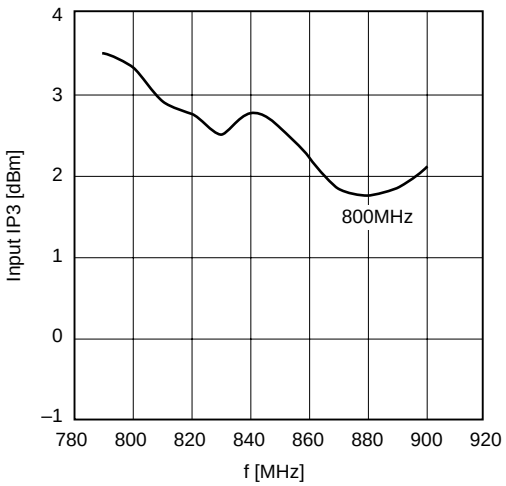
Noise figure NF



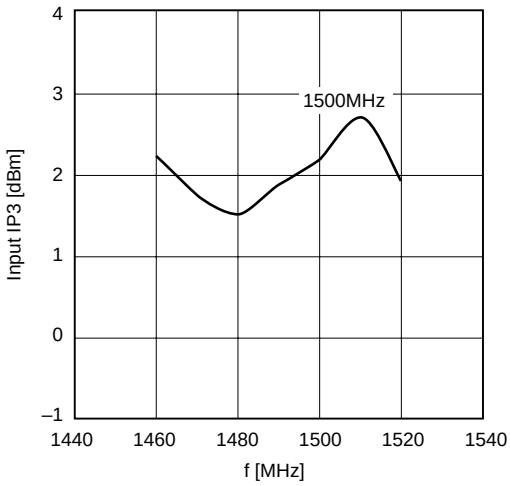
Noise figure NF



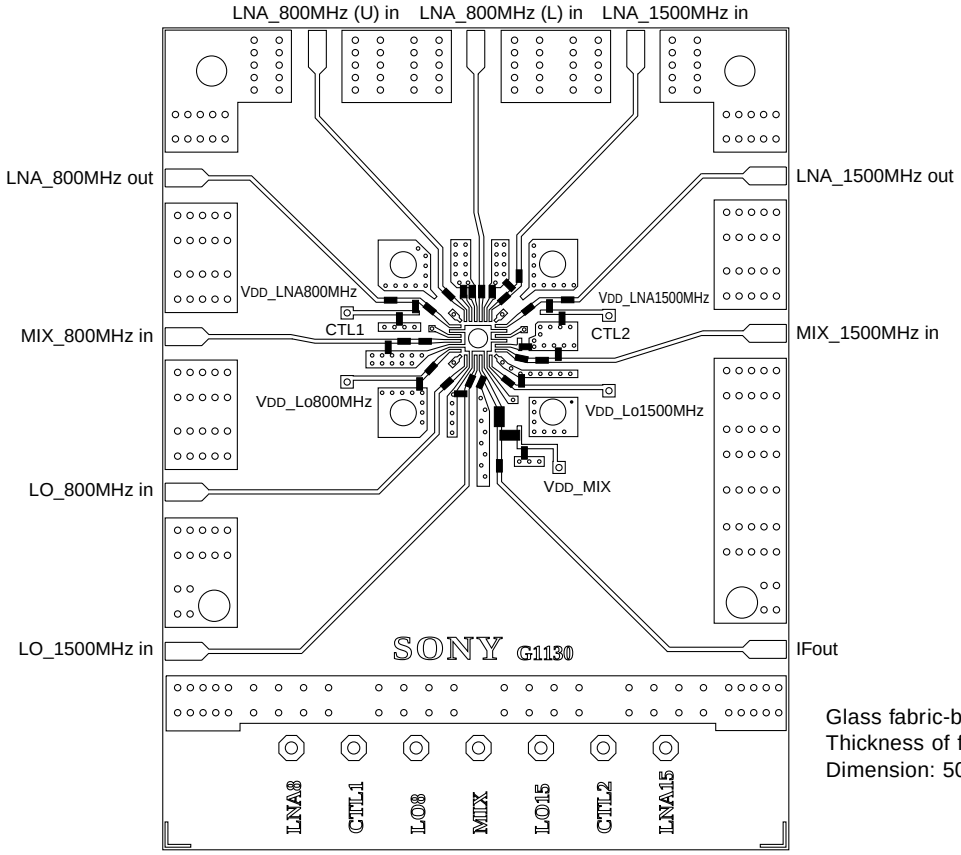
Input IP3



Input IP3

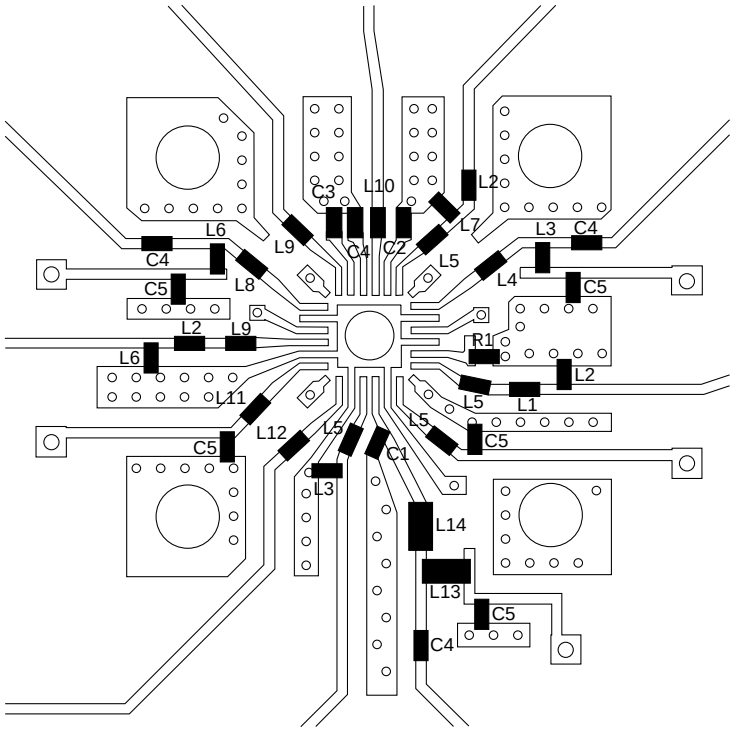


Recommended Evaluation Board



Glass fabric-base 4-layer epoxy board
Thickness of film between layers 1 and 2: 0.2mm
Dimension: 50mm × 66mm

Enlarged Diagram of External Circuit Block

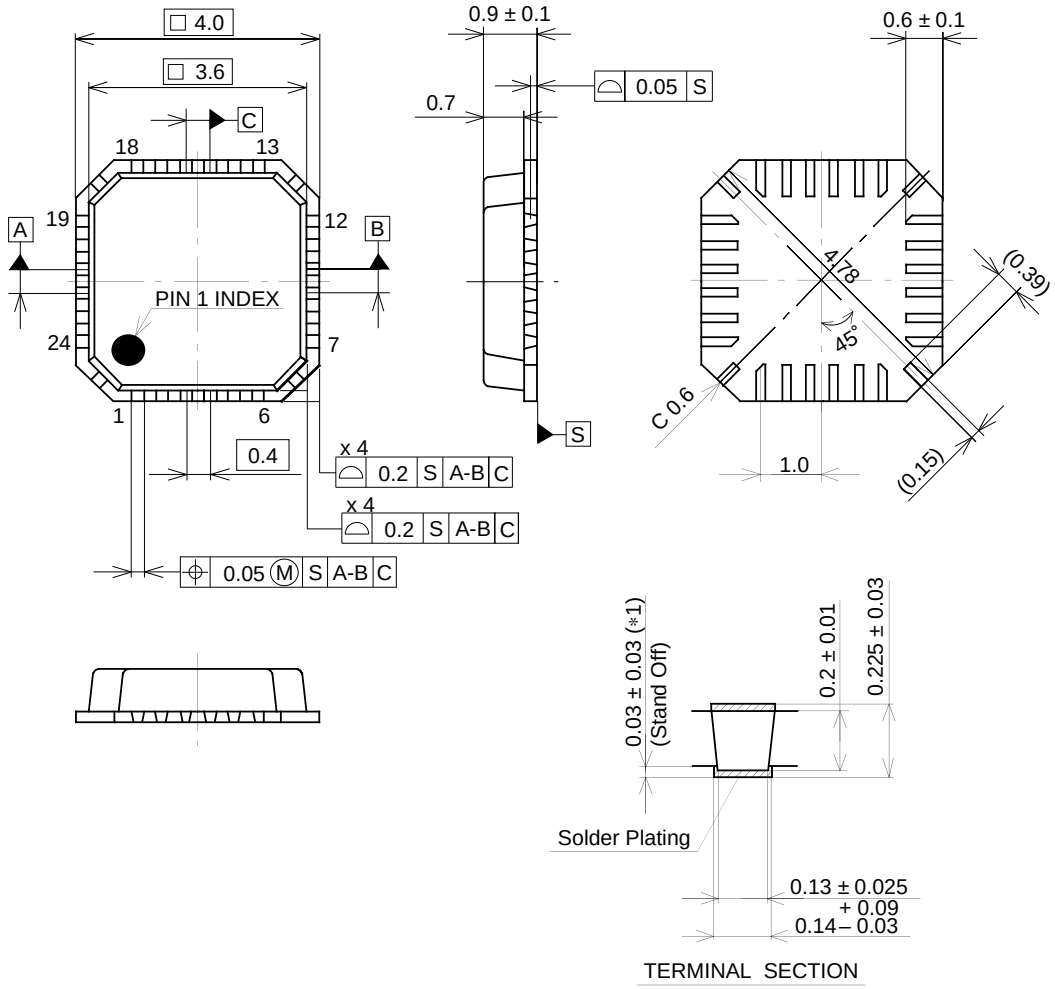


L1 = 1nH	C1 = 5pF
L2 = 2.7nH	C2 = 12pF
L3 = 3.9nH	C3 = 22pF
L4 = 6.8nH	C4 = 100pF
L5 = 8.2nH	C5 = 1nF
L6 = 10nH	
L7 = 15nH	R1 = 470Ω
L8 = 18nH	
L9 = 22nH	
L10 = 27nH	
L11 = 33nH	
L12 = 39nH	
L13 = 100nH	
L14 = 150nH	

Series resistors of 4.7kΩ to CTL1 and CTL2 are attached on the solder side of the board.

Package Outline Unit: mm

24PIN VQFN(PLASTIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g

SONY CODE	VQFN-24P-03
EIAJ CODE	————
JEDEC CODE	————

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER PLATING	Sn-Bi Bi:1-4wt%
LEAD TREATMENT THICKNESS	5-18µm