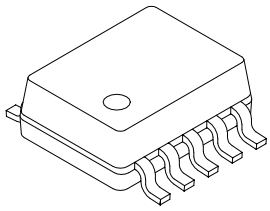
SONY

CXG1104TN

High Power SPDT Switch with Logic Control

10 pin TSSOP (Plastic)



Description

The CXG1104TN is a high power antenna switch MMIC for use in cellular handsets, for example, CDMA.

The CXG1104TN has on-chip logic, which enables the switch circuit to operate by 1 CMOS control line.

The Sony JFET process is used for low insertion loss and on-chip logic circuit.

Features

- Low insertion loss: 0.3dB @900MHz, 0.4dB @1.9GHz
- High linearity: IIP3 (Typ.) = 70dBm
- 1 CMOS compatible control line
- Small package size: 10-pin TSSOP

Applications

Cellular handsets, for example, narrow band CDMA and wide band CDMA

Structure

GaAs J-FET MMIC

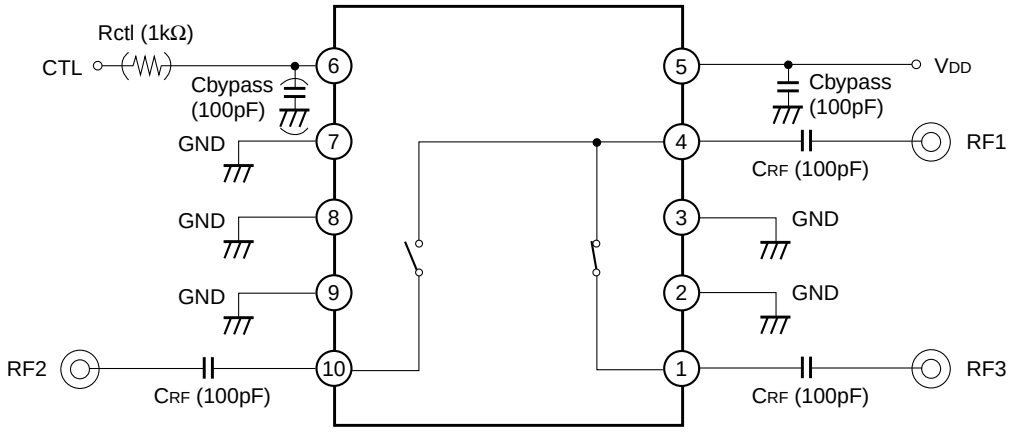
Absolute Maximum Ratings (Ta = 25°C)

• Bias voltage	V_{DD}	7	V
• Control voltage	Vctl	5	V
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

GaAs MMICs are ESD sensitive devices. Special handling precautions are required.
The actual ESD test data will be available later.

E00X23A2Z-PS

Block Diagram and Recommended Circuit



When using this IC, the following external components should be used:

Rctl: This resistor is used to improve ESD performance. 1kΩ is recommended.

C_{RF}: This capacitor is used for RF decoupling and must be used for all applications. 100pF is recommended.

Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Truth Table

On Pass	CTL
RF1 – RF2	L
RF1 – RF3	H

DC Bias Condition

(Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	3.0	3.6	V
Vctl (L)	0	—	0.8	V
V_{DD}	2.6	3.0	4.5	V

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	900MHz		0.30	0.55	dB
		1.9GHz		0.40	0.65	dB
Isolation	ISO.	900MHz	20	23		dB
		1.9GHz	14	16.5		dB
VSWR	VSWR	900MHz, 1.9GHz		1.2	1.4	—
Harmonics	2fo	*1	–60	–75		dBc
	3fo	*1	–60	–75		dBc
1dB compression input power	P1dB	V_{DD} = 3.0V, 0/3V control	32	35		dBm
Input IP3	IIP3	*2	60	70		dBm
Switching speed	TSW			2	5	µs
Control current	Ictl	Vctl (High) = 3V		40	80	µA
Bias current	I_{DD}	V_{DD} = 3V		100	200	µA

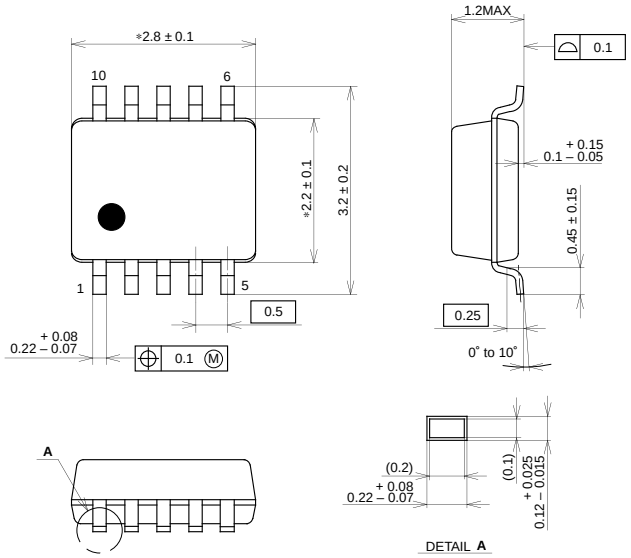
*1 Pin = 29dBm, 900MHz, V_{DD} = 3.0V, 0/3V control

*2 Pin = 25dBm (900MHz) + 25dBm (901MHz), V_{DD} = 3.0V, 0/3V control

Package Outline

Unit: mm

10PIN TSSOP (PLASTIC)



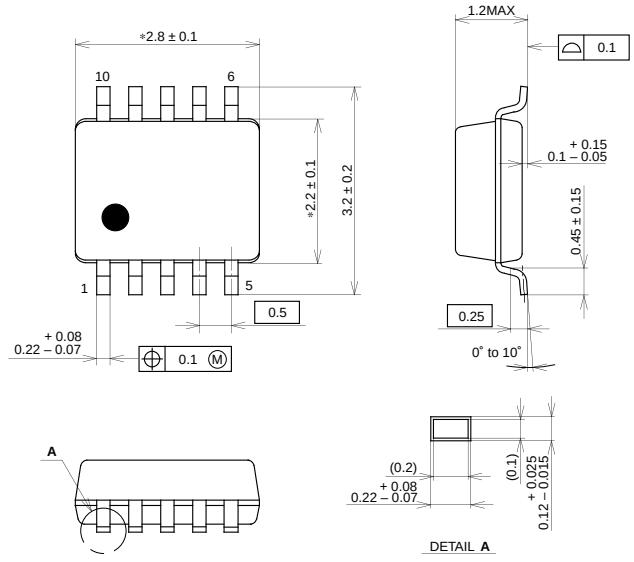
NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	TSSOP-10P-L01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02g

10PIN TSSOP (PLASTIC)



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LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm