Sitronix

ST8009

Dot Matrix Lcd
96 Output LCD Common/Segment driver IC

DESCRIPTION

The ST8009 is a 96-output segment/common driver IC suitable for driving small/medium scale dot matrix LCD panels, and is used in PDA or electronic dictionary . The ST8009 is good as a segment driver or a common driver or a common/segment driver, and it can create low power consumption, high-resolution LCD. The ST8009 have eight modes can selected to set common and segment numbers by select pin. The ST8009 also have analog DC/DC converter to used.

FEATURES

- Number of LCD drive outputs: 96
- Supply voltage for LCD drive: Max +16V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption and low output impedance
- Display duty selectable by internal select register

SEL_2,SEL_1,SEL_0	DUTY	BIAS
0 0 0	---	Segment mode
0 0 1	1/16	1/5 or 1/4
0 1 0	1/32	1/6 or 1/5
0 1 1	1/48	1/7 or 1/5
1 0 0	1/64	1/9 or 1/7
1 0 1	1/80	1/9 or 1/7
1 1 0	1/96	1/10 or 1/8
1 1 1	1/96	1/10 or 1/8

- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratio of 2X/3X/4X/5X/6X)
  Regulator circuit
  Follower circuit
- Abundant command functions
  LCD bias set, electronic volume, V_{SS} voltage regulation internal resistor ratio and booster frequency.
  All Functions have initial value, user can set by programmable.
- Package: 124-pin COB.

(Segment mode)

- Shift clock frequency
  - 20 MHz (MAX.): V_{DD} = +5.0 ± 0.5 V
  - 15 MHz (MAX.): V_{DD} = +3.0 to + 4.5 V
  - 12 MHz (MAX.): V_{DD} = +2.5 to + 3.0 V
- Adopts a data bus system
- 4-bit parallel / serial input modes are selectable by programmable.
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 16、32、48 、64、 80、96 bits of input data
- Line latch circuits are reset when XDISPOFF active

(Common mode)

- Shift clock frequency: 4 MHz (MAX.)
- Built-in X-bit shift register
- Available in a single mode
- Y_1->Y_X Single mode

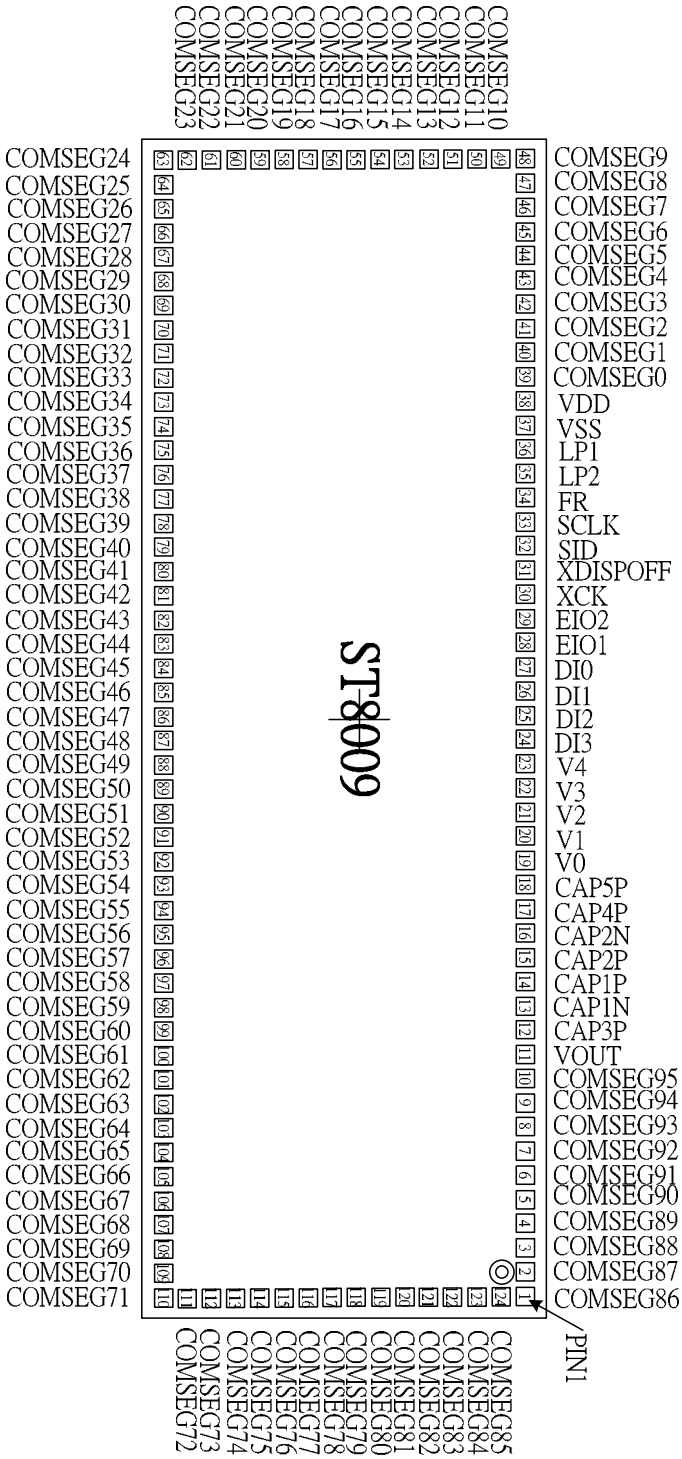
  Y_X->Y_1 Single mode

  PS:X=16、32、48、64、64、80、96

  The above 4 shift directions are register selectable
- Shift register circuits are reset when XDISPOFF active

PAD ARRANGEMENT

Chip size: 5070.0(um) x1790.0 (um)
Pad size：80 (um) x80 (um)
Pad pin pitch: 100 (um) ~ 140 (um)
Origin : chip center (0,0)
Chip Thickness：19 mil



Substrate Connect to Vss.

Pad Configuration

Pad No.	Function	X	Y
1	CS[86]	2450	810
2	CS[87]	2310	810
3	CS[88]	2180	810
4	CS[89]	2060	810
5	CS[90]	1950	810
6	CS[91]	1850	810
7	CS[92]	1750	810
8	CS[93]	1650	810
9	CS[94]	1550	810
10	CS[95]	1450	810
11	VOUT	1350	810
12	CAP3P	1250	810
13	CAP1N	1150	810
14	CAP1P	1050	810
15	CAP2P	950	810
16	CAP2N	850	810
17	CAP4P	750	810
18	CAP5P	650	810
19	V0	550	810
20	V1	450	810
21	V2	350	810
22	V3	250	810
23	V4	150	810
24	ED[3]	50	810
25	ED[2]	-50	810
26	ED[1]	-150	810
27	ED[0]	-250	810
28	EIO1	-350	810
29	EIO2	-450	810
30	XCKPAD	-550	810
31	XDISPAD	-650	810
32	SIDPAD	-750	810

Pad No.	Function	X	Y
33	SCLKPAD	-850	810
34	FRPAD	-950	810
35	LP2PAD	-1050	810
36	LP1PAD	-1150	810
37	VSS	-1250	810
38	VDD	-1350	810
39	CS[0]	-1450	810
40	CS[1]	-1550	810
41	CS[2]	-1650	810
42	CS[3]	-1750	810
43	CS[4]	-1850	810
44	CS[5]	-1950	810
45	CS[6]	-2060	810
46	CS[7]	-2180	810
47	CS[8]	-2310	810
48	CS[9]	-2450	810
49	CS[10]	-2450	680
50	CS[11]	-2450	560
51	CS[12]	-2450	450
52	CS[13]	-2450	350
53	CS[14]	-2450	250
54	CS[15]	-2450	150
55	CS[16]	-2450	50
56	CS[17]	-2450	-50
57	CS[18]	-2450	-150
58	CS[19]	-2450	-250
59	CS[20]	-2450	-350
60	CS[21]	-2450	-450
61	CS[22]	-2450	-560
62	CS[23]	-2450	-680
63	CS[24]	-2450	-810
64	CS[25]	-2310	-810

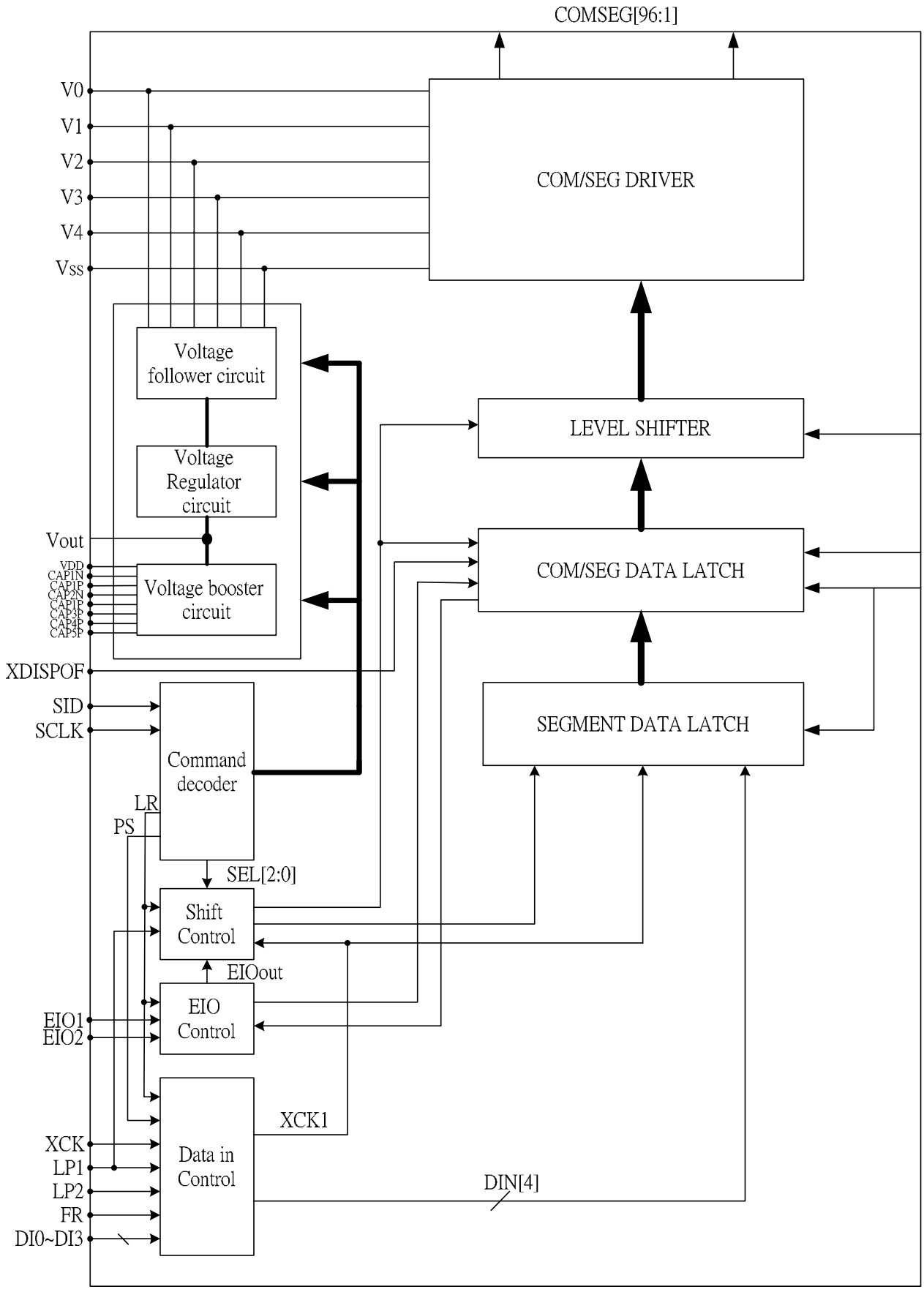
Pad No.	Function	X	Y
65	CS[26]	-2180	-810
66	CS[27]	-2060	-810
67	CS[28]	-1950	-810
68	CS[29]	-1850	-810
69	CS[30]	-1750	-810
70	CS[31]	-1650	-810
71	CS[32]	-1550	-810
72	CS[33]	-1450	-810
73	CS[34]	-1350	-810
74	CS[35]	-1250	-810
75	CS[36]	-1150	-810
76	CS[37]	-1050	-810
77	CS[38]	-950	-810
78	CS[39]	-850	-810
79	CS[40]	-750	-810
80	CS[41]	-650	-810
81	CS[42]	-550	-810
82	CS[43]	-450	-810
83	CS[44]	-350	-810
84	CS[45]	-250	-810
85	CS[46]	-150	-810
86	CS[47]	-50	-810
87	CS[48]	50	-810
88	CS[49]	150	-810
89	CS[50]	250	-810
90	CS[51]	350	-810
91	CS[52]	450	-810
92	CS[53]	550	-810
93	CS[54]	650	-810
94	CS[55]	750	-810
95	CS[56]	850	-810
96	CS[57]	950	-810
97	CS[58]	1050	-810

Pad No.	Function	X	Y
98	CS[59]	1150	-810
99	CS[60]	1250	-810
100	CS[61]	1350	-810
101	CS[62]	1450	-810
102	CS[63]	1550	-810
103	CS[64]	1650	-810
104	CS[65]	1750	-810
105	CS[66]	1850	-810
106	CS[67]	1950	-810
107	CS[68]	2060	-810
108	CS[69]	2180	-810
109	CS[70]	2310	-810
110	CS[71]	2450	-810
111	CS[72]	2450	-680
112	CS[73]	2450	-560
113	CS[74]	2450	-450
114	CS[75]	2450	-350
115	CS[76]	2450	-250
116	CS[77]	2450	-150
117	CS[78]	2450	-50
118	CS[79]	2450	50
119	CS[80]	2450	150
120	CS[81]	2450	250
121	CS[82]	2450	350
122	CS[83]	2450	450
123	CS[84]	2450	560
124	CS[85]	2450	680

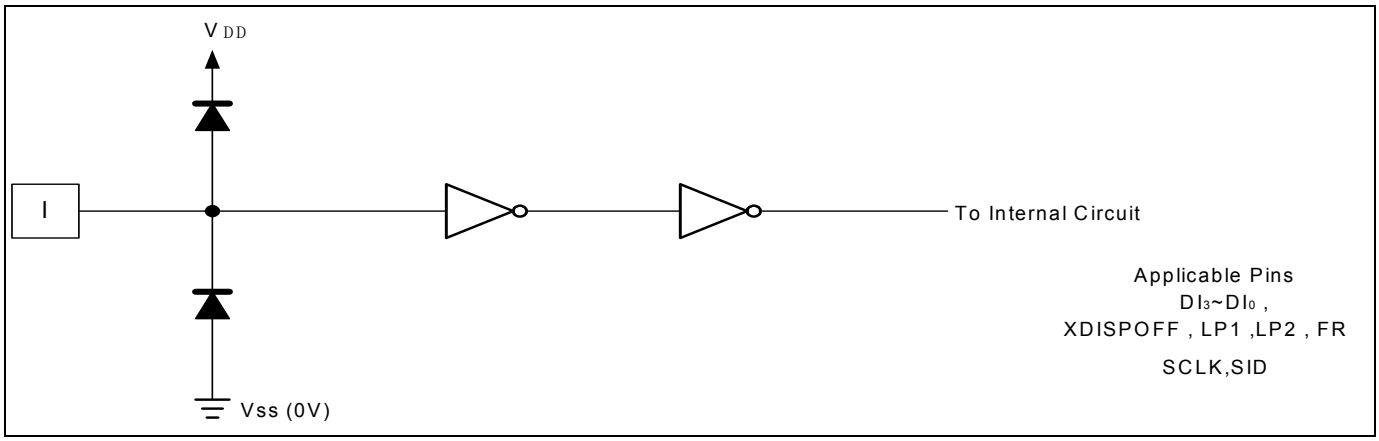
PIN DESCRIPTION

SYMBOL	I/O	DESCRIPTION	No of Num
$COMSEG_0$-$COMSEG_{95}$	O	LCD drive output	96
V_0~V_4	P	Power supply for LCD drive	5
V_{DD}	P	Power supply for logic system (+2.5 to +5.5 V)	1
EIO_2, EIO_1	I/O	Input/output for chip selection at segment mode and FLM input output function at com/seg mix mode or common mode	2
DI_0-DI_3	I	Display data input at segment mode	4
XCK	I	Clock input for taking display data at segment mode	1
XDISPOFF	I	Control input for output of non-select level	1
LP1	I	Latch pulse input for display data at segment mode	1
LP2	I	Shift clock input for shift register at common mode	1
FR	I	AC-converting signal input for LCD drive waveform	1
V_{SS}	P	Ground (0 V)	1
CAP1-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	1
CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	1
CAP2-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	1
CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	1
CAP3+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	1
CAP4+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	1
CAP5+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	
VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS.	1
SID	I	The command data. See Figure1	1
SCLK	I	The serial clock input. See Figure1	1

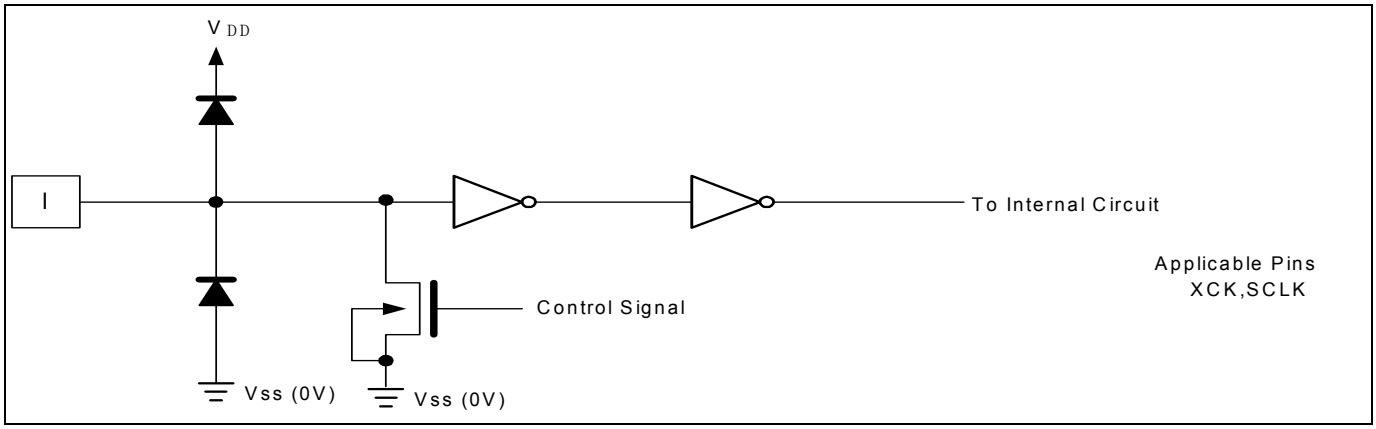
BLOCK DIAGRAM



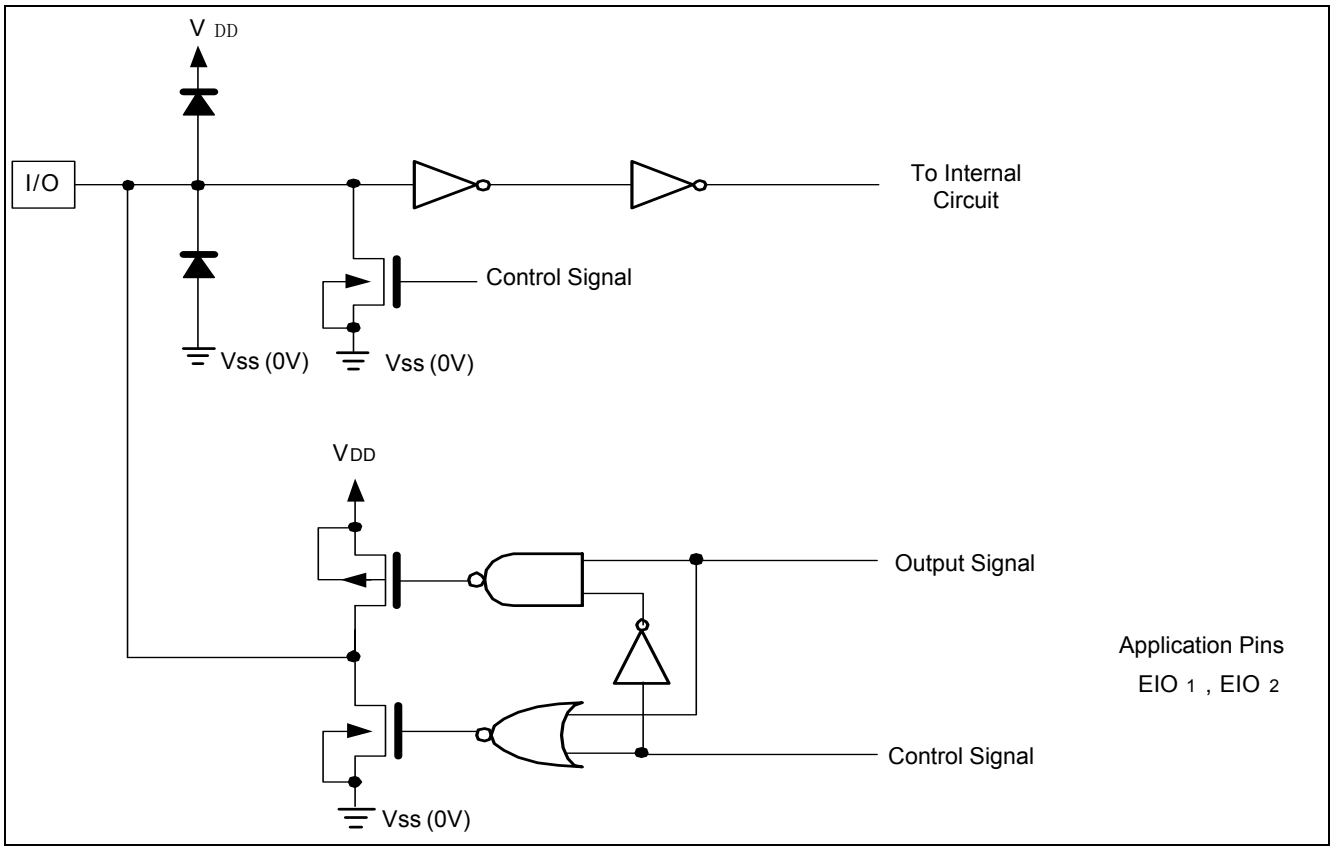
NPUT/OUTPUT CIRCUITS



Input Circuit (1)



Input Circuit (2)



Input/Output Circuit

FUNCTIONAL DESCRIPTION

(Segment mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_0 V_1 V_2 V_3 V_4	This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VSS, and must maintain the relative magnitudes shown below. $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{ss}$ When the power supply turns on, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
DI_3-DI_0	Input pins for display data • In 4-bit parallel input mode, input data into the 4 pins, DI_3-DI_0. • In serial input mode, input data into the 1 pin,DI_0. Then DI_3-DI_1 must connect to V_{SS} . • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
LP1	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
XDISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to VSS level "L", the LCD drive output pins ($COMSEG_1$-$COMSEG_{96}$) are set to level Vss. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of XDISPOFF. When the XDISPOFF function is canceled, the driver outputs non-select level (V_2 or V_3), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if XDISPOFF removal time does not correspond to what is shown in AC characteristics, it cannot output the reading data correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
EIO_1, EIO_2	Input/output pins for chip selection.

	AT segment mode: • When L/R register is set '0' , EIO_1 is set for output, and EIO_2 is set for input(connect to Vss). • When L/R register is set '1', EIO_1 is set for input(connect to Vss), and EIO_2 is set for output. • During output, set to "H" while LP • XCK is "H" and after 96 bits of data have been read, set to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 96 bits of data have been read.
$COMSEG_1$ –$COMSEG_{96}$	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V_0, V_2 ,V_3,V_{ss}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
CAP1-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP1+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP2-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP2+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP3+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP4+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
VOUT	DC/DC voltage converter. Connect a capacitor between this terminal and VSS.
SID	The serial command data. See Figure1
SCLK	The serial clock input. See Figure1

(Common mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_0, V_1 V_2, V_3 V_4	This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below. $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{ss}$ When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
LP2	Shift clock pulse input pin for bi-directional shift register • * Data is shifted at the falling edge of the clock pulse. • When use gray scale mode, then must use the pin. • When use monochrome mode, then the pin should be connected with LP1 together.
XDISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins ($COMSEG_0$-$COMSEG_x$) are set to level Vss. • When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V_1 or V_4), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
DI_3-DI_0	Not used. Connect DI_3-DI_0 to V_{SS}, not floating.
XCK	Not used • XCK is pulled down in common mode, so connect to V_{SS} .
$COMSEG_0$ –$COMSEG_{95}$	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V_0 V_1, V_4, or V_{SS}) is Selected and output. Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.

EIO_1, EIO_2	Shift data Input/output pins for shift register • EIO_1 is output pin when L/R is at Vss level "L", EIO_1 is input pin when L/R is at Vdd level "H" • When L/R register ='1', EIO_1 is used as input pin, it will be connect to FLM. • When L/R register ='0', EIO_1 is used as output pin, it won't be connect to FLM. • EIO_2 is input pin when L/R is at Vss level "L", EIO_1 is output pin when L/R is at Vdd level "H" • When L/R register ='1', EIO_2 is used as output pin, it won't be connect to FLM, • When L/R register ='0', EIO_2 is used as input pin, it will be connect to FLM • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
CAP1-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP1+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP2-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP2+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP3+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP4+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
VOUT	DC/DC voltage converter. Connect a capacitor between this terminal and VSS.
SID	The serial command data. See Figure1
SCLK	The serial clock input. See Figure1

(common /segment mix mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_0 V_1 V_2 V_3 V_4	This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VSS, and must maintain the relative magnitudes shown below. $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{ss}$ When the power supply turns ON, the internal power supply circuits produce the V1to V4voltages shown below. The voltage settings are selected using the LCD bias set command.
DI_3-DI_0	Input pins for display data • In 4-bit parallel input mode, input data into the 4 pins, DI_3-DI_0. • In serial input mode, input data into the 1 pin,DI_0. Connect DI_3-DI_1 to V_{SS} . • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
XCK	Clock input pin for taking display data * Data is read at the falling edge of the clock pulse.
LP1	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
LP2	Shift clock pulse input pin for bi-directional shift register • * Data is shifted at the falling edge of the clock pulse. • When use gray scale mode, then must use the pin. • When use monochrome mode, then the pin should be connected with LP1 together.
XDISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to VSS level "L", the LCD drive output pins ($COMSEG_0$-$COMSEG_{95}$) are set to level Vss. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of XDISPOFF. When the XDISPOFF function is canceled, the driver outputs non-select level (V_2 or V_3), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if XDISPOFF removal time does not correspond to what is shown in AC characteristics, it cannot output the reading data correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal.

	• The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
EIO_1, EIO_2	Input/output pins for chip selection AT common/segment mode: • When L/R register is '0' , EIO_1 is set output, and EIO_2 is set for input. EIO_1 : segment chip enable output, as default segment is enabled internally and be non-selected after 16,32,48,64 or 80 bits of data have been read. Depend on select mode. EIO_2 :common shift data input, no sift data output • When L/R register is '1', EIO_1 is set for input, and EIO_2 is set for output. EIO_1 :common shift data, no shift data output EIO_2 : segment chip enable output, as default segment is enabled internally and be non-selected after 16,32,48,64 or 80 bits of data have been read. Depend on select mode. • During output, set to "H" while LP • XCK is "H" and after 96 bits of data have been read, set to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 96 bits of data have been read.
$COMSEG_1$ –$COMSEG_{96}$	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V_0, V_2 ,V_3,V_{ss}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
CAP1-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP1+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP2-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP2+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP3+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP4+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
VOUT	DC/DC voltage converter. Connect a capacitor between this terminal and VSS.
XCS	This is the command mode select pin. When XCS="L" then write command to the LCD, when not used the command mode then must fixed to Vdd . See Figure1
SID	The command data. See Figure1
SCLK	The serial clock input. See Figure1

Functional Operations

TRUTH TABLE

(Segment Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (COMSEG0-COMSEG95)
L	L	H	V_3
L	H	H	V_{ss}
H	L	H	V_2
H	H	H	V_0
X	X	L	V_{ss}

(Common Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (COMSEG0-COMSEG95)
L	L	H	V_4
L	H	H	V_0
H	L	H	V_1
H	H	H	V_{ss}
X	X	L	V_{ss}

NOTES:

- L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

  There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.

  Supply regular voltage that is assigned by specification for each power pin.

RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(Segment Mode)

(A) 4-bit Parallel Input Mode

L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
				24 CLOCK	23 CLOCK	22 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI_0	$COMSEG_0$	$COMSEG_4$	$COMSEG_8$	…	$COMSEG_{84}$	$COMSEG_{88}$	$COMSEG_{92}$
			DI_1	$COMSEG_1$	$COMSEG_5$	$COMSEG_9$	…	$COMSEG_{85}$	$COMSEG_{89}$	$COMSEG_{93}$
			DI_2	$COMSEG_2$	$COMSEG_6$	$COMSEG_{10}$	…	$COMSEG_{86}$	$COMSEG_{90}$	$COMSEG_{94}$
			DI_3	$COMSEG_3$	$COMSEG_7$	$COMSEG_{11}$	…	$COMSEG_{87}$	$COMSEG_{91}$	$COMSEG_{95}$
H	Input	Output	DI_0	$COMSEG_{95}$	$COMSEG_{91}$	$COMSEG_{87}$	…	$COMSEG_{11}$	$COMSEG_7$	$COMSEG_3$
			DI_1	$COMSEG_{94}$	$COMSEG_{90}$	$COMSEG_{86}$	…	$COMSEG_{10}$	$COMSEG_6$	$COMSEG_2$
			DI_2	$COMSEG_{93}$	$COMSEG_{89}$	$COMSEG_{85}$	…	$COMSEG_9$	$COMSEG_5$	$COMSEG_1$
			DI_3	$COMSEG_{92}$	$COMSEG_{88}$	$COMSEG_{84}$	…	$COMSEG_8$	$COMSEG_4$	$COMSEG_0$

(B) Serial Input Mode

L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
				120 CLOCK	119 CLOCK	118 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI_0	$COMSEG_0$	$COMSEG_1$	$COMSEG_2$	…	$COMSEG_{93}$	$COMSEG_{94}$	$COMSEG_{95}$
			DI_1	X	X	X	X	X	X	X
			DI_2	X	X	X	X	X	X	X
			DI_3	X	X	X	X	X	X	X
H	Input	Output	DI_0	$COMSEG_{95}$	$COMSEG_{94}$	$COMSEG_{93}$	…	$COMSEG_2$	$COMSEG_1$	$COMSEG_0$
			DI_1	X	X	X	X	X	X	X
			DI_2	X	X	X	X	X	X	X
			DI_3	X	X	X	X	X	X	X

(Common Mode)

L/R	DATA TRANSFER DIRECTION	EIO_1	EIO_2
L	$COMSEG_{95} \rightarrow COMSEG_0$	Output	Input
H	$COMSEG_0 \rightarrow COMSEG_{95}$	Input	Output

MIX MODE(SEGMENT/ COMMON MODE)

When (SEL2,SEL1,SEL0)=(0,1,0)➔ SELECT THE 32 COM / 64 SEGMENT MODE

THEN SEGMENT SIDE OF MIX MODE

(A) 4-bit Parallel Input Mode

L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
				16 CLOCK	15 CLOCK	14 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Seg_end Output	Com_FLM Input	DI_0	$COMSEG_0$	$COMSEG_4$	$COMSEG_8$	…	$COMSEG_{52}$	$COMSEG_{56}$	$COMSEG_{60}$
			DI_1	$COMSEG_1$	$COMSEG_5$	$COMSEG_9$	…	$COMSEG_{53}$	$COMSEG_{57}$	$COMSEG_{61}$
			DI_2	$COMSEG_2$	$COMSEG_6$	$COMSEG_{10}$	…	$COMSEG_{54}$	$COMSEG_{58}$	$COMSEG_{62}$
			DI_3	$COMSEG_3$	$COMSEG_7$	$COMSEG_{11}$	…	$COMSEG_{55}$	$COMSEG_{59}$	$COMSEG_{63}$
H	Com_FLM Input	Seg_end Output	DI_0	$COMSEG_{95}$	$COMSEG_{91}$	$COMSEG_{87}$	…	$COMSEG_{43}$	$COMSEG_{39}$	$COMSEG_{35}$
			DI_1	$COMSEG_{94}$	$COMSEG_{90}$	$COMSEG_{86}$	…	$COMSEG_{42}$	$COMSEG_{38}$	$COMSEG_{34}$
			DI_2	$COMSEG_{93}$	$COMSEG_{89}$	$COMSEG_{85}$	…	$COMSEG_{41}$	$COMSEG_{37}$	$COMSEG_{33}$
			DI_3	$COMSEG_{92}$	$COMSEG_{88}$	$COMSEG_{84}$	…	$COMSEG_{40}$	$COMSEG_{36}$	$COMSEG_{32}$

(B) Serial Input Mode

L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
				64 CLOCK	63 CLOCK	62CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Seg_end Output	Com_FLM Input	DI_0	$COMSEG_0$	$COMSEG_1$	$COMSEG_2$	…	$COMSEG_{61}$	$COMSEG_{62}$	$COMSEG_{63}$
			DI_1	X	X	X	X	X	X	X
			DI_2	X	X	X	X	X	X	X
			DI_3	X	X	X	X	X	X	X
H	Com_FLM Input	Seg_end Output	DI_0	$COMSEG_{95}$	$COMSEG_{94}$	$COMSEG_{93}$	…	$COMSEG_{34}$	$COMSEG_{33}$	$COMSEG_{32}$
			DI_1	X	X	X	X	X	X	X
			DI_2	X	X	X	X	X	X	X
			DI_3	X	X	X	X	X	X	X

COMMON SIDE OF MIX MODE

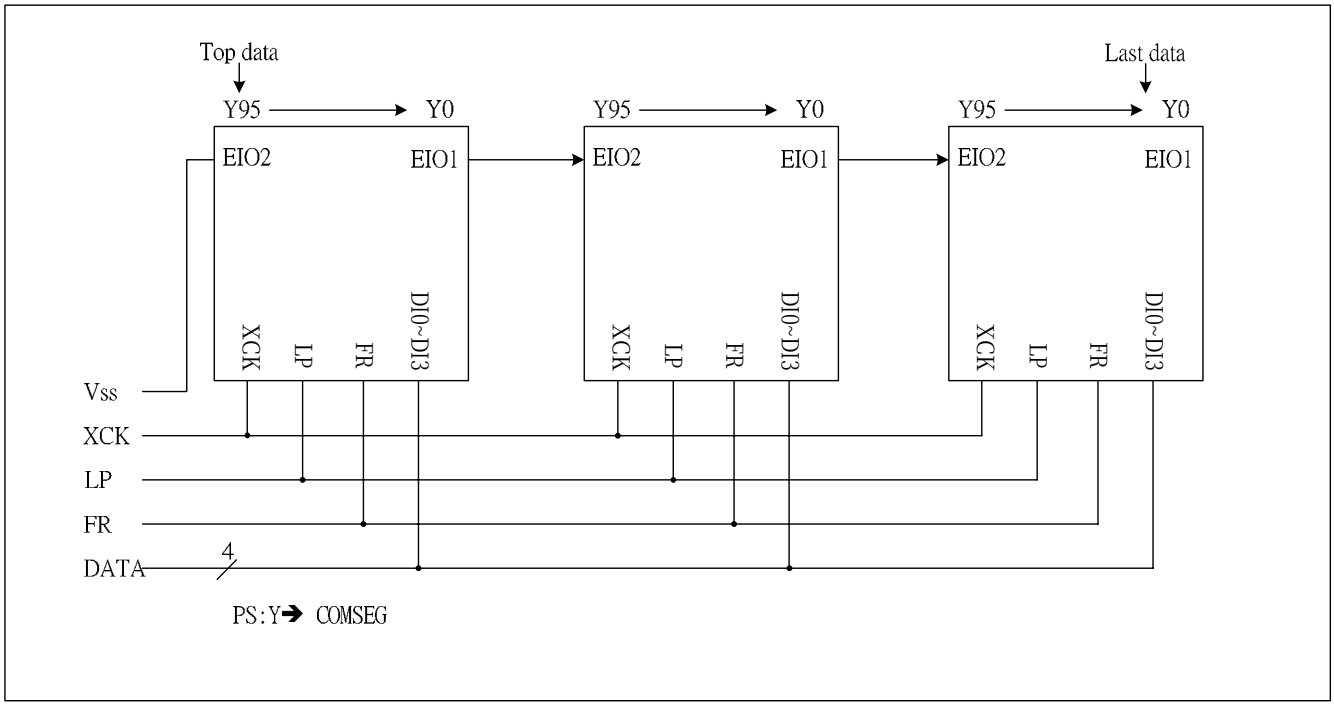
L/R	DATA TRANSFER DIRECTION	EIO_1	EIO_2
L	$COMSEG_{95}$ → $COMSEG_{62}$	Seg_end output	Input
H	$COMSEG_0$ → $COMSEG_{31}$	Input	Seg_end output

NOTES:

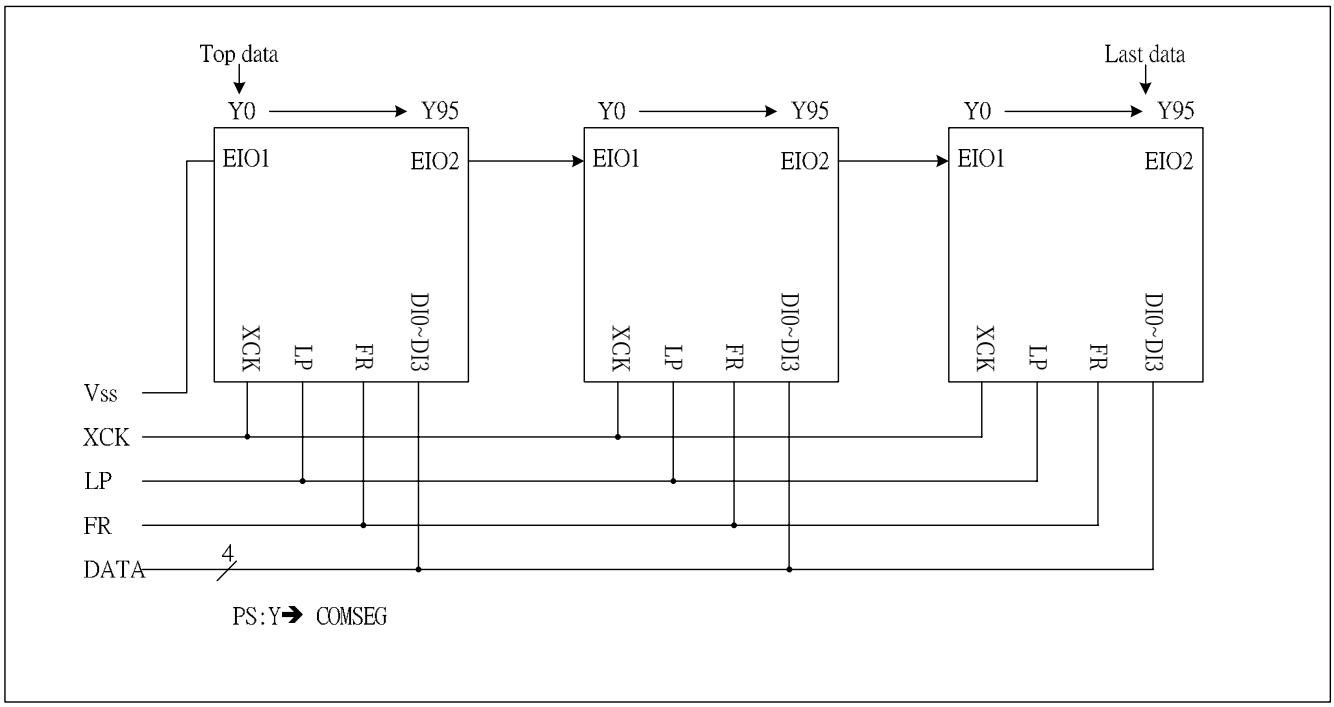
- L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

Connection examples of plural segment drivers in 4-bits interface(288 segment)

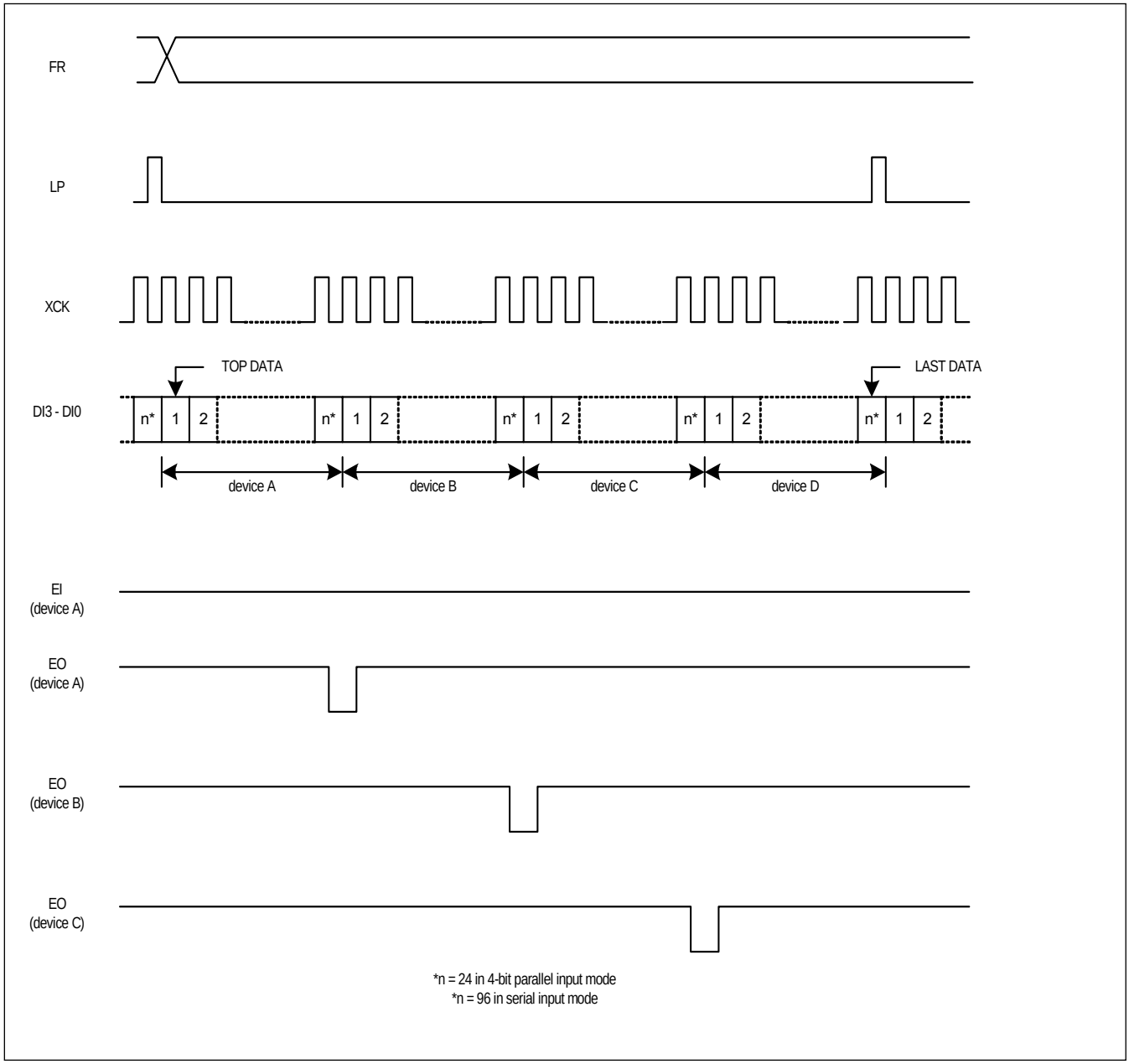
(a) When the L/R register set "L" level



(b) When the L/R register set "H" level

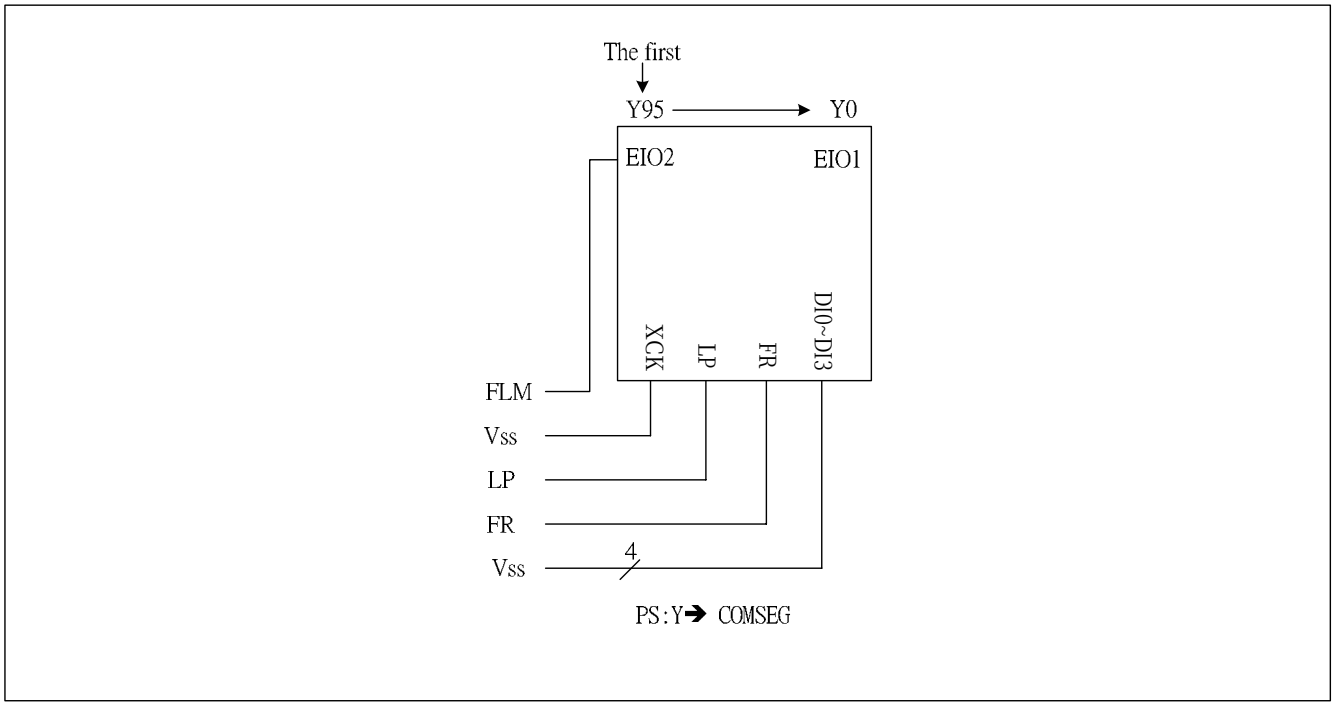


Timing chart of 4-device cascade connection of segment drivers

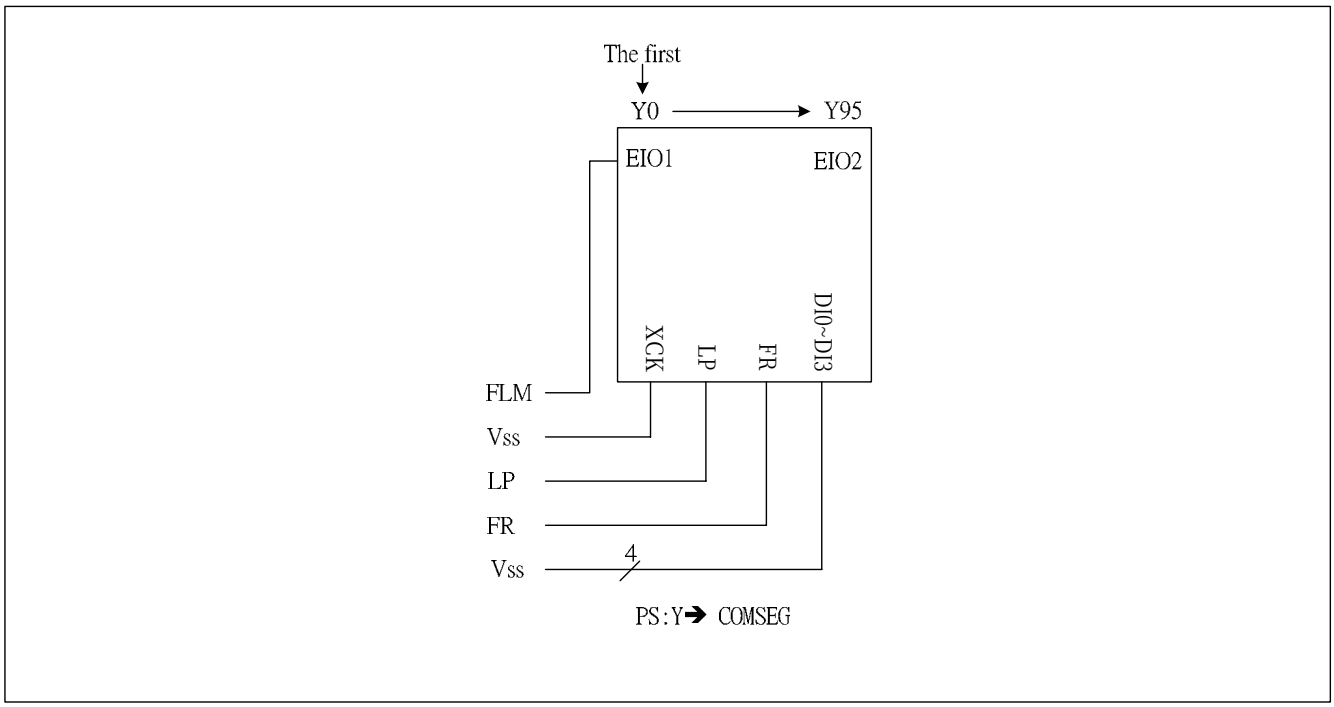


Connection examples for signal common drivers (96 common)

(c) When the L/R register set "L" level



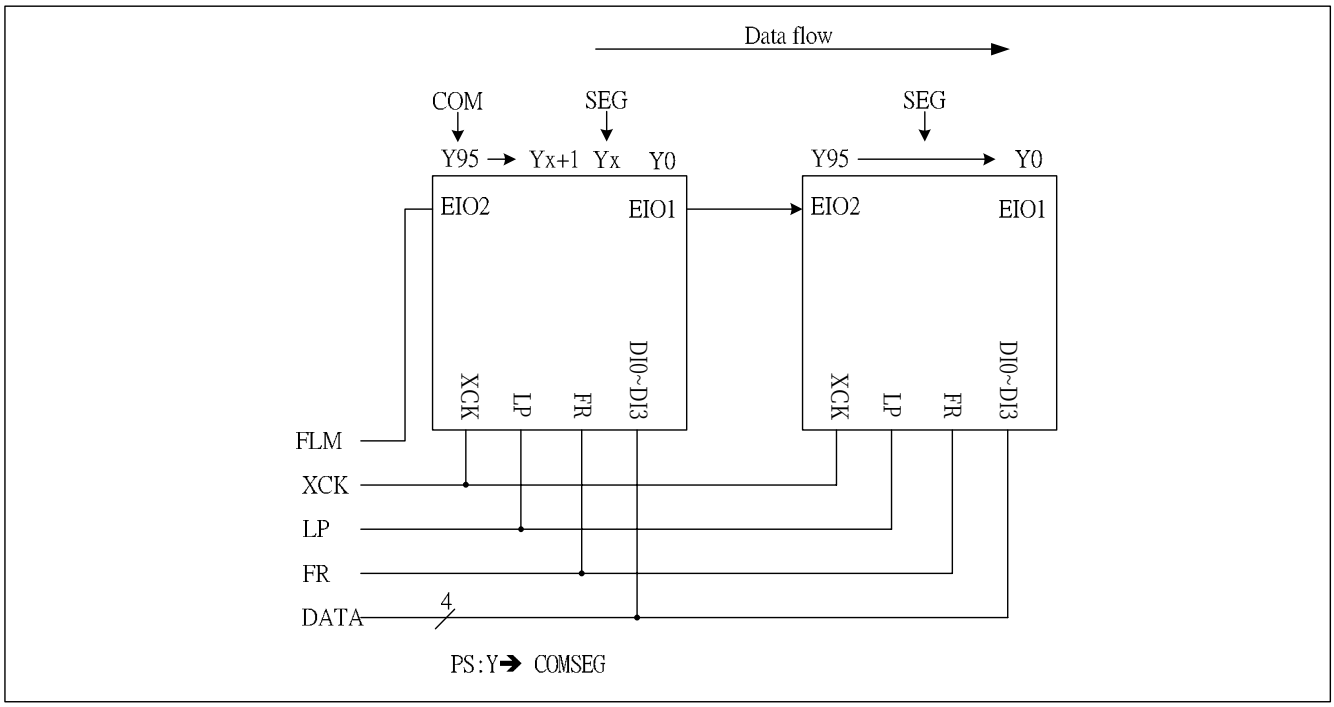
(d) When the L/R register set "H" level



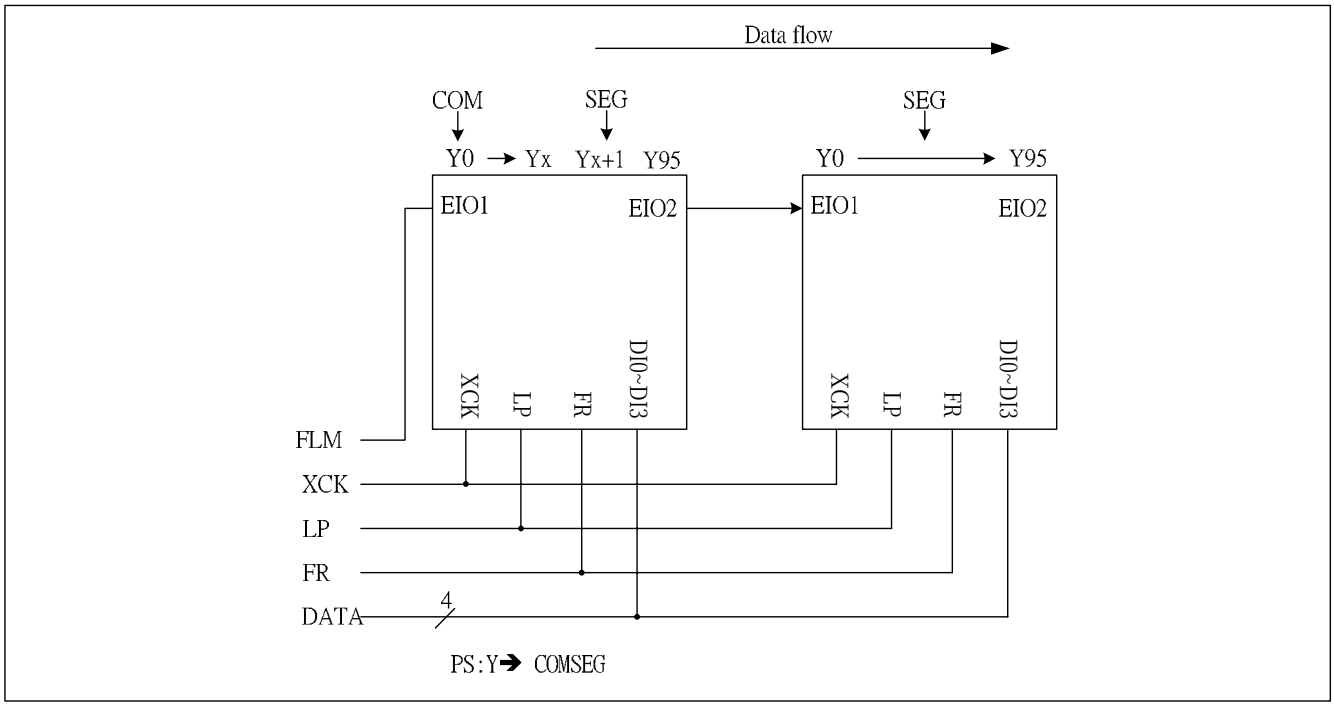
Connection examples for plural common/segment (mix mode) drivers

The mix mode is 1/16, 1/32, 1/48, 1/64, 1/80, 1/96 duty mode

(e) When the L/R register set "L" level



(f) When the L/R register set "H" level



PRECAUTIONS

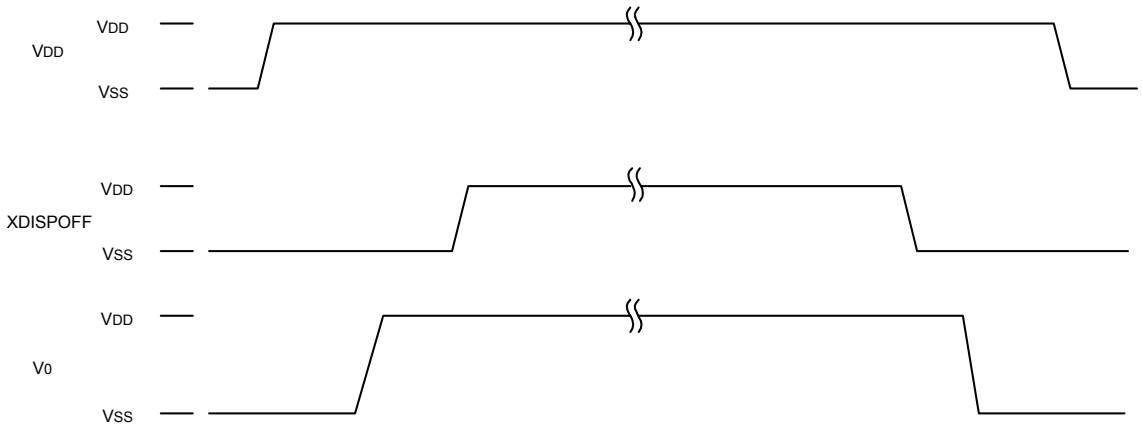
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so a high current that may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating may permanently damage it. The details are as follows,

When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on XDISPOFF function. After that, cancel the XDISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level Vss on XDISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here



DESCRIPTION FUNCTIONS

The MPU Interface

Selecting the Interface Type

With the ST8012 chips, data transfers are done through an 4-bit parallel data bus (D3 to D0) or through a serial data input (SI). Through selecting the P/S regoster to the “H” or “L” it is possible to select either parallel data input or serial data input as shown in Table 1.

Table 1

P/S register	D_0	D_3~D_1
H: Parallel Input	D_0	D_3~D_1
L: Serial Input	SI	VDD

Command Serial Interface

With the ST8009 chips, command data transfers are done through a serial data input. And it’s timing show in Figure1.

Serial Interface

The serial interface send the commands sent via the serial Interface. It could send command it to the register. The two lines are a Serial Data line (SDI) and a Serial Clock line (SCLK). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDI line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.2.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.3.

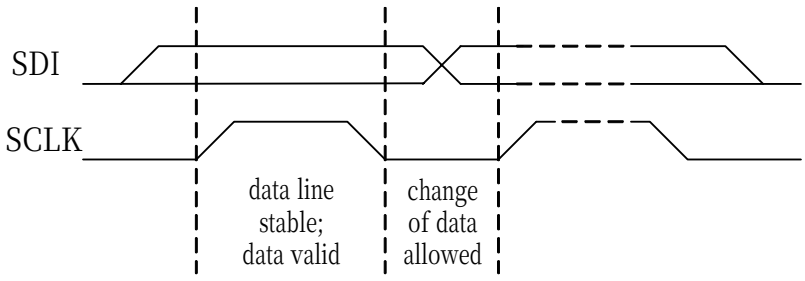


Fig .2 Bit transfer

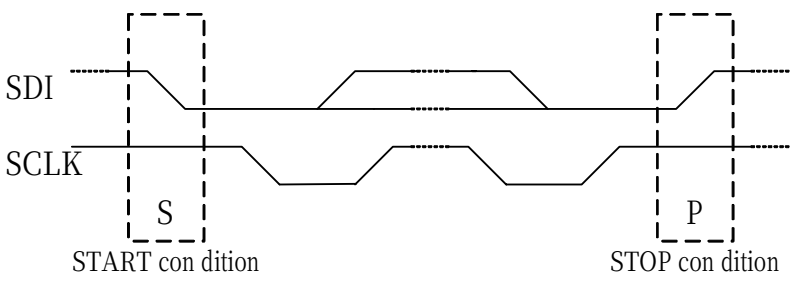


Fig .3 Definition of START and STOP conditions

The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the LCD drivers. They are Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation, when the mode is in common mode or common/segment mode. The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 2 shows the Power Control Set Command 3-bit data control function, and Table 3 shows reference combinations.

Table2

bit			Function	Status	
				"1"	"0"
D2	D1	D0	Booster circuit control bit	ON	OFF
D2	D1	D0	Voltage regulator circuit control bit (V/R circuit)	ON	OFF
D2	D1	D0	Voltage follower circuit control bit (V/F circuit)	ON	OFF

The Control Details of Each Bit of the Power Control Set Command

Table3

Use Settings	Com / Seg	D2	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Step-up voltage
Only the internal power supply is used	Com mode / Com/Seg mode	1	ON	ON	ON	VDD	Used
Only the voltage regulator circuit and the voltage follower circuit are used		0	OFF	ON	ON	VOUT, VDD	Open
Only the internal power supply is used	Seg mode	1	ON	ON	ON	VDD	Used
Only the voltage regulator circuit and the voltage follower circuit are used		0	OFF	ON	ON	VOUT, VDD	Open

The Step-up Voltage Circuits

Using the step-up voltage circuits equipped within the ST8009 chips it is possible to product a 2X, 3X, 4X, 5X or 6X step-up of the V_{DD} – V_{SS} voltage levels.

6X step-up:

Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, between CAP2+ and CAP4–,between CAP1+ and CAP5–, and between V_{DD} and V_{OUT}, to produce a voltage level in the negative direction at the V_{OUT} terminal that is 6 times the voltage level between V_{DD} and V_{SS}.

5X step-up:

Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, between CAP2+ and CAP4–,and between V_{DD} and V_{OUT}, to produce a voltage level in the negative direction at the VOUT terminal that is 5 times the voltage level between V_{DD} and V_{SS}.

4X

step-up:

Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, and between V_{DD} and V_{OUT}, to produce a voltage level in the negative direction at the V_{OUT} terminal that is 4 times the voltage level between V_{DD} and V_{SS}.

3X step-up:

Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2– and between V_{DD} and V_{OUT},and short between CAP3– and V_{OUT} to produce a voltage level in the negative direction at the V_{OUT} terminal that is 3 times the voltage difference between V_{DD} and V_{SS}. The step-up voltage relationships are shown in Figure4.

2X step-up:

Connect capacitor C1 between CAP1+ and CAP1–, and between V_{DD} and V_{OUT}, leave CAP2+ open, and short between CAP2–, CAP3– and V_{OUT} to produce a voltage in the negative direction at the V_{OUT} terminal that Is twice the voltage between V_{DD} and V_{SS}.

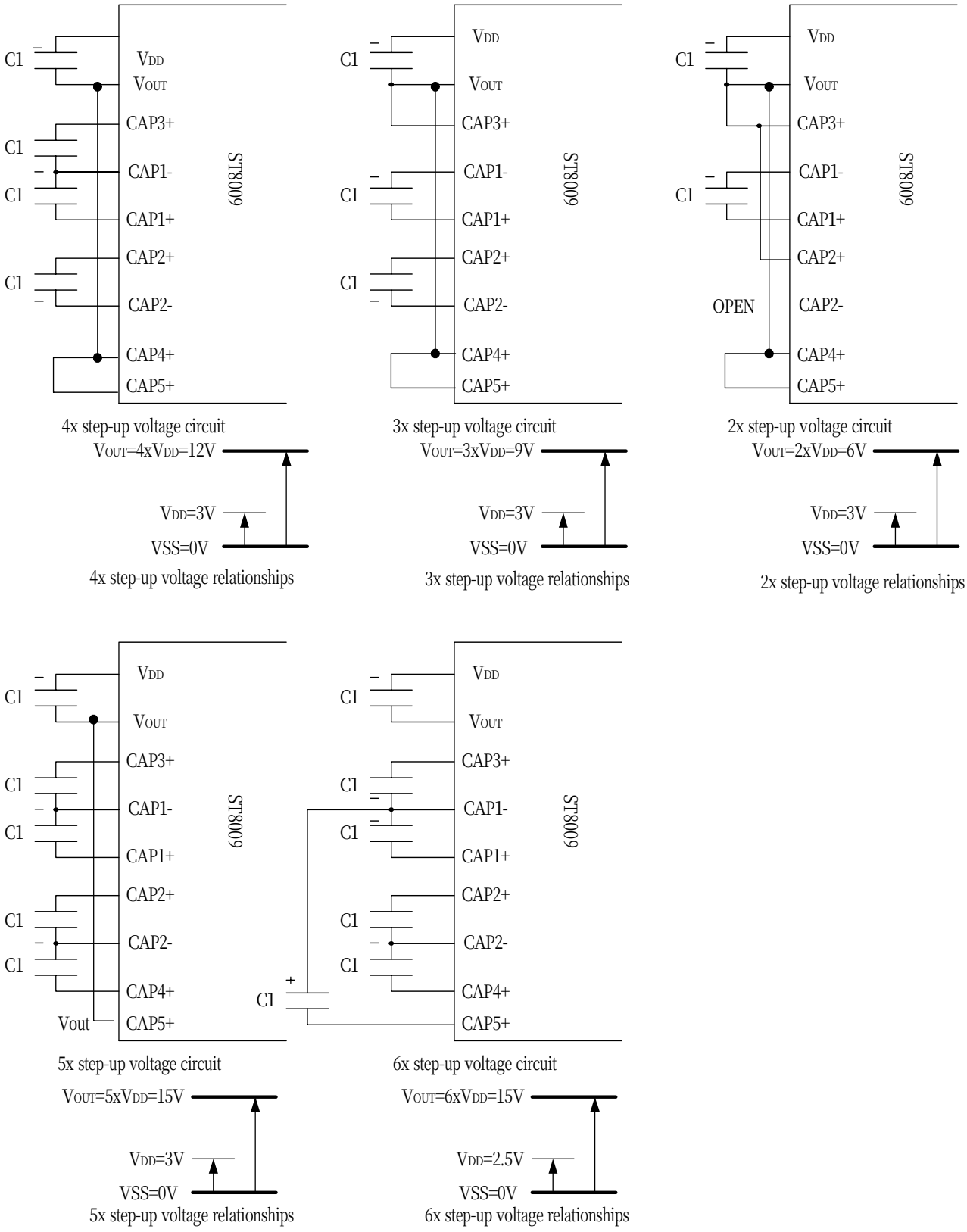


Figure4

* The V_{SS} voltage range must be set so that the V_{OUT} terminal voltage does not exceed the absolute maximum rated value.

The Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the LCD driver voltage V0 through the voltage regulator circuit. Because the ST8009 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.(VREG thermal gradients approximate -0.05%/°C)

(A) When the V0 Voltage Regulator Internal Resistors Are Used

Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where

| V0 | < | VOUT|

$$V_0 = \left(1 + \frac{Rb}{Ra}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{Rb}{Ra}\right) \bullet \left(1 - \frac{\alpha}{200}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{200}\right) \bullet V_{REG}\right]$$

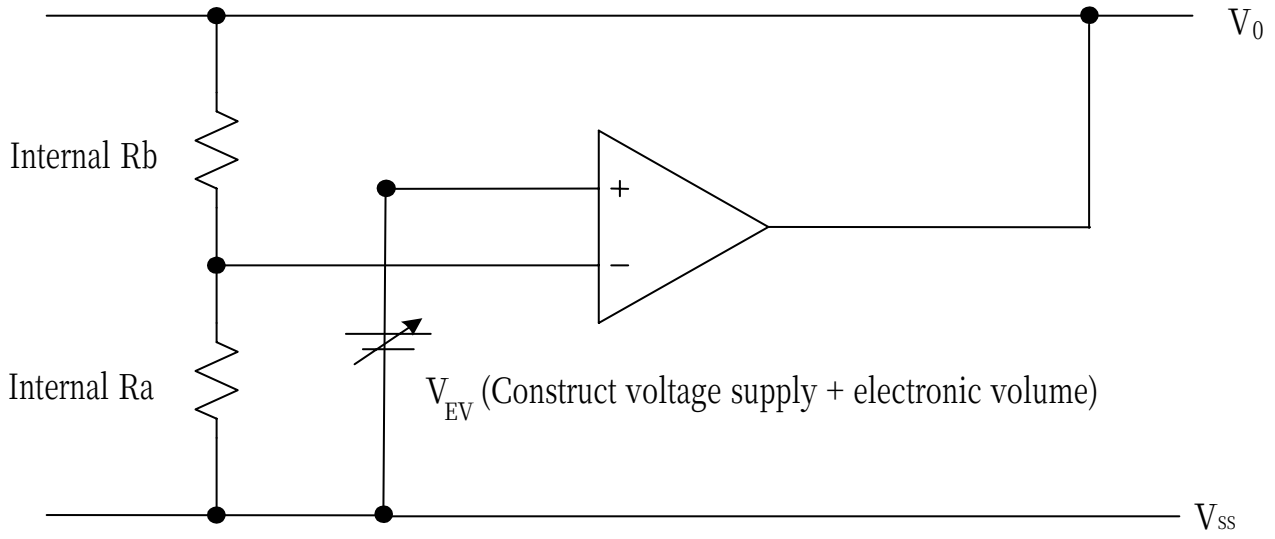


Figure5

VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 4.

Part no.	Equipment Type	Thermal Gradient	V_{REG}
ST8009	Internal Power Supply	–0.05 %/°C	2.1V

Table4

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 5 shows the value for α depending on the electronic volume register settings.

Rb/Ra is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The Rb/Ra ratio assumes the values shown in Table 6 depending on the 3-bit data settings in the VDD voltage regulator internal resistor ratio register.

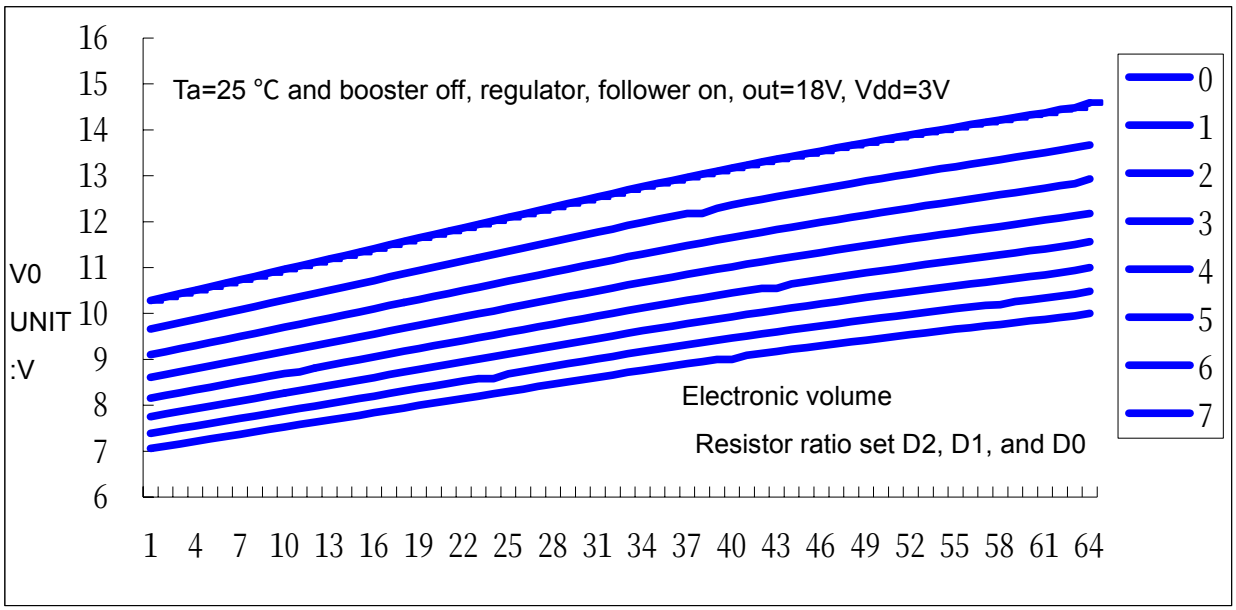
Table5

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			:			:
			:			:
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

V_0 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table6

Register			ST8009
D2	D1	D0	(1) –0.05 %/°C
0	0	0	5.0
0	0	1	5.22
0	1	0	5.48
0	1	1	5.76
1	0	0	6.07
1	0	1	6.42
1	1	0	6.81
1	1	1	7.25



The LCD Voltage Generator Circuit

The V_0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3, and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3 and V_4 to the liquid crystal drive circuit.

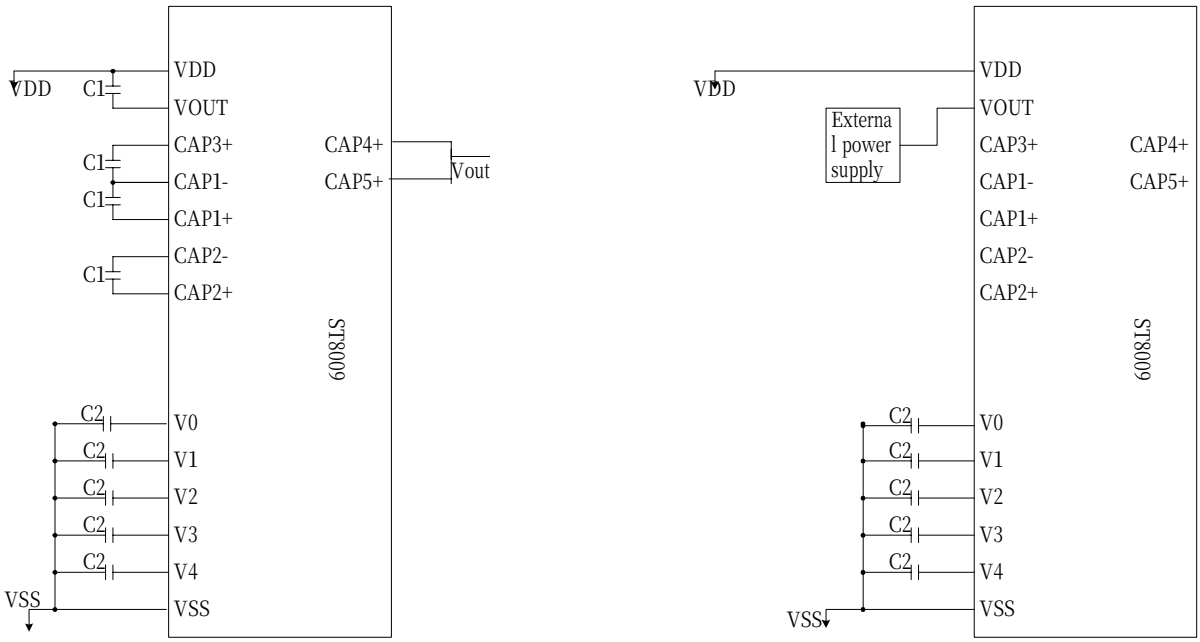
Reference Circuit Examples

Figure 6 shows reference circuit examples.

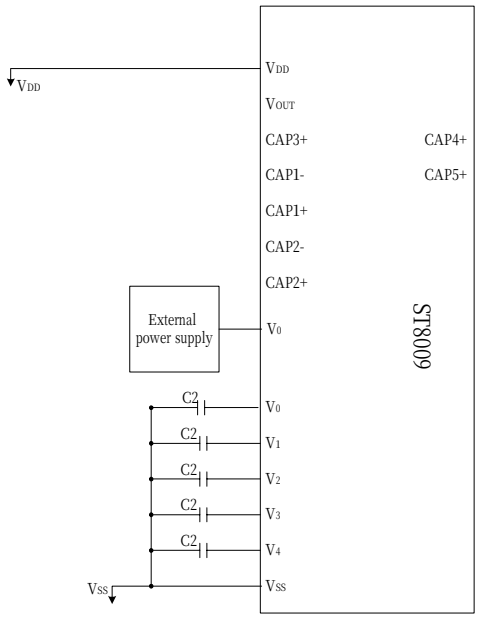
1. When used all of the step-up circuit, voltage regulating circuit and V/F circuit.
   (Example with 4x setup-up)

2. When the voltage regulator circuit and V/F circuit alone are used

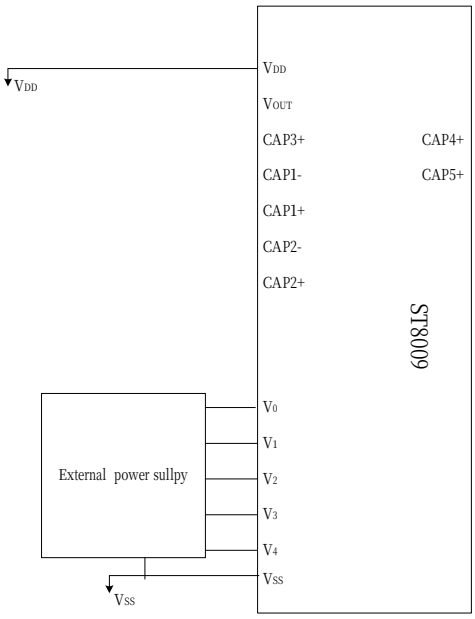
Figure 6



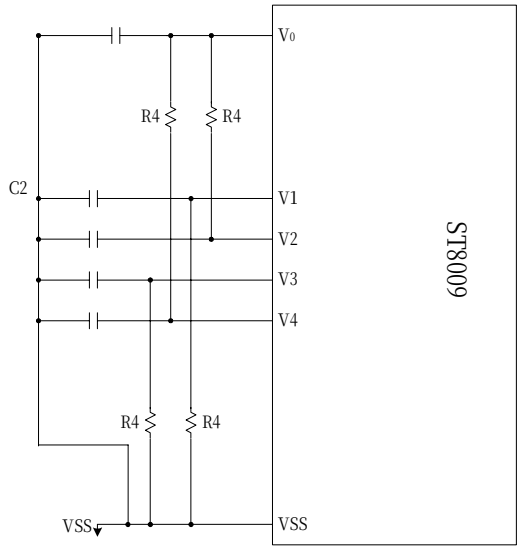
3. When the V/F circuit alone is used



4.When the built-in power is not used



5. When the built-in power circuit is used to drive a liquid crystal panel heavily loaded with AC or DC, it is recommended to connect an external resistor to stabilize potentials of V_1, V_2, V_3 and V_4 which are output from the built-in voltage follower. Examples of shared reference settings When V_0 can vary between 7V and 14 V



Item	Set value	units
c1	1.0 to 4.7	uF
c2	0.1 to 4.7	uF

C1 and C2 are determined by the size of the LCD being driven

Reference set value R4:100K Ω ~ 1M Ω it is recommended to set an optimum resistance value R4 taking the liquid crystal display and the drive waveform

* 1. Because the VR terminal input impedance is high, use short leads and shielded lines.
* 2. C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

Example of the Process by which to Determine the Settings:

• Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to V_{OUT} from the outside.

• Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the liquid crystal drive voltages (V_1 to V_4). Note that all C2 capacitors must have the same capacitance value.

• Next turn all the power supplies ON and determine C1.

Instruction Table

Instruction	Instruction Code								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
Interface control selection	0	0	0	0	0	M	LR	PS	Interface selection and set
Software Reset	0	0	0	1	0	0	0	XRST	Software reset, when set the register then the ST8009 will be reset
LCD Duty selection	0	0	1	0	0	DU2	DU1	DU0	The register can select the LCD duty numbers
LCD Bias Set	0	0	1	1	0	B2	B1	B0	The register can select the LCD bias
Power Controller Set	0	1	0	1	0	B	R	F	Set the power mode. The register contain three power circuits can select (booster, regulator, follow)
Booster Frequency Set	1	0	0	0	0	F2	F1	F0	Set the booster frequency
V0 Voltage Regulator Internal Resistor Ratio Set	1	0	0	1	0	Rab2	Rab1	Rab0	Select internal resistor ratio(Ra/Rb) mode
Electronic Volume Register Set	1	1	E5	E4	E3	E2	E1	E0	Set the V0 output voltage electronic volume register

Instruction Description

The ST8009 identify the data bus signals by a combination of SID,SCLK signals.

Interface control

The register can control frame direction, com, seg, com/seg direction and serial or parallel (4-bits) input data interface.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	M	LR	PS

M: Frame direction control bit

When M=" Height", the internal frame direction and external frame direction are the same. (normally)

When M=" Low", the internal frame direction and external frame direction are adverse.

LR: COMSEG output direction control bit

When LR="Height", the direction is normal.

When LR="Low", the direction is inverse.

LR="H"	COMSEG0	→	COMSEG95
LR="L"	COMSEG95	→	COMSEG0

PS: Data Interface mode select control bit

When PS="Height" , the data input interface is serial

When PS="Low" , the data input interface is parallel (4-bits)

Software Reset

The Software Reset will be initialized or cleared whenever the command enable signal is disabled.

On the other word, remember to release the Software reset state by disable the command enable signal once the Software Reset is written.

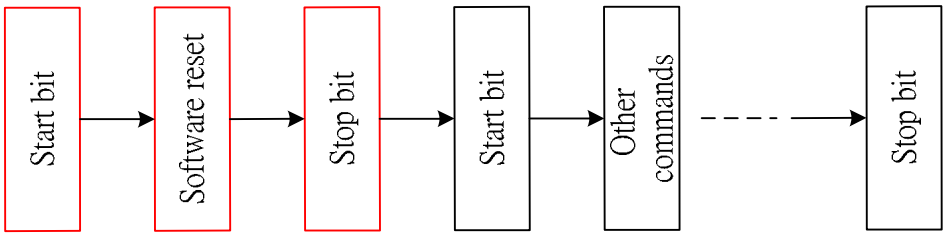
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	XRST

Only this command (software reset) ,when used then must set the both start bit and stop bit to write and finished it.

Because it's independent and different to other commands so can't write continue with other data.

Note: Other commands can write continue so they can use only one start bit and stop bit to finished a serial of commands.

When use the software then please conform to the follow path:



LCD Duty selection

ST8009 can set the display duty by software from internal register. This command cans selection the liquid crystal display duty.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	DU2	DU1	DU0

DU2	DU1	DU0	COM Numbers	SEG Numbers
0	0	0	0	96
0	0	1	16	80
0	1	0	32	64
0	1	1	48	48
1	0	0	64	32
1	0	1	80	16
1	1	0	96	0
1	1	1	96	0

LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

ST8009 has eight bias modes can select.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	B2	B1	B0

B2	B1	B0	Bias select
0	0	0	1/4
0	0	1	1/5
0	1	0	1/6
0	1	1	1/7
1	0	0	1/8
1	0	1	1/9
1	1	0	1/10
1	1	1	1/11

Power Controller Set

This command sets the power supply circuit functions. See the function explanation in “The Power Supply Circuit,” for details

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	B	R	F

B	R	F	Status
0	--	--	Booster circuit : on
1	--	-	Booster circuit : off
--	0	--	Regulator circuit : on
--	1	--	Regulator circuit : off
--	--	0	Follower circuit : on
--	--	1	Follower circuit : off

Booster Frequency Set

By using this command to set three bits of data to the booster frequency, the liquid crystal drive Booster Frequency assumes one of the 8 frequency .When this command is input, the booster frequency register has been set.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	F2	F1	F0

F2	F1	F0	Booster Frequency
0	0	0	1K
0	0	1	2K
0	1	0	3K
0	1	1	4K
1	0	0	5K
1	0	1	6K
1	1	0	7K
1	1	1	8K

V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V_0 voltage regulator internal resistor ratio.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	Rab2	Rab1	Rab0

Rab2	Rab1	Rab0	Ra/Rb Ratio
0	0	0	Small ↓ Large
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

The Electronic Volume

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the LCD drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume registers set command, and both commands must be issued one after the other.

Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V0 assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume register has been set.

D7	D6	D5	D4	D3	D2	D1	D0
1	1	E5	E4	E3	E2	E1	E0

E5	E4	E3	E2	E1	E0	Ra/Rb Ratio
0	0	0	0	0	0	Small ↓ Large
0	0	0	0	0	1	
0	0	0	0	1	0	
⋮	⋮	⋮	⋮	⋮	⋮	
1	1	1	1	0	1	
1	1	1	1	1	0	
1	1	1	1	1	1	

Reset Function

Initializing by internal Reset circuit

An internal reset circuit automatically initializes the ST8009 when software reset has active.

The following instructions are executed during the initialization.

1. Interface control selection

   FR: 0

   LP: 0

   PS: 1

2. LCD Duty selection

   Default the segment mode (96 segments) is selected.

3. LCD Bias Set

   Default the 1/4 bias is selected.

4. Power Controller Set

   Default all the power circuit (booster, regulator and follower) will be turned off.

5. Booster Frequency Set

   Default volume is 1 0 0

6. V0 Voltage Regulator Internal Resistor Ratio Set

   Default volume is 1 0 0

7. Electronic Volume Register Set

   Default volume is 1 0 0 0 0 0

BSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	VDD	VDD	2.5~5.5	V	1,2
	VRS	VRS	5.0~+16		
Supply voltage (2)	V1	V1	VDD-10~ VDD+0.3	V	
	V2	V2	VDD-10~ VDD+0.3		
	V3	V3	-0.3~VSS+10	V	
	V4	V4	-0.3~VSS+10	V	
Input voltage	VI	D14-DI0, XCK, FR, EIO1, EIO2, XDISPOFF	-0.3 to VDD+0.3	V	
Storage temperature	TSTG		-45 to +125	°C	

NOTES:

1. TA = +25 °C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	VDD	VDD	+2.5		+5.5	V	1, 2
Supply voltage (2)	V0	V0	+5.0		+16.0	V	
Operating temperature	TOPR		-20		+85	°C	

NOTES:

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. Ensure that voltages are set such that V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧VSS.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Segment Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 5.0 to +15.0 V, T_{OPR} = -20 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_7-DI_0, XCK, FR, EIO_1,			$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}		EIO_2,XDISPOFF	$0.8V_{DD}$			V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	$V_I = V_{SS}$	DI_7-DI_0, XCK, LP, FR,			-10	μA	
	I_{LIH}	$V_I = V_{DD}$	EIO_1, EIO_2,XDISPOFF			+10	μA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0 = 30 V	$COMSEG_0$-$COMSEG_{95}$		1.0	1.5	kΩ	
Standby current	I_{STB}		V_{SS}			50	μA	1
Supply current (1) (Non-selection)	I_{DD1}		V_{DD}			2.0	mA	2
Supply current (2) (Selection)	I_{DD2}		V_{DD}			7.0	mA	3
Supply current (3)	I_0		V_0, V_0			0.9	mA	4

NOTES:

1. V_{DD} = +5.0 V, V_0 = +16.0 V, Vi = V_{SS}.
2. V_{DD} = +5.0 V, V_0 = +16.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{DD}. The input data is turned over by data taking clock (4-bit parallel input mode).
3. V_{DD} = +5.0 V, V_0 = +16.0 V, f_{XCK} = 8MHz, f_{LP} = 19.2 kHz, f_{FR} = 80 Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABL E PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_4-DI_0, XCK, FR,			$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}		EIO_1, EIO_2, XDISPOFF	$0.8V_{DD}$			V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	$V_I = V_{SS}$	DI_4-DI_0, XCK, FR, P/S, EIO_1, EIO_2, XDISPOFF			-10.0	μA	
	I_{LIH}	$V_I = V_{DD}$	DI_4-DI_0, FR,XDISPOFF			+10.0	μA	
Input pull-down current	I_{PD}	$V_I = V_{DD}$	XCK, EIO_1, EIO_2			100	μA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$=0.5V, V_0 = 16V	$COMSEG_0$-$COMSEG_{95}$		1.0	1.5	kΩ	
Standby current	I_{SPD}		V_{SS}			50	μA	1
Supply current (1)	I_{DD}		V_{DD}			80	μA	2
Supply current (2)	I_0		V_O			130	μA	2

NOTES:

1. V_{DD} = +5.0 V, V_0 = +30.0 V, V_I = V_{SS}
2. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{LP} =19.2 kHz, f_{FR} = 80 Hz, 1/96 duty operation, no-load.

AC Characteristics

(Segment Mode 1) (V_{SS} = 0 V, V_{DD} = +2.5 to +3.0 V, V_0 = + 5.0 to +16.0 V, T_{OPR} = -20 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	tWCK	tR,tF ≤ 11ns	125			ns	1
Shift clock "H" pulse width	tWCKH		51			ns	
Shift clock "L" pulse width	tWCKL		51			ns	
Data setup time	tDS		30			ns	
Data hold time	tDH		40			ns	
Latch pulse "H" pulse width	tWLPH		51			ns	
Shift clock rise to latch pulse rise time	tLD		0			ns	
Shift clock fall to latch pulse fall time	tSL		51			ns	
Latch pulse rise to shift clock rise time	tLS		51			ns	
Latch pulse fall to shift clock fall time	tLH		51			ns	
Enable setup time	tS		36			ns	
Input signal rise time	tR				50	ns	2
Input signal fall time	tF				50	ns	2
DISPOFF removal time	tSD		100			ns	
DISPOFF "L" pulse width	tWDL		1.2			µs	
Output delay time (1)	tD	CL = 15 pF			78	ns	
Output delay time (2)	tPD1, t PD2	CL = 15 pF			1.2	µs	
Output delay time (3)	t PD3	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2) (V_{SS} = 0 V, V_{DD} = +5.0±0.5 V, V_0 = + 5.0 to +16.0 V, T_{OPR} = -20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	tWCK	tR,tF ≤ 10ns	66			ns	1
Shift clock "H" pulse width	tWCKH		23			ns	
Shift clock "L" pulse width	tWCKL		23			ns	
Data setup time	tDS		15			ns	
Data hold time	tDH		23			ns	
Latch pulse "H" pulse width	tWLPH		30			ns	
Shift clock rise to latch pulse rise time	tLD		0			ns	
Shift clock fall to latch pulse fall time	tSL		50			ns	
Latch pulse rise to shift clock rise time	tLS		30			ns	
Latch pulse fall to shift clock fall time	tLH		30			ns	
Enable setup time	tS		15			ns	
Input signal rise time	tR				50	ns	2
Input signal fall time	tF				50	ns	2
DISPOFF removal time	tSD		100			ns	
DISPOFF "L" pulse width	tWDL		1.2			µs	
Output delay time (1)	tD	CL = 15 pF			41	ns	
Output delay time (2)	tPD1, t PD2	CL = 15 pF			1.2	µs	
Output delay time (3)	t PD3	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 3) (V_{SS} = 0 V, V_{DD} = +3.0 to +4.5 V, V_0 = + 5.0 to +16.0 V, T_{OPR} = -20 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

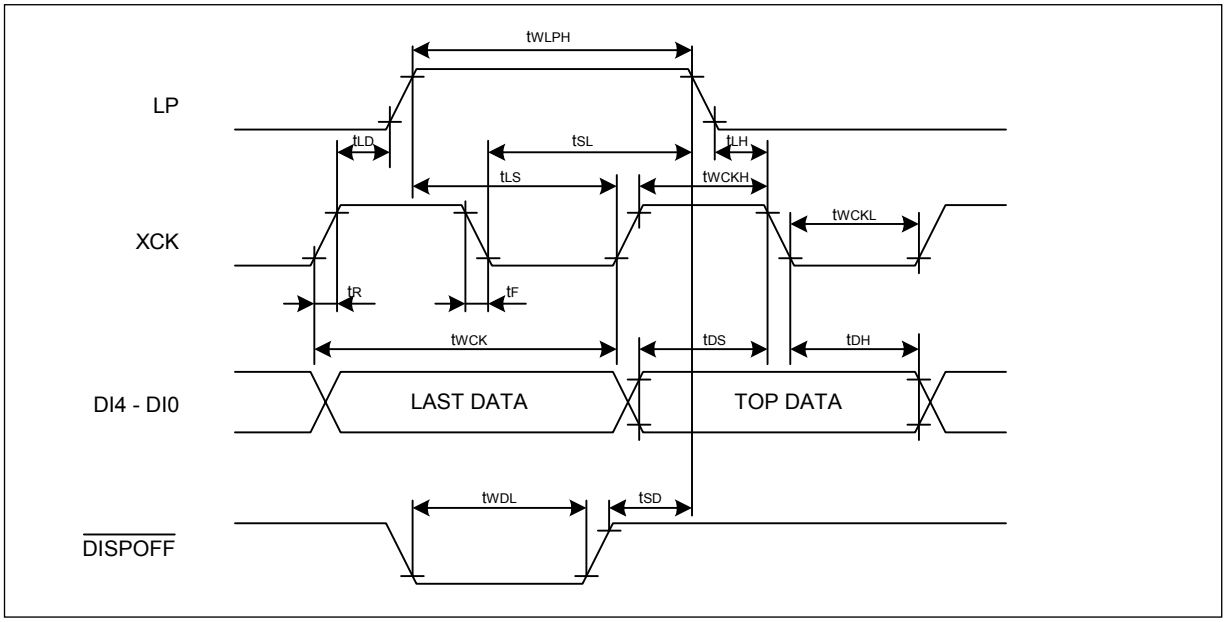
NOTES:

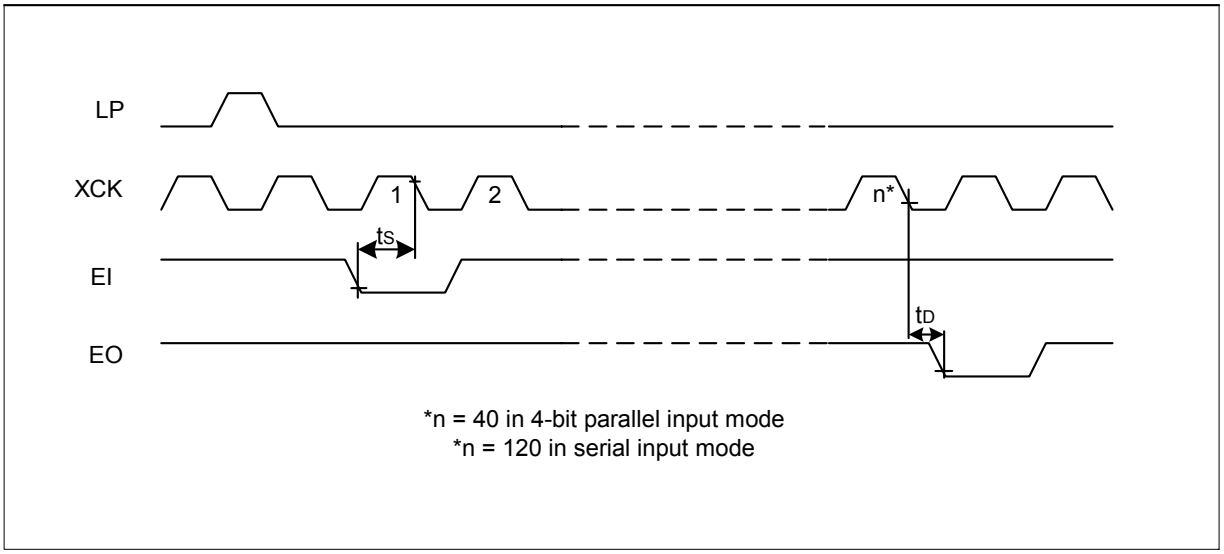
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 5.0 to +16.0 V, T_{OPR} = -20 10+85 °C)

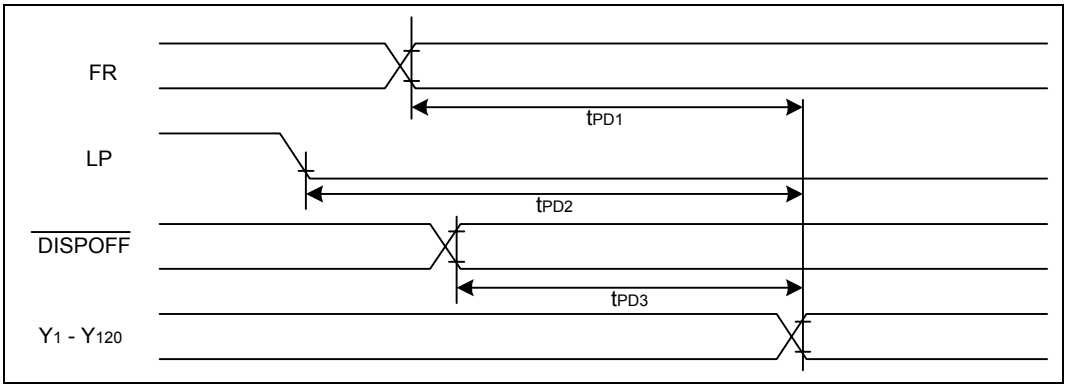
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Shift clock period	t_{WLP}	t_R, t_F 20ns	250			ns
Shift clock “H” pulse width	t_{WLPH}	V_{DD}=5± 0.5V V_{DD}=2.5~4.5V	15 30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF “L” pulse width	t_{WDL}		1.2			us
Output delay time (1)	t_{DL}	CL=10pF			200	ns
Output delay time (2)	t_{PD1},t_{PD2}	CL=10pF			1.2	us
Output delay time (3)	t_{PD3}	CL=10pF			1.2	us

Timing Chart of Segment Mode





*n = 40 in 4-bit parallel input mode
*n = 120 in serial input mode

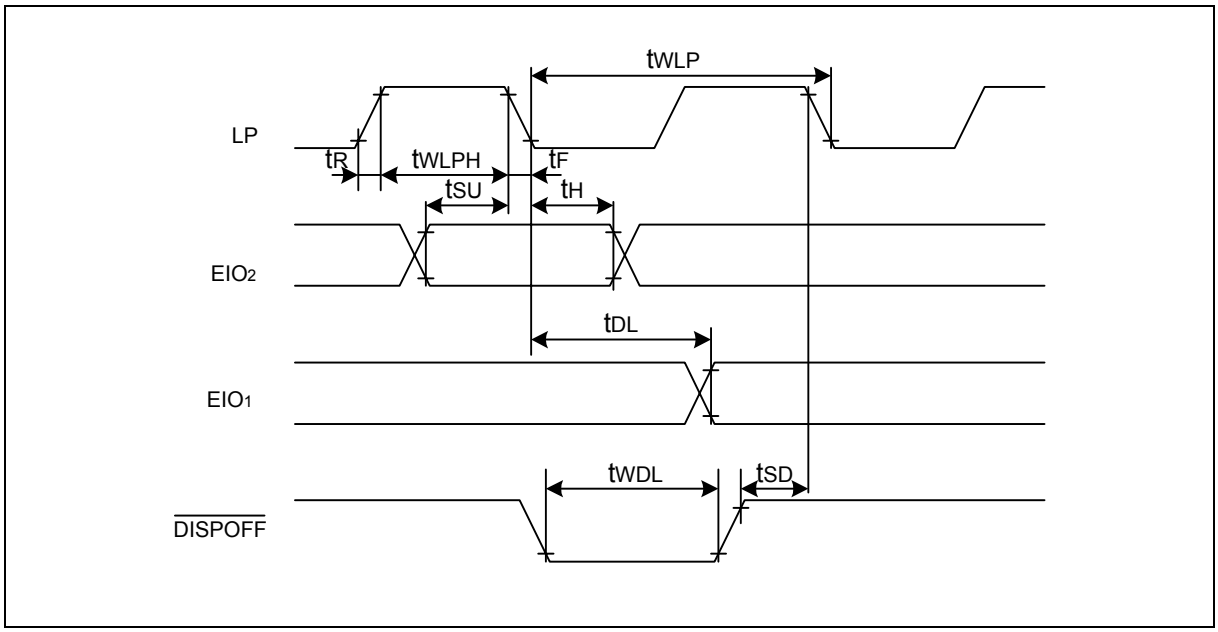


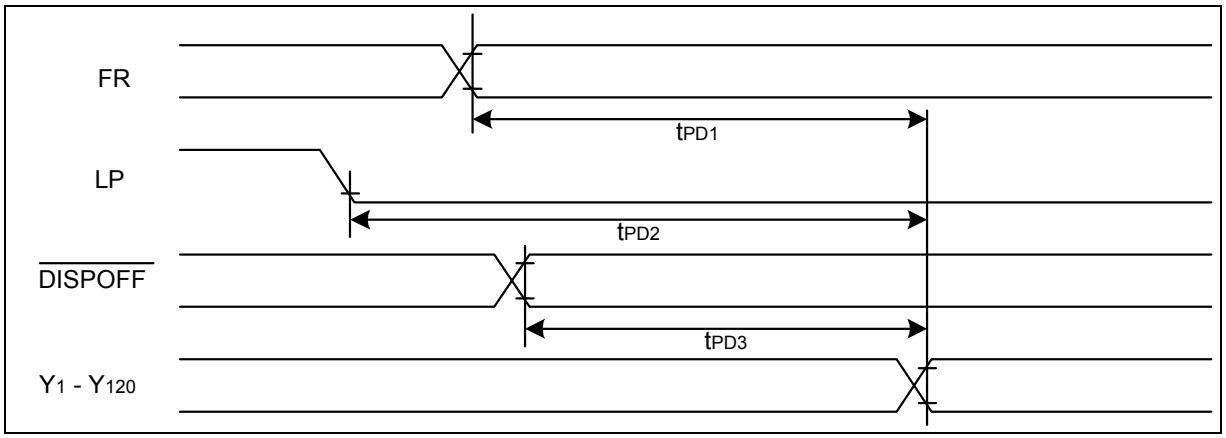
Timing Characteristics (3)

(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +5.0 to +16.0 V, T_{OPR} = -20 to +85° C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	t_R,t_F ≤ 20ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD} = +5.0± 0.5V	15			ns
		V_{DD} = +2.5+ 4.5V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF "L" pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_{DL}	CL = 15 pF			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs

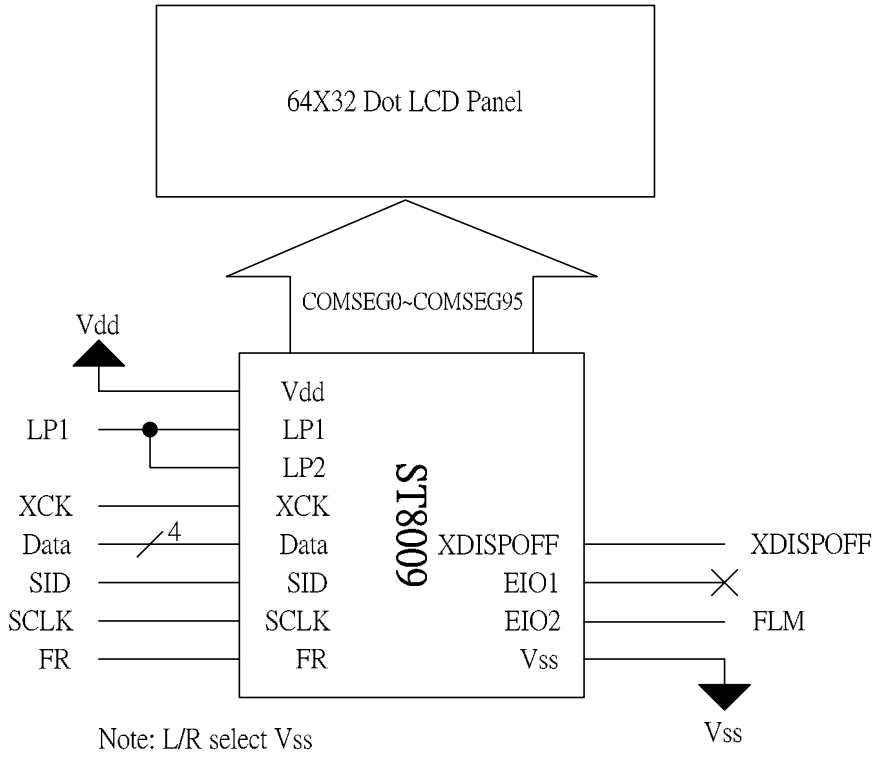
Timing Chart of Common Mode



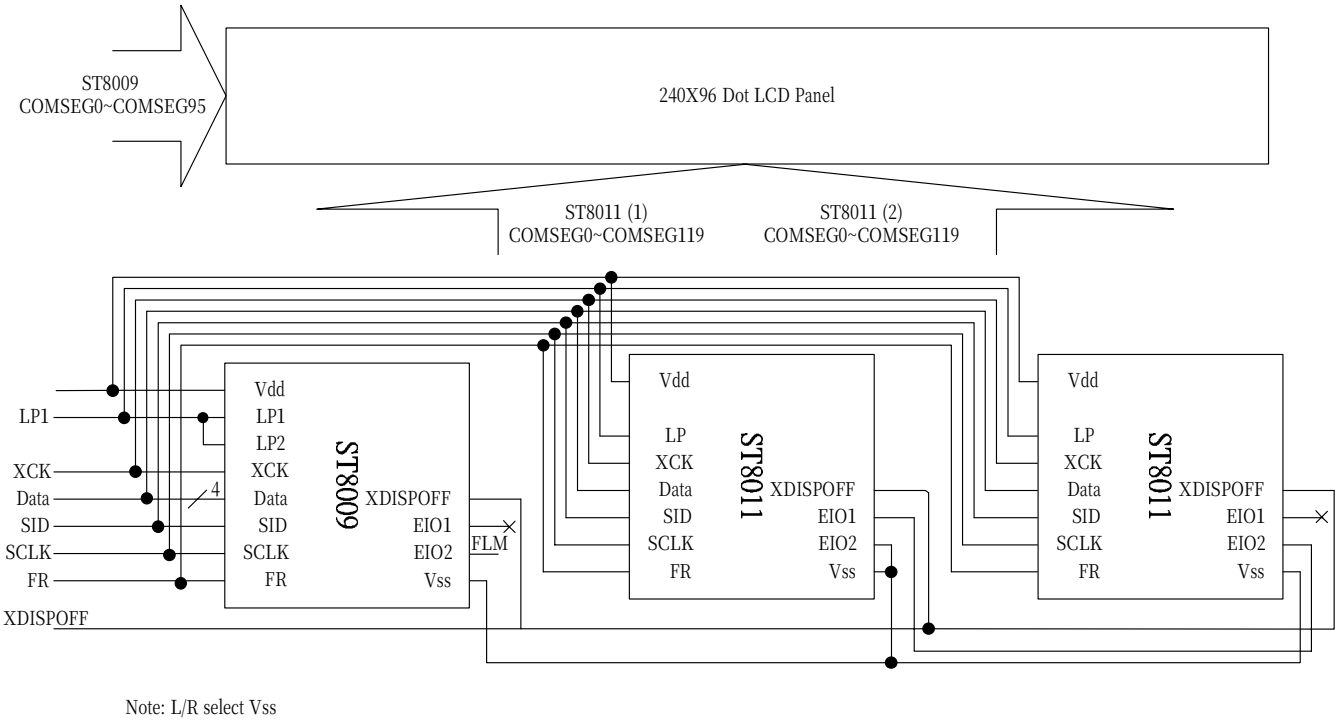

FR
LP
DISPOFF
Y1 - Y120
tPD1
tPD2
tPD3

Application Circuit

(a) When only use one ST8009 in mix mode (64X32)

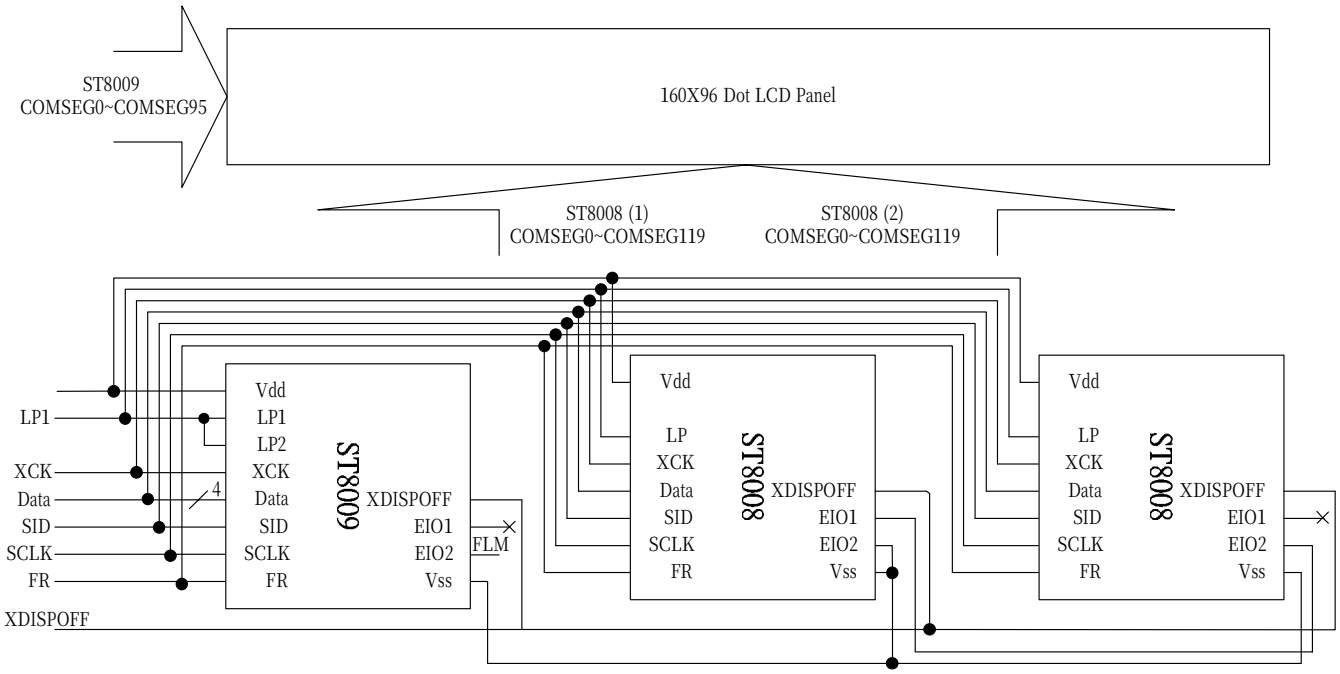


(b) When use one ST8009 and two ST8011 (240X96)



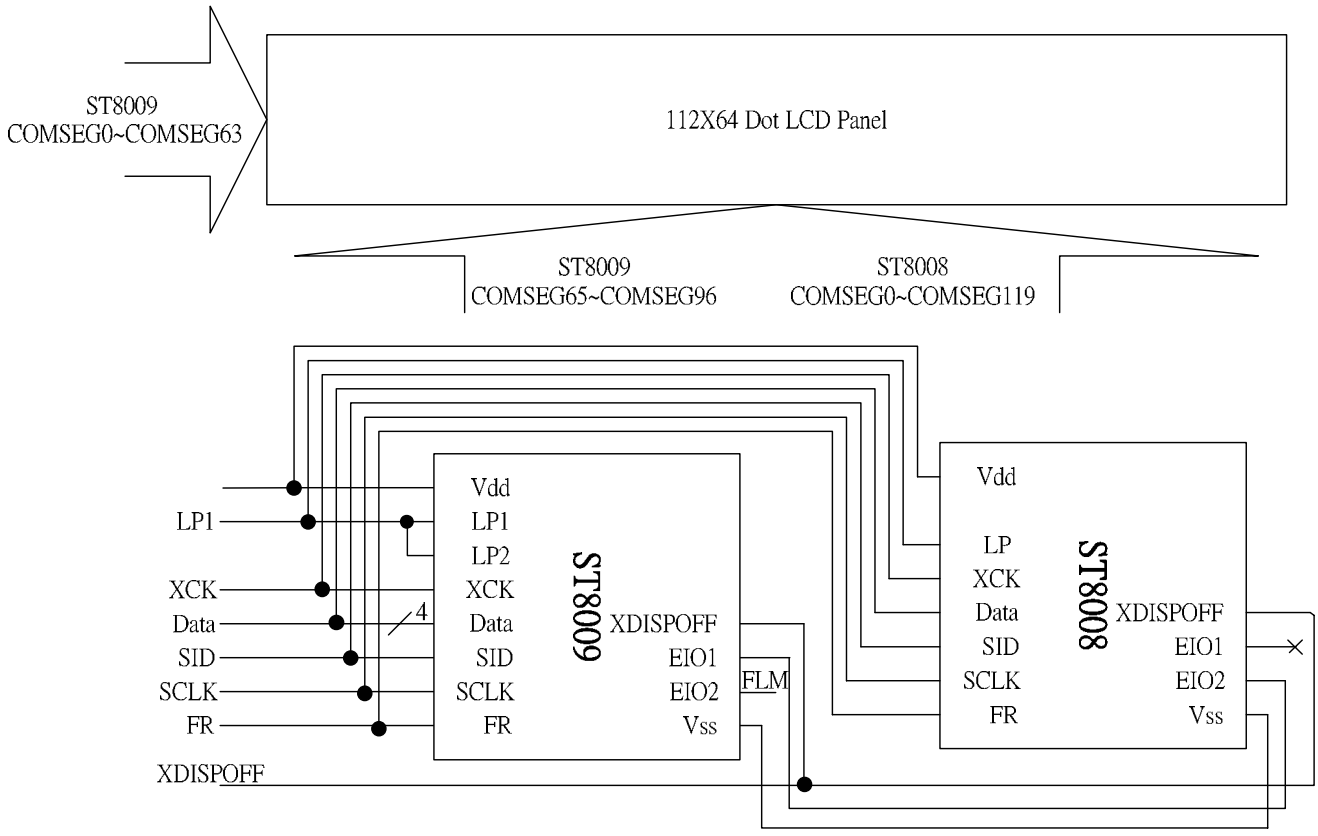
Note: L/R select Vss

(c) When use one ST8009 and two ST8008 (160X96)



Note: L/R select Vss

(d) When use one ST8009 and one ST8008 (112X64)



Note: L/R select Vss

ST8009 Serial Specification Revision History

ST8009 Serial Specification Revision History		
Version	**Date**	**Description**
0.0	**2003/12/25**	**Preliminary version**