SS1103C
Single-Chip Spread Spectrum Processor
for
Digital Cordless Phone

External Specification

PRELIMINARY (V 1.1)

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1. General

The SS1103C is a highly integrated chip for Digital Cordless Phones. The chip performs Direct Sequence Spread Spectrum modulation/demodulation, voice modem functions, and user interface control functions. A baseband spread spectrum modem, a controller, I/O interfaces, and a voice module are implemented into a single chip. The device performs all protocol, data formatting, spread spectrum, audio processing and peripheral functions for a DCP in conformance with FCC regulations Part 15. The device is common for both base station and handset.

2. Main Features

2.1. System Controller Functions

- 8051 Compatible 8-bit CPU
- Programmable divider of the Master Clock frequency
- 32KHz oscillator for sleep mode
- On-chip 16K bytes ROM and 512 bytes RAM
- Serial Peripheral Interface (SPI)
- Asynchronous Serial Interface (UART)
- Serial I/O
- Watch-Dog/Sleep Timer
- General Purpose Timer
- Time Base Timer
- Two External Interrupts
- Power-on Reset

2.2. Peripheral Controller Functions

- SST Baseband Module control
- 4 LED outputs
- Keypad interface
- Battery Low Detect
- Pulse/DTMF Dialing
- Flash Control
- Memory Redial
- Mute Control
- Voice Module Control

2.3. Baseband Module

- High Frequency Oscillator
- Direct Sequence Spread Spectrum Transceiver

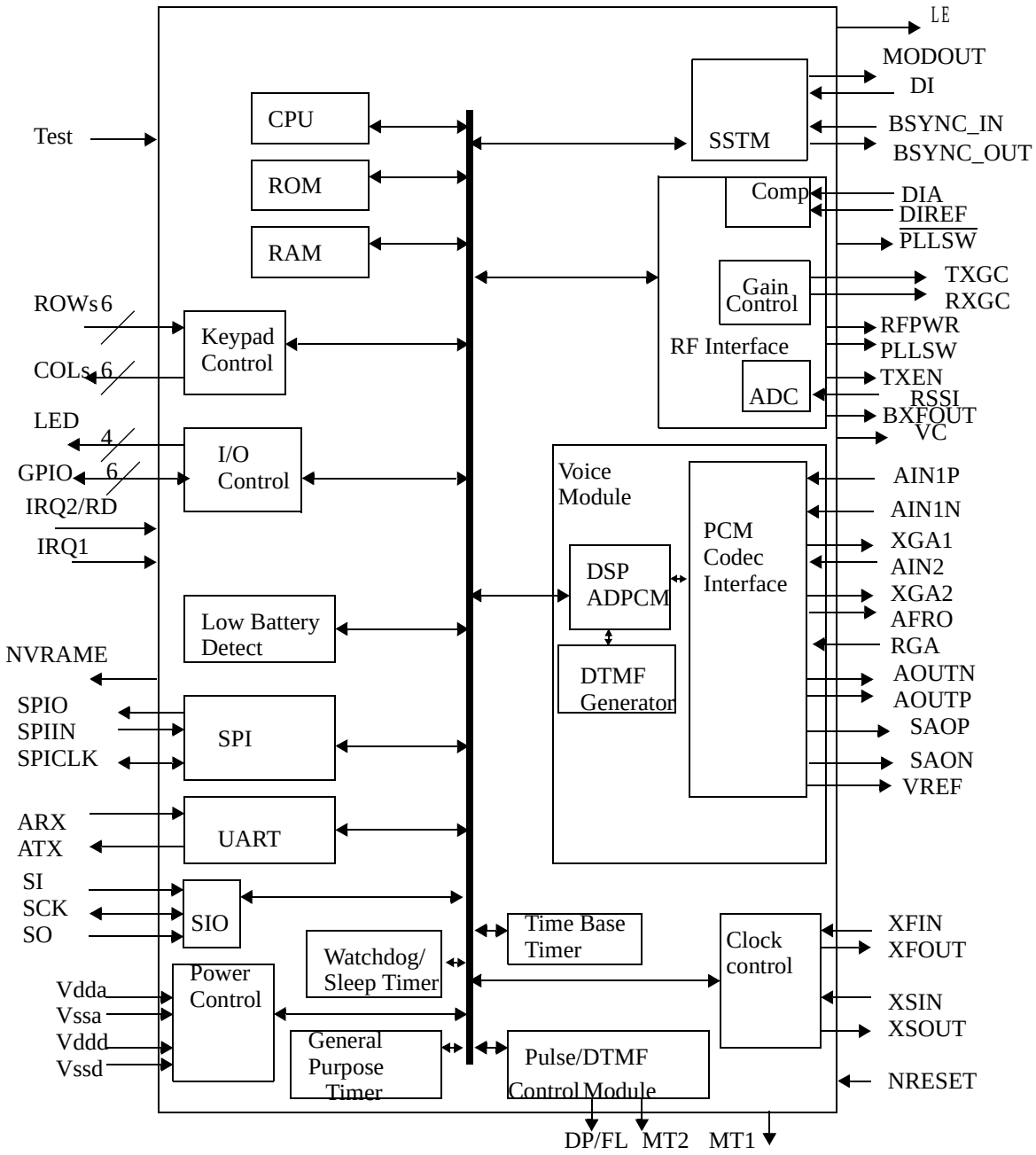
- 3-bit/symbol Baseband Modulation
- Support for MSK
- Time -Division Duplexing (TDD) control
- Processing Gain - 10dB
- Signal Quality Indicator
- Data scrambler for spectral whitening and added security
- ADPCM Voice Module Interface
- Voice Module Frame and Clock Generator
- Transmit and receive FIFO (30 bytes each)
- Low speed signaling channel

2.4. RF Device Interface

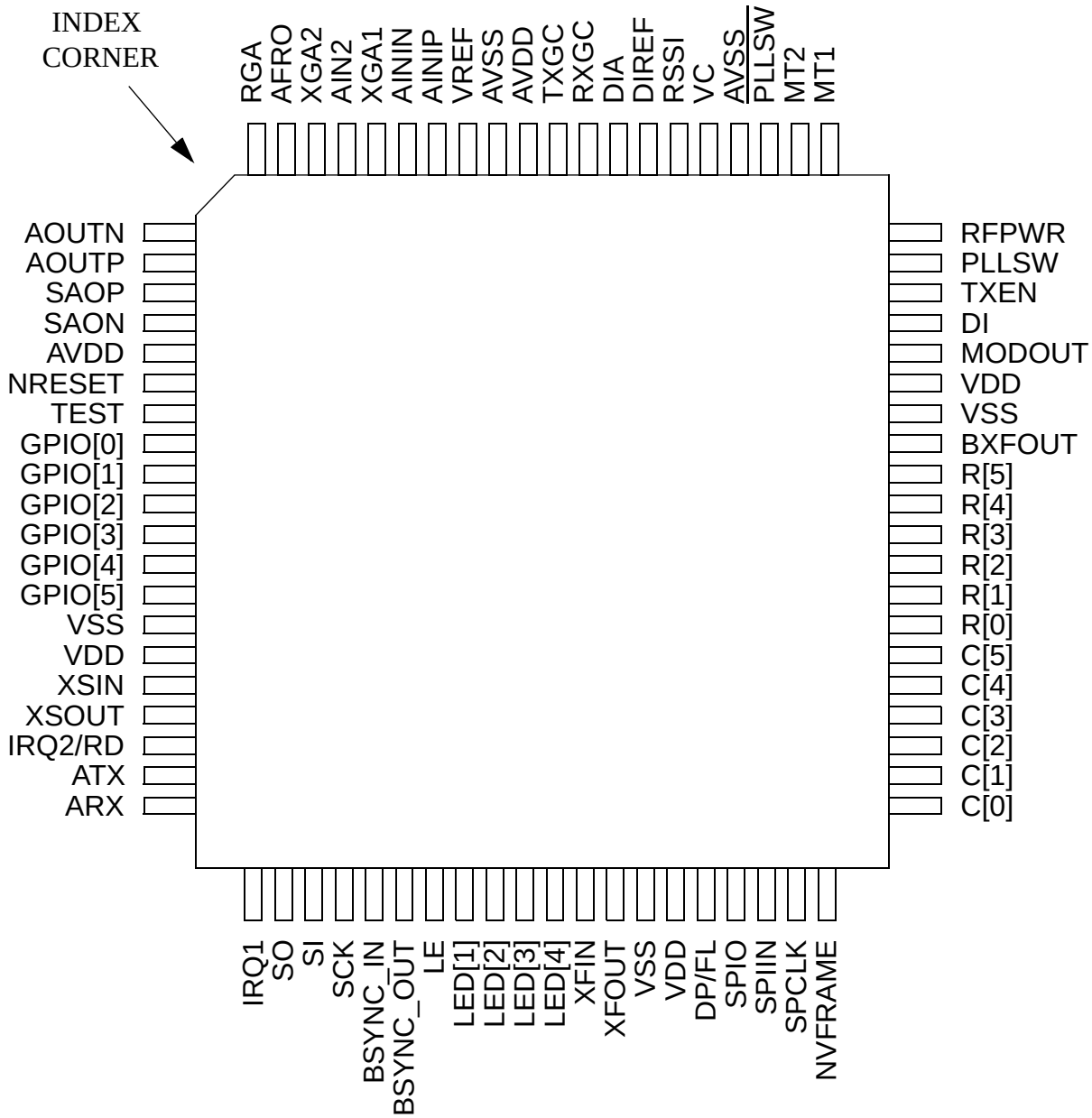
- TX/RX Switch Control
- Power Control
- Synthesizer Control
- RSSI A/D Converter
- Transmit and Receive Gain Control DAC
- Buffered Master Clock Output
- Received Analog Data Signal Comparator/Slicer

2.5. Voice Module

- ADPCM Transcoder ITU G.726
- PCM Codec-Filter ITU G.711
- Tone/DTMF Generation
- Microphone amplifier
- Sounder Driver
- Voice Activity Detection and Control
- Error Detection and Control


LE
MODOUT
DI
BSYNC_IN
BSYNC_OUT
Test
CPU
ROM
RAM
SSTM
Comp
DIA
DIREF
PLLSW
Gain Control
TXGC
RXGC
RFPWR
PLLSW
TXEN
RSSI
BXFOUT
VC
RF Interface
ADC
ROWs 6
Keypad Control
COLs 6
LED 4
GPIO 6
I/O Control
IRQ2/RD
IRQ1
Voice Module
DSP ADPCM
DTMF Generator
PCM Codec Interface
AIN1P
AIN1N
XGA1
AIN2
XGA2
AFRO
RGA
AOUTN
AOUTP
SAOP
SAON
VREF
Low Battery Detect
NVRAME
SPIO
SPIIN
SPICLK
SPI
ARX
ATX
UART
SI
SCK
SO
SIO
Time Base Timer
Clock control
XFIN
XFOUT
XSIN
XSOUT
Watchdog/ Sleep Timer
Power Control
Vdda
Vssa
Vddd
Vssd
General Purpose Timer
Pulse/DTMF Control Module
NRESET
DP/FL
MT2
MT1

MQFP


INDEX
CORNER
RGA
AFRO
XGA2
AIN2
XGA1
AININ
AINIP
VREF
AVSS
AVDD
TXGC
RXGC
DIA
DIREF
RSSI
VC
AVSS
PLLSW
MT2
MT1
AOUTN
AOUTP
SAOP
SAON
AVDD
NRESET
TEST
GPIO[0]
GPIO[1]
GPIO[2]
GPIO[3]
GPIO[4]
GPIO[5]
VSS
VDD
XSIN
XSOUT
IRQ2/RD
ATX
ARX
RFPWR
PLLSW
TXEN
DI
MODOUT
VDD
VSS
BXFOUT
R[5]
R[4]
R[3]
R[2]
R[1]
R[0]
C[5]
C[4]
C[3]
C[2]
C[1]
C[0]
IRQ1
SO
SI
SCK
BSYNC_IN
BSYNC_OUT
LE
LED[1]
LED[2]
LED[3]
LED[4]
XFIN
XFOUT
VSS
VDD
DP/FL
SPIO
SPIIN
SPCLK
NVFRAME

3. Pin Descriptions

3.1. Spread Spectrum Transceiver Module

Pin #	Name	Type	Description
	MODOUT	O	Digital spreaded output data
	DI/GPIO	BI	Digital Data Input from RF module. This input can be used to bypass the DI comparator. Should be configured as DI when the DI comparator is not used, otherwise should be configured as GPIO.
	BSYNC_OUT /GPIO	O	Burst sync pulse. Can be used to sync the burst timing. Can be used as GPIO when internally connected to BSYNC_IN.
	BSYNC_IN /GPIO	I	To be internally looped back to BSYNC_OUT or to an external burst timing source. Can be used as GPIO when internally connected to BSYNC_OUT.

TABLE 1. *Transceiver module pins*

3.2. RF Interface

Pin #	Name	Type	Description
	DIA	I-A	Positive analog data input from RF module to DI comparator (1 bit A/D converter).
	DIREF	I-A	Negative analog data input from RF module to DI comparator.
	RFPWR	O	RF power switch.
	PLLSW	O	Switches the transceiver synthesizer between TX and RX frequencies.
	$\overline{\text{PLLSW}}$/ GPIO	O	Inverted PLLSW signal
	TXEN	O	Transmitter enable. When asserted, can connect the antenna to the transmitter.
	TXGC	O-A	Output of DAC to control the gain circuits in the transmit path. This output is enabled during the transmission.
	RXGC	O-A	Output of DAC to control the gain circuits in the receive path. This output is enabled during the receiving.
	RSSI	I-A	Analog Receive Signal Strength Indication input to RSSI ADC
	VC		RSSI ADC treshold voltage

Pin #	Name	Type	Description
	BXFOUT	O	Buffered High Frequency output
	LE/ GPIO	O	Load Enable. When used as a connection of SIO module to RF Synthesizer, enables the load. This pin is controlled by the application software.

TABLE 2. *RF interface pins*

3.3. Serial Peripheral Interface

Pin #	Name	Type	Description
	SPIO/GPIO	O	Serial out
	SPIIN/GPIO	I	Serial in
	SPICLK/ GPIO	BI	SPI Clock

TABLE 3. *Serial Peripheral Interface pins*

3.4. Serial I/O

Pin #	Name	Type	Description
	SO/GPIO	O	Serial out
	SI/GPIO	I	Serial in
	SCK/GPIO	BI	Clock

3.5. Voice Module

Pin #	Name	Type	Description
	AIN1P	I-A	Differential amplifier non-inverting input
	AIN1N	I-A	Differential amplifier inverting input

Pin #	Name	Type	Description
	XGA1	O-A	Differential amplifier gain control
	AIN2	I-A	Single ended input amplifier inverting input
	XGA2	O-A	Single ended amplifier gain control
	AFRO	O-A	Receive filter output
	RGA	I-A	Receive gain adjustment
	AOUTN	O-A	Differential analog output negative
	AOUTP	O-A	Differential analog output positive
	SAOP	O-A	Sounder differential output positive
	SAON	O-A	Sounder differential output negative
	VREF	O-A	On Chip signal ground. Connect 10mF and 0.1 mF in parallel to Analog Ground

TABLE 4. *Voice interface pins*

3.6. UART

Pin #	Name	Type	Description
	ARX	Ipup	Receive data in
	ATX	Tpup	Transmit data out

TABLE 5. *Base / Hanset control pins*

3.7. Keypad Control

Pin #	Name	Type	Description
	R0/GPIO	Ipup	Row 0 sense input
	R1/GPIO	Ipup	Row 1 sense input
	R2/GPIO	Ipup	Row 2 sense input
	R3/GPIO	Ipup	Row 3 sense input
	R4/GPIO	Ipup	Row 4 sense input
	R5/GPIO	Ipup	Row 5 sense input
	C0/GPIO	BI	Column scan output
	C1/GPIO	BI	Column scan output

Pin #	Name	Type	Description
	C2/GPIO	BI	Column scan output
	C3/GPIO	BI	Column scan output
	C4/GPIO	BI	Column scan output
	C5/GPIO	BI	Column scan output

TABLE 6. *Key pad I/O pins*

3.8. Power Supply

Pin #	Name	Type	Description
	Vssa		Analog Ground
	Vdda		Analog Supply Voltage
	Vddd		Digital Supply Voltage
	VVssd		Digital Ground

TABLE 7. *Power supply pins*

3.9. Miscellaneous

TABLE 8. *Miscellaneous pins*

Pin #	Name	Type	Description
	Nreset	I	Chip Reset
	IRQ1/ GPIO	I	External Interrupt.
	XFIN	I	High Frequency Crystal Input
	XFOUT	O	High Frequency Crystal Output
	XSIN	I	32 KHz Crystal Input
	XSOUT	O	32 KHz Crystal Output
	IRQ2 /RD	I-S	External Interrupt. This pin has a Schmitt trigger circuit and can be used as the Ring Detect input.
	MT2 /GPIO	O	Mute 2 Output Control.

Pin #	Name	Type	Description
	LED1/ GPIO	O	LED Driver Output. 12mA
	LED2 / GPIO	O	LED Driver Output. 12mA
	LED3/ GPIO	O	LED Driver Output. 12mA
	LED4/ GPIO	O	LED Driver Output. 12mA
	DP/FL	O	Dialing Pulse and Flash Output. 12mA
	MT1/ GPIO	O	Mute1 Output Control.
	TEST	I	Test Pin
	NVRAME/ GPIO	O	External RAM Enable Output
	GPIO0	BI	General Purpose I/O
	GPIO1	BI	General Purpose I/O
	GPIO2	BI	General Purpose I/O
	GPIO3	BI	General Purpose I/O
	GPIO4	BI	General Purpose I/O
	GPIO5	BI	General Purpose I/O

4. CPU

High performance CMOS 8-bit CPU with the industry standard 80C51 instruction set.

Extensive boolean processing (single bit logic) capabilities

Arithmetic: 8 bit including multiply and divide

Jumps, 8/16 bit address, conditional and unconditional

Logical separation of program and data memory

Six addressing modes

For a complete description of the CPU with block diagrams, opcode definitions and timing diagrams please refer to the SM82XX cpu core data sheet.

5. Memory Organization

5.1. Data Memory

The SS1103 has separate address space for Program Memory and Data Memory.

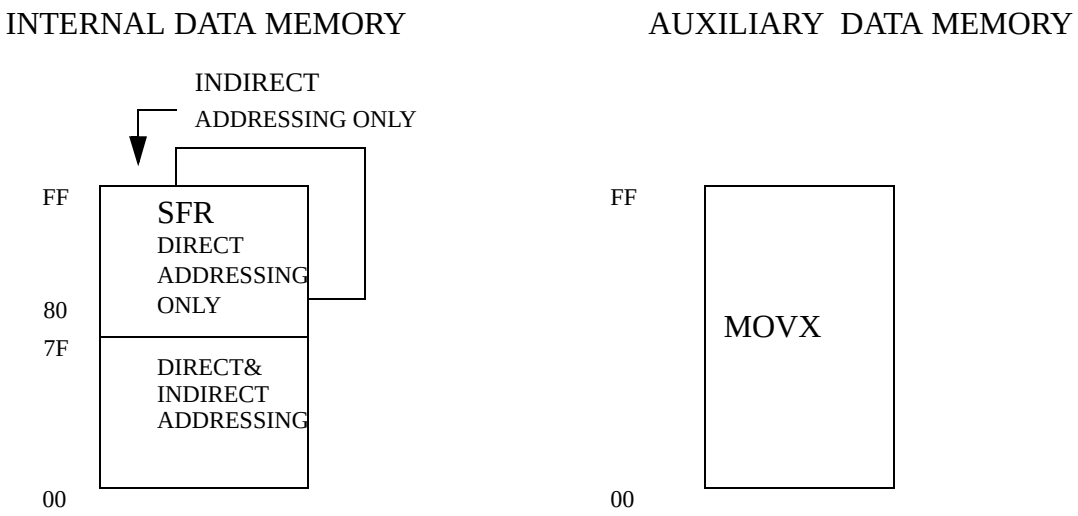


Figure 1. The SS1103 Data Memory

The SS1103 has 512 bytes of onchip data space 256 bytes accessed by MOVX.

By direct and indirect addressing the lowest 128 bytes can be accessed. Then the next 128 bytes are accessed by indirect addressing while direct addressing in this area will access the SFR registers. With the MOVX command there are up to 256 bytes of data memory accessible.

5.2. Program Memory

The SS1103 program memory will fetch 16Kbytes from internal mask ROM.

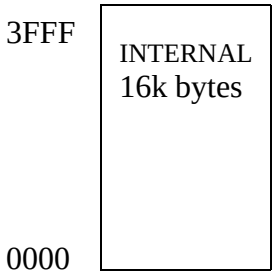


Figure 2. The SS1103 Program Memory

5.3. EXTERNAL MEMORY MODE

The SS1107 is designed to be used in a 80 pin package with internal program and data memory. For test purposes the chip can be put into external memory mode such that external programs and data may be accessed to test the device. This mode is entered by driving the TST pin high with P4.3 and P4.2 low during reset. After reset P4.3 will become the PSEN output and P4.2 will become the ALE output. The remaining pin functions are listed below along with timing diagrams.

PIN	TYPE	FUNCTION
P07-0/AD7-0	I/O	Lower address and data
P27-0/A15-8	OUTPUT	Upper address output
P3.6/NWR	OUTPUT	Data memory write
P3.7/NRD	OUTPUT	Data memory read
P4.3/PSEN	OUTPUT	Program store enable
P4.2/ALE	OUTPUT	Address latch enable

6. Special Function Registers

The SS1103 special function registers (SFR) are accessed with direct memory addressing in the memory space from 80H to FFH. The table below shows the location of each register. The description of the register functions are in the respective peripheral block descriptions and the architectural overview section.

Lo \ Hi	8	9	A	B	C	D	E	F
0	P0	P1	P2	P3	P4	PSW	ACC	B
1	SP	SYSSR	WDCR	TBCR	SSTMCR	DPFCR	CT2CR	SPI1CR
2	DPL	GCMCR	WDCNT	TBCNT	KPDCR	DPFDAT	CT2CNTL	SPI1DAT
3	DPH	TXGCDAT	ADCCR	TBDAT		DPFCNT	CT2CNTH	SPI1SR
4	LBDCR	RXGCDAT	ADCDAT				CT2DATL	SIOCR
5	CMPRCR			UACNT			CT2DATH	SIO-DATAT
6		SREL	XICR0	UACR				VMINTCR
7		PSCR				ISE0	ISE1	ISE2
8		SCON	IE	IP	0:IS 1:UW2 2:TXSW2/ RXSW2 3:PER- RCNT	INT0	INT1	INT2
9		SBUF	P0NOP	P1NOP	P2NOP	P3NOP	P4NOP	
A		PCR	P0IO	P1IO	P2IO	P3IO	P4IO	
B		ZCR	P0RD	P1RD	P2RD	P3RD	P4RD	
C								
D								
E	CI_l	0:LCK 1: 2:TXSW3/ RXSW3		0:PNA0 1:PNC0 2:PNE0 3:PNG0	0:PNA1 1:PNC1 2:PNE1 3:PNG1	0:PNA2 1:PNC2 2:PNE2 3:PNG2	0:PNA3 1:PNC3 2:PNE3 3:PNG3	0: 1:UW1 2.TXSW1/ RXSW1 3:NSVAL
F	0: CIH 1: UW0		0:SN	0:PNB0 1:PND0	0:PNB1 1:PND1	0:PNB2 1:PND2	0:PNB3 1:PND3	MSIZ

The SFR register definitions are described within each peripheral block description and the general CPU registers SP, DPTR, PSW, ACC, B, and MSIZ are described below.

The underlined names are the registers for the CPU and the dashed lines are for registers used in standard 8051 devices not used in the SS1103 microcontroller.

6.1. Stack Pointer (SP)

The SP register contains the stack pointer. The stack pointer is used to load the program counter into memory during LCALL and ACALL instructions, and is used to retrieve the program counter from memory in RET and RETI instructions. The stack may also be saved or loaded using PUSH and POP instructions, which also increment and decrement the stack pointer. The stack pointer points to the top location of the stack. On reset the stack pointer is set to 07 hex.

6.2. Data Pointer (DPTR)

The Data Pointer (DPTR) is 16 bits in size, and consists of two registers, the Data Pointer High byte (DPH), and the Data Pointer Low byte (DPL). Two 16 bit operations are possible on this register, they are load immediate and increment. This register is used for 16 bit address external memory accesses, for offset code byte fetches, and for offset program jumps. On reset the value of this register is 0000 hex.

6.3. Program Status Word (PSW)

This register contains status information resulting from CPU and ALU operation. The bit definitions are given below:

PSW.7 CY. ALU carry flag.

PSW.6 AC. ALU auxiliary carry flag.

PSW.5 F0. General purpose user definable flag.

PSW.4 RS1. Register bank select bit 1.

PSW.3 RS0. Register bank select bit 0.

PSW.2 OV. ALU overflow flag.

PSW.1 F1. User definable flag.

PSW.0 P. Parity flag. Set each instruction cycle to indicate odd/even parity in the accumulator.

The register bank select bits operate as follows.

RS1	RS0	Register Bank Select

0	0	RB0. Registers from 00 - 07 hex.
0	1	RB1. Registers from 08 - 0F hex.
1	0	RB2. Registers from 10 - 17 hex.
1	1	RB3. Registers from 18 - 1F hex.

On reset this register returns 00 hex.

6.4. Accumulator (ACC)

This register provides one of the operands for most ALU operations. In the instruction table it is denoted as “A”.

On reset this register returns 00 hex.

6.5. B Register (B)

This register provides the second operand for multiply or divide instructions. Otherwise it may be used as a scratch pad register.

On reset this register returns 00 hex.

6.6. Memory Size Register (MSIZ)

The purpose of this register is to define the amount of available internal program memory. The amount available is:

(MSIZ + 1) $\times$ 256. On reset this register returns 3F hex or 16K of internal program memory.

256 bytes standard RAM and 256 bytes of additional on-chip data memory accessible by the MOVX command (XRAM). This makes a total of 512 bytes of on-chip data RAM.

7. Port Definition

7.1. Overview

After reset the pins should be configured as they are shown by their names. The pins which can be reconfigured should be reconfigured by application software.

In the SS1103, there are two groups of ports, Port-0 to 3, Port-4. Each port group has diferent configuration. Thus, user should carefully read port specification.

The output drivers of Port-0 and 2, and the input buffer of Port-0 may be used in accesses to external memory. In this application, Port-0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port-2 outputs the high byte of the external memory address when the address is 16-bits wide. Otherwise the Port-2 pins continue to emit the P2 SFR content.

The Port-1 pins and Port-3 pins are multifunctional. They are not only port pins, but also serve the functions of various special features as listed below:

P0.7	MT2		P1.7	SPICK
P0.6	MT1		P1.6	SPIIN
P0.5	GPIO5		P1.5	SPIO
P0.4	GPIO4		P1.4	DI
P0.3	GPIO3		P1.3	LED4
P0.2	GPIO2		P1.2	LED3
P0.1	GPIO1		P1.1	LED2
P0.0	GPIO0		P1.0	LED1
P2.7	C5		P3.7	BSYNC_OUT
P2.6	C4		P3.6	BSYNC_IN
P2.5	C3		P3.5	SCK
P2.4	C2		P3.4	SI
P2.3	C1		P3.3	SO
P2.2	C0		P3.2	IRQ1
P2.1	NVFRAME		P3.1	ARX
P2.0	LE		P3.0	ATX

P4.6	PLLSWB			
P4.5	R5			
P4.4	R4			
P4.3	R3			
P4.2	R2			
P4.1	R1			
P4.0	R0			

The alternate functions for NWR, NRD can only be activated if the corresponding port bit latch (P3.6, P3.7) in the port SFR contains a 1 (high, initial value). Otherwise the port pin is stuck at 0 (low).

7.2. Read-Modify-Write Feature

Some instructions, that read a port (Port-0 to 3 only), read the latch and others read pin. The instructions that read the latch rather than the pin are the ones that read a value, possibly change it, and then rewrite it to the latch. These are called “read-modify-write” instructions. The instructions listed below are read-modify-write instructions. When the destination operand is a port, or a port bit, these instructions read the latch than the pin:

INSTRUCTIONS	DESCRIPTION
ANL	logical AND, e.g. ANL P0, A
ORL	logical OR, e.g. ORL P1, A
XRL	logical EX-OR, e.g. XRL P2, A
JBC	jump if bit = 1 and clear bit, e.g. JBC P3.0, LABEL
CPL	complement bit, e.g. CPL P3.1
INC	increment, e.g. INC P0
DEC	decrement, e.g. DEC P1
DJNZ	decrment and jump if not zero, e.g. DJNZ P0, LABEL

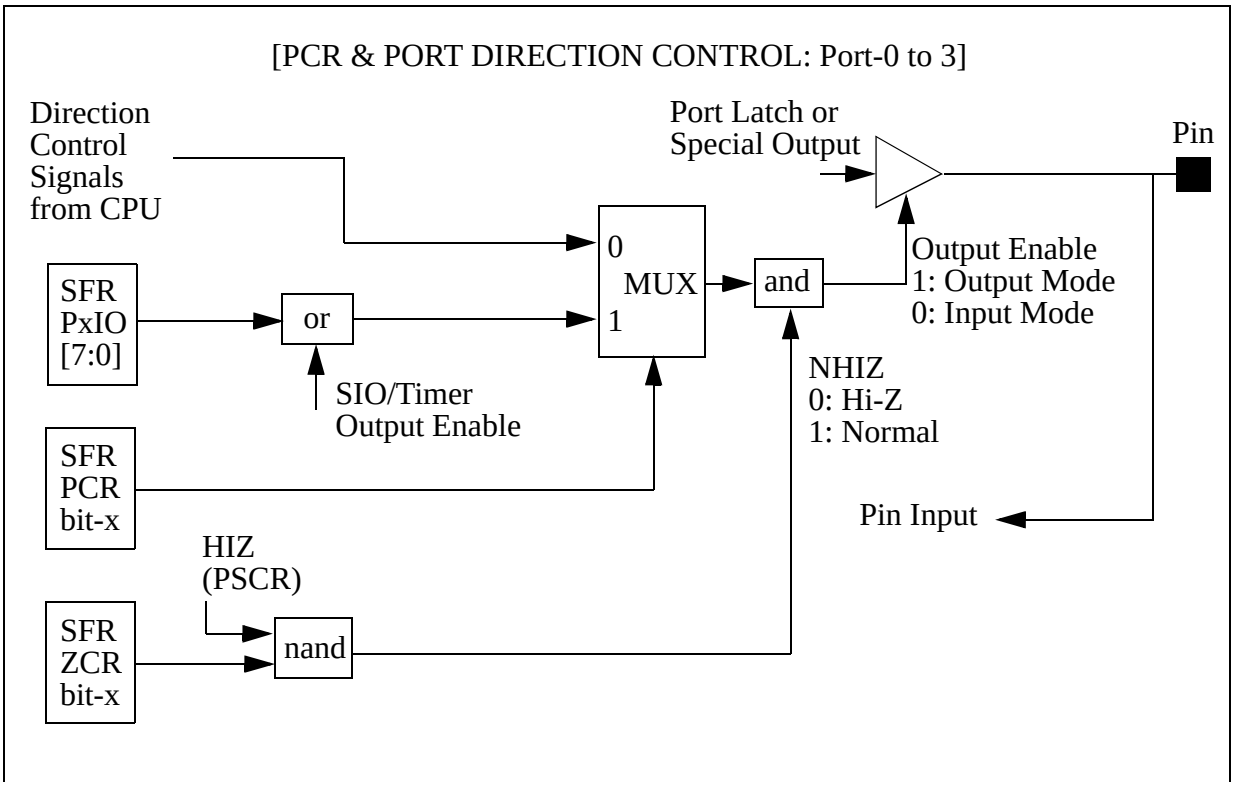
INSTRUCTIONS	DESCRIPTION
MOV PX.Y, C	move carry bit to bit Y of Port-X
CLR PX.Y	clear bit Y of Port-X
SET PX.Y	set bit Y of Port-X

It is not obvious that the last three instructions in this list are read-modify-instructions, but they are. They read the port byte, all 8 bits, modify the addressed bit, then write the new byte back to the latch. The reason that read-modify-write instructions are directed to the latch than the pin is to avoid a possible misinterpretation of the voltage level at the pin. For example, a port bit might be used to drive the base of the transistor. When a 1 is written to the bit, the transistor is turn on. If the CPU then reads the same port bit at the pin rather than the latch, it will read the base voltage of the transistor and interpret it as a 0. Reading the latch rather than the pin will return the correct value of 1.

7.3. PCR (Port Control Register)

[Table: Definition of PCR]

Address	**9AH**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME				**P4LATIN**	**PCR3**	**PCR2**	**PCR1**	**PCR0**
Definition	**Reserved bit**	**Reserved bit**	**Reserved bit**	**Port-4 Input Select 0: Pin In 1:Latch In**	**Port-3 I/O Control bit 0: CPU Control 1: P3IO Control**	**Port-2 I/O Control bit 0: CPU Control 1: P2IO Control**	**Port-1 I/O Control bit 0: CPU Control 1: P1IO Control**	**Port-0 I/O Control bit 0: CPU Control 1: P0IO Control**
Reset Value	**0**	**0**		**0**	**0**	**0**	**0**	**0**
Read/Write by Software	**R**	**R**		**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								



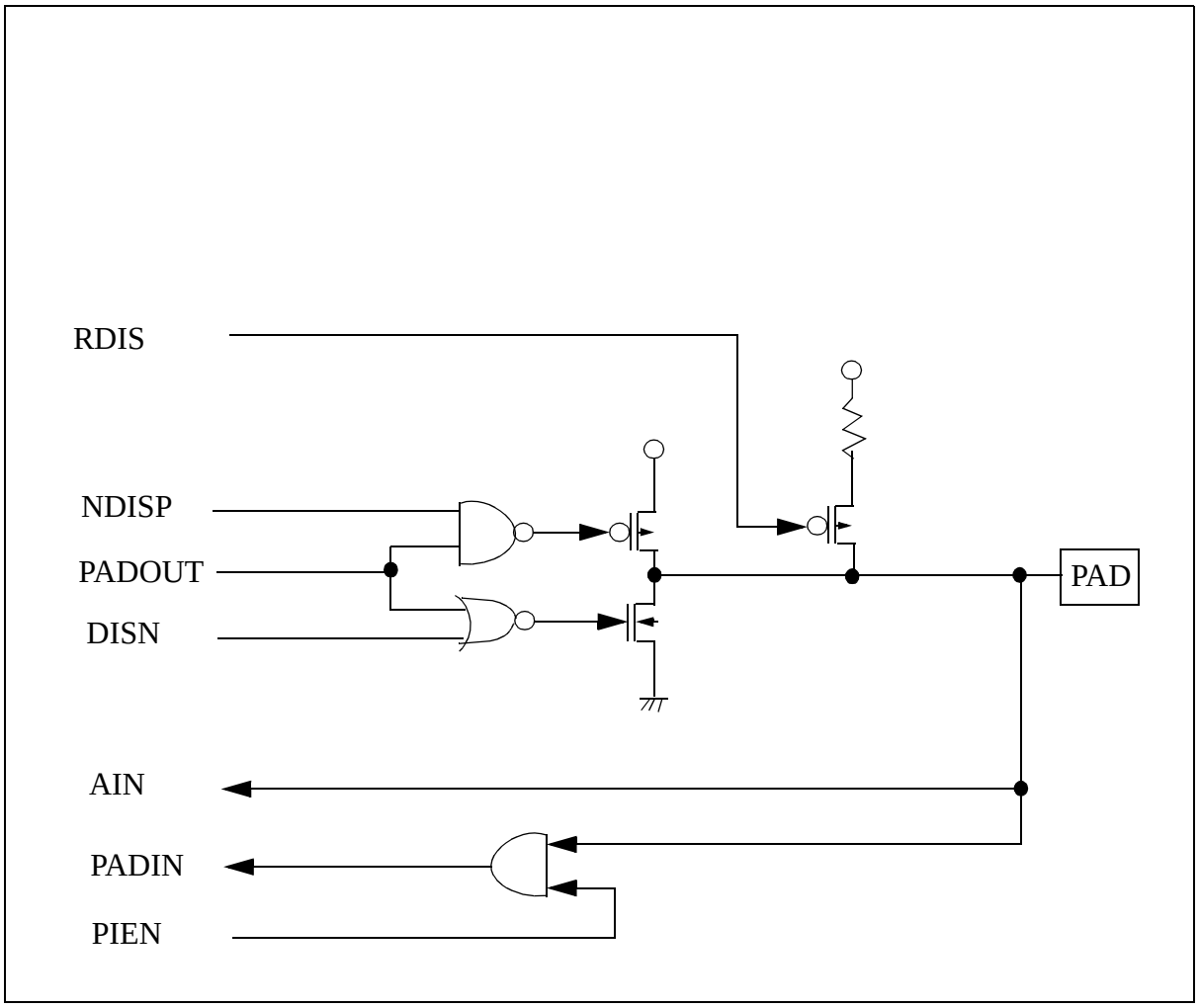
7.4. ZCR (Hi-Z Control Register)

[Table: Definition of ZCR]

Address	9BH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME				ZCR4	ZCR3	ZCR2	ZCR1	ZCR0
Definition	Reserved bit	Reserved bit	Reserved bit	Port-4 Hi-Z Control bit 0: Disable 1: Hi-Z Enable	Port-3 Hi-Z Control bit 0: Disable 1: Hi-Z Enable	Port-2 Hi-Z Control bit 0: Disable 1: Hi-Z Enable	Port-1 Hi-Z Control bit 0: Disable 1: Hi-Z Enable	Port-0 Hi-Z Control bit 0: Disable 1: Hi-Z Enable

Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software	**R**	**R**	**R**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								

7.5. PAD Cell



7.6. P0 (Port-0)

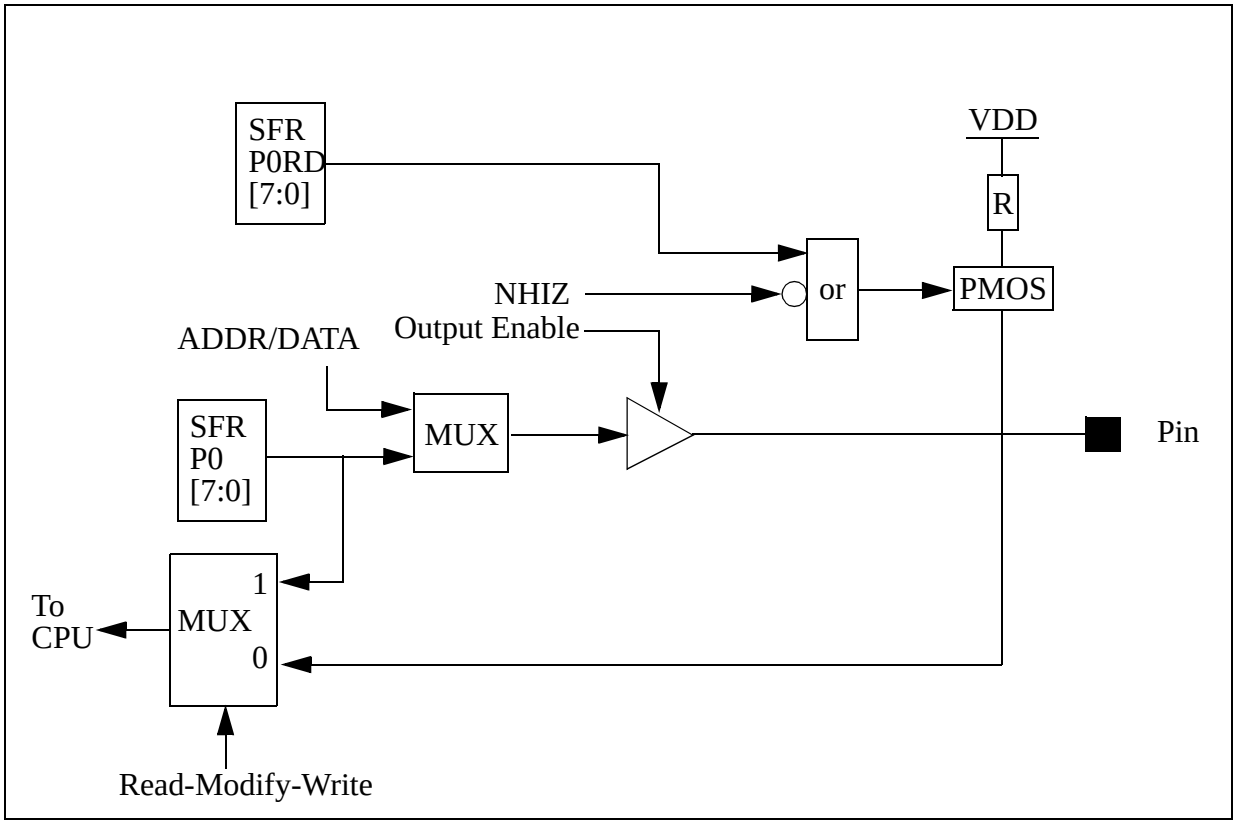
The Pin-0.0 to 0.7 have two functional modes, A/D Mode (Low Address/Data Mode) and Port Mode (Bi-directional Port Mode). Initial Staus is A/D Mode because PCR0 (Port Control Register Bit-0) is 0 (low). In Port Mode, the direction of Port-0 can be decided bit-by-bit. In A/D Mode, writing to Port-0 is prohibited. The read policy in Port Mode follows that described before. Read-Modify-Write instructions read the port latch than the pin.

To use Pin-0.0 to 0.7 as a normal input port, PCR0 should be high. If PCR0 is high, the direction of each Port-0 pin is decided by each P0IO bit. If the P0IO bit-x is high, Port-0.x is output mode. If low, Port-0.x is input mode. Initial status is input mode because P0IO (Port-0 I/O Direction Register) is reset to 00000000B. In input mode, pull-up resistor can be connected by P0RD (Port-0 Resistor Disable Register). If the P0RD bit-x is high, Port-0.x pull-up resistor is disconnected. If low, Port-0.x pull-up resistor is connected. Initial status of P0RD is 11111111B, thus pull-up resistor is disconnected. If ZCR0 (High-Z Control Register Bit-0) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pull-up resistor is disconnected and pin status becomes high impedence.

To use Pin-0.0 to 0.7 as a normal output port, PCR0 should be high. If the P0IO bit-x is high, Port-0.x is output mode. In output mode, pull-up resistor is not automatically disconnected regardless P0RD bit-x. If ZCR0 (High-Z Control Register Bit-0) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pin status becomes high impedence.

To use Pin-0.0 to 0.7 as an A/D input/output port, PCR0 should be low (reset value). If PCR0 is low, the direction of each Port-0 pin is controlled by CPU. In input mode, pull-up resistor can be connected by P0RD (Port-0 Resistor Disable Register). In output mode, pull-up resistor is not automatically disconnected regardless P0RD bit-x. For the A/D Mode, the ZCR0 must be low (reset value) not to support Hi-Z state.

When P0NOPNx = 0, Port-0.x output buffer will be CMOS Push-Pull. But, P0NOPNx = 1, Port-0.x output buffer will become N-channel Open Drain.



[Table: Definition of P0]

Address	80H							
Bit Addr.	87H	86H	85H	84H	83H	82H	81H	80H
BIT	7	6	5	4	3	2	1	0
NAME	P07	P06	P05	P04	P03	P02	P01	P00
Definition	Port-0 Pin or Latch bit-7	Port-0 Pin or Latch bit-6	Port-0 Pin or Latch bit-5	Port-0 Pin or Latch bit-4	Port-0 Pin or Latch bit-3	Port-0 Pin or Latch bit-2	Port-0 Pin or Latch bit-1	Port-0 Pin or Latch bit-0
Reset Value	1	1	1	1	1	1	1	1

Read/Write by Software	**R/W RMW Ins: P07 Latch Read Other Ins: P0.7 Pin Read**	**R/W RMW Ins: P06 Latch Read Other Ins: P0.6 Pin Read**	**R/W RMW Ins: P05 Latch Read Other Ins: P0.5 Pin Read**	**R/W RMW Ins: P04 Latch Read Other Ins: P0.4 Pin Read**	**R/W RMW Ins: P03 Latch Read Other Ins: P0.3 Pin Read**	**R/W RMW Ins: P02 Latch Read Other Ins: P0.2 Pin Read**	**R/W RMW Ins: P01 Latch Read Other Ins: P0.1 Pin Read**	**R/W RMW Ins: P00 Latch Read Other Ins: P0.0 Pin Read**
Write by Hardware								

[Table: Definition of P0IO]

Address	**AAH**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**P0IO7**	**P0IO6**	**P0IO5**	**P0IO4**	**P0IO3**	**P0IO2**	**P0IO1**	**P0IO0**
Definition	**Port-0 I/O Control Register bit-7 0: Input Mode 1: Output Mode**	**Port-0 I/O Control Register bit-6 0: Input Mode 1: Output Mode**	**Port-0 I/O Control Register bit-5 0: Input Mode 1: Output Mode**	**Port-0 I/O Control Register bit-4 0: Input Mode 1: Output Mode**	**Port-0 I/O Control Register bit-3 0: Input Mode 1: Output Mode**	**Port-0 I/O Control Register bit-2 0: Input Mode 1: Output Mode**	**Port-0 I/O Control Register bit-1 0: Input Mode 1: Output Mode**	**Port-0 I/O Control Register bit-0 0: Input Mode 1: Output Mode**
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								

[Table: Definition of P0RD]

Address	**ABH**

Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P0RD7	P0RD6	P0RD5	P0RD4	P0RD3	P0RD2	P0RD1	P0RD0
Definition	Port-0 Resistor Disable Register bit-7 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-6 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-5 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-4 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-3 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-2 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-1 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-0 0: Resistor Enable 1: Disable
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of P0NOPN]

Address	A9H							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P0NOPN7	P0NOPN6	P0NOPN5	P0NOPN4	P0NOPN3	P0NOPN2	P0NOPN1	P0NOPN0
Definition	Port-0 Output Buffer bit-7 0: CMOS Push_Pull 1: N-ch open drain	Port-0 Output Buffer bit-6 0: CMOS Push_Pull 1: N-ch open drain	Port-0 Output Buffer bit-5 0: CMOS Push_Pull 1: N-ch open drain	Port-0 Output Buffer bit-4 0: CMOS Push_Pull 1: N-ch open drain	Port-0 Output Buffer bit-3 0: CMOS Push_Pull 1: N-ch open drain	Port-0 Output Buffer bit-2 0: CMOS Push_Pull 1: N-ch open drain	Port-0 Output Buffer bit-1 0: CMOS Push_Pull 1: N-ch open drain	Port-0 Output Buffer bit-0 0: CMOS Push_Pull 1: N-ch open drain
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

7.7. P2 (Port-2)

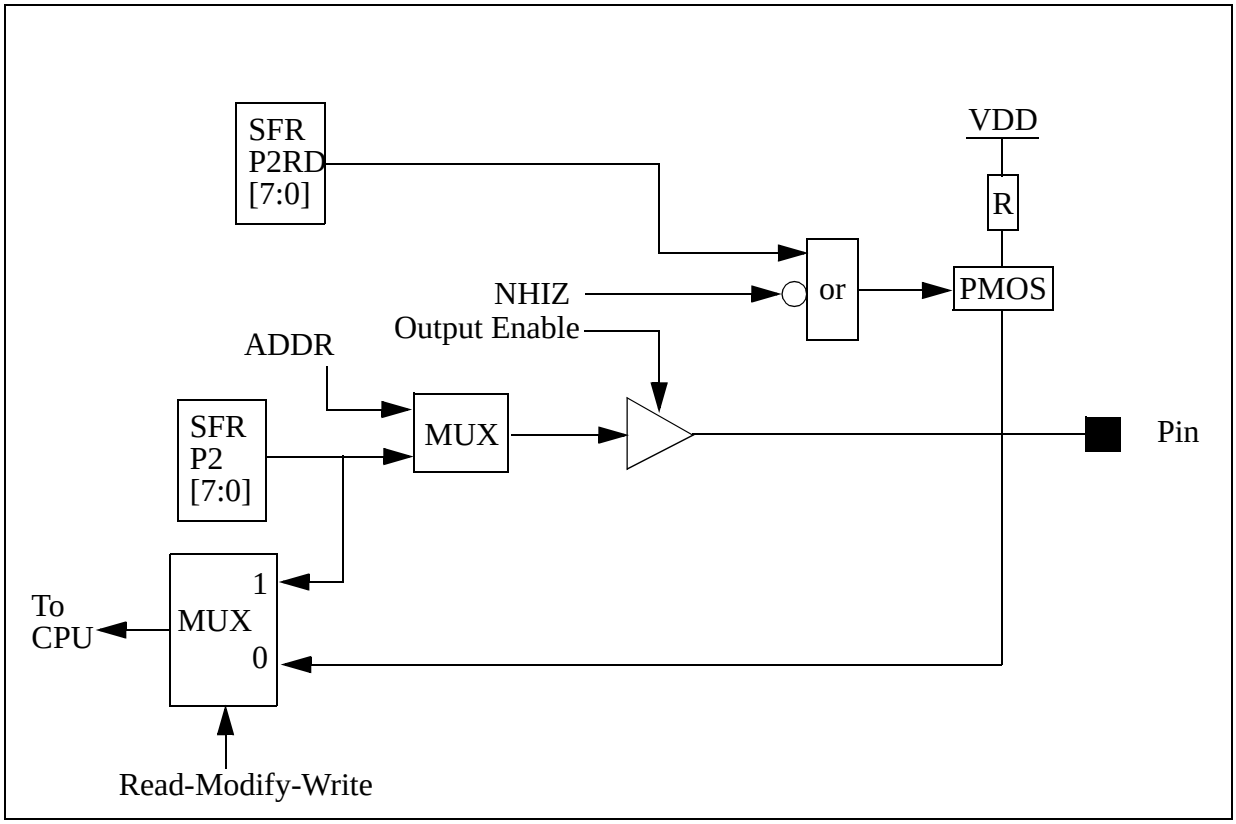
The Pin-2.0 to 2.7 have two functional modes, ADDR Mode (High Address Mode) and Port Mode (Bi-directional Port Mode). Initial Staus is ADDR Mode because PCR2 (Port Control Register Bit-2) is 0 (low). In Port Mode, the direction of Port-2 can be decided bit-by-bit. The read policy in Port Mode follows that described before. Read-Modify-Write instructions read the port latch than the pin.

To use Pin-2.0 to 2.7 as a normal input port, PCR2 should be high. If PCR2 is high, the direction of each Port-2 pin is decided by each P2IO bit. If the P2IO bit-x is high, Port-2.x is output mode. If low, Port-2.x is input mode. Initial status is input mode because P2IO (Port-2 I/O Direction Register) is reset to 00000000B. In input mode, pull-up resistor can be connected by P2RD (Port-2 Resistor Disable Register). If the P2RD bit-x is high, Port-2.x pull-up resistor is disconnected. If low, Port-2.x pull-up resistor is connected. Initial status of P2RD is 11111111B, thus pull-up resistor is disconnected. If ZCR2 (High-Z Control Register Bit-2) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pull-up resistor is disconnected and pin status becomes high impedence.

To use Pin-2.0 to 2.7 as a normal output port, PCR2 should be high. If the P2IO bit-x is high, Port-2.x is output mode. In output mode, pull-up resistor is not automatically disconnected regardless P2RD bit-x. If ZCR2 (High-Z Control Register Bit-2) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pin status becomes high impedence.

To use Pin-2.0 to 2.7 as an ADDR output port, PCR2 should be low (reset value). If PCR2 is low, the direction of each Port-2 pin is controlled by CPU. In output mode, pull-up resistor is not automatically disconnected regardless P2RD bit-x. For the ADDR Mode, the ZCR2 must be low (reset value) not to support Hi-Z state.

When P2NOPNx = 0, Port-2.x output buffer will be CMOS Push-Pull. But, P2NOPNx = 1, Port-2.x output buffer will become N-channel Open Drain.



[Table: Definition of P2]

Address	A0H							
Bit Addr.	A7H	A6H	A5H	A4H	A3H	A2H	A1H	A0H
BIT	7	6	5	4	3	2	1	0
NAME	P27	P26	P25	P24	P23	P22	P21	P20
Definition	Port-2 Pin or Latch bit-7	Port-2 Pin or Latch bit-6	Port-2 Pin or Latch bit-5	Port-2 Pin or Latch bit-4	Port-2 Pin or Latch bit-3	Port-2 Pin or Latch bit-2	Port-2 Pin or Latch bit-1	Port-2 Pin or Latch bit-0
Reset Value	1	1	1	1	1	1	1	1

Read/Write by Software	**R/W RMW Ins: P27 Latch Read Other Ins: P2.7 Pin Read**	**R/W RMW Ins: P26 Latch Read Other Ins: P2.6 Pin Read**	**R/W RMW Ins: P25 Latch Read Other Ins: P2.5 Pin Read**	**R/W RMW Ins: P24 Latch Read Other Ins: P2.4 Pin Read**	**R/W RMW Ins: P23 Latch Read Other Ins: P2.3 Pin Read**	**R/W RMW Ins: P22 Latch Read Other Ins: P2.2 Pin Read**	**R/W RMW Ins: P21 Latch Read Other Ins: P2.1 Pin Read**	**R/W RMW Ins: P20 Latch Read Other Ins: P2.0 Pin Read**
Write by Hardware								

[Table: Definition of P2IO]

Address	**CAH**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**P2IO7**	**P2IO6**	**P2IO5**	**P2IO4**	**P2IO3**	**P2IO2**	**P2IO1**	**P2IO0**
Definition	**Port-2 I/O Control Register bit-7 0: Input Mode 1: Output Mode**	**Port-2 I/O Control Register bit-6 0: Input Mode 1: Output Mode**	**Port-2 I/O Control Register bit-5 0: Input Mode 1: Output Mode**	**Port-2 I/O Control Register bit-4 0: Input Mode 1: Output Mode**	**Port-2 I/O Control Register bit-3 0: Input Mode 1: Output Mode**	**Port-2 I/O Control Register bit-2 0: Input Mode 1: Output Mode**	**Port-2 I/O Control Register bit-1 0: Input Mode 1: Output Mode**	**Port-2 I/O Control Register bit-0 0: Input Mode 1: Output Mode**
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								

[Table: Definition of P2RD]

Address	**CBH**

Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P2RD7	P2RD6	P2RD5	P2RD4	P2RD3	P2RD2	P2RD1	P2RD0
Definition	Port-2 Resistor Disable Register bit-7 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-6 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-5 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-4 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-3 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-2 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-1 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-0 0: Resistor Enable 1: Disable
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

Table: Definition of P2NOPN]

Address	C9H							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P2NOPN7	P2NOPN6	P2NOPN5	P2NOPN4	P2NOPN3	P2NOPN2	P2NOPN1	P2NOPN0
Definition	Port-2 Output Buffer bit-7 0: CMOS Push_Pull 1: N-ch open drain	Port-2 Output Buffer bit-6 0: CMOS Push_Pull 1: N-ch open drain	Port-2 Output Buffer bit-5 0: CMOS Push_Pull 1: N-ch open drain	Port-2 Output Buffer bit-4 0: CMOS Push_Pull 1: N-ch open drain	Port-2 Output Buffer bit-3 0: CMOS Push_Pull 1: N-ch open drain	Port-2 Output Buffer bit-2 0: CMOS Push_Pull 1: N-ch open drain	Port-2 Output Buffer bit-1 0: CMOS Push_Pull 1: N-ch open drain	Port-2 Output Buffer bit-0 0: CMOS Push_Pull 1: N-ch open drain
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

7.8. P1 (Port-1)

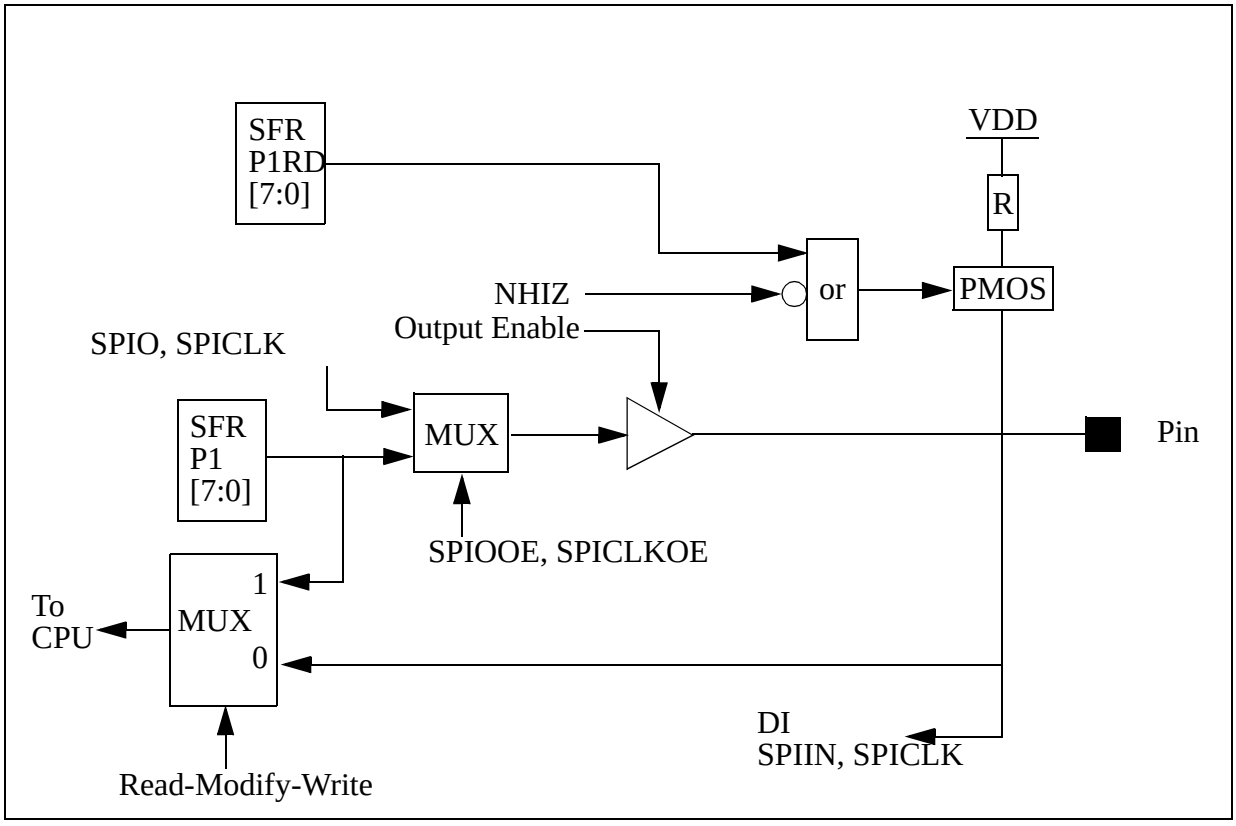
The Pin-1.4 to 1.7 have two functional modes, special output Mode (SPIO, SPICLK) and Port Mode (Bi-directional Port Mode). Initial Staus of PCR1 (Port Control Register Bit-1) is 0 (low). The PCR1 must be set to high for any case. In Port Mode, the direction of Port-1 can be decided bit-by-bit. The read policy in Port Mode follows that described before. Read-Modify-Write instructions read the port latch than the pin.

To use Pin-1.0 to 1.7 as a normal input port, PCR1 should be high. If PCR1 is high, the direction of each Port-1 pin is decided by each P1IO bit. If the P1IO bit-x is high, Port-1.x is output mode. If low, Port-1.x is input mode. Initial status is input mode because P1IO (Port-1 I/O Direction Register) is reset to 00000000B. In input mode, pull-up resistor can be connected by P1RD (Port-1 Resistor Disable Register). If the P1RD bit-x is high, Port-1.x pull-up resistor is disconnected. If low, Port-1.x pull-up resistor is connected. Initial status of P1RD is 11111111B, thus pull-up resistor is disconnected. If ZCR1 (High-Z Control Register Bit-1) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pull-up resistor is disconnected and pin status becomes high impedence. In input mode, P1.4/DI, P1.6/SPIIN, and P1.7/SPICLK can be used DI or SPI input pins.

To use Pin-1.0 to 1.7 as a normal output port, PCR1 should be high. If the P1IO bit-x is high, Port-1.x is output mode. In output mode, pull-up resistor is not automatically disconnected regardless P1RD bit-x. If ZCR1 (High-Z Control Register Bit-1) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pin status becomes high impedence.

To use P1.5/SPIO and P1.7/SPICLK as an SIO output port, PCR1 should be high.

When P1NOPNx = 0, Port-1.x output buffer will be CMOS Push-Pull. But, P1NOPNx = 1, Port-1.x output buffer will become N-channel Open Drain.



[Table: Definition of P1]

Address	90H							
Bit Addr.	97H	96H	95H	94H	93H	92H	91H	90H
BIT	7	6	5	4	3	2	1	0
NAME	P17	P16	P15	P14	P13	P12	P11	P10
Definition	Port-1 Pin or Latch bit-7	Port-1 Pin or Latch bit-6	Port-1 Pin or Latch bit-5	Port-1 Pin or Latch bit-4	Port-1 Pin or Latch bit-3	Port-1 Pin or Latch bit-2	Port-1 Pin or Latch bit-1	Port-1 Pin or Latch bit-0
Reset Value	1	1	1	1	1	1	1	1

Read/Write by Software	**R/W RMW Ins: P17 Latch Read Other Ins: P1.7 Pin Read**	**R/W RMW Ins: P16 Latch Read Other Ins: P1.6 Pin Read**	**R/W RMW Ins: P15 Latch Read Other Ins: P1.5 Pin Read**	**R/W RMW Ins: P14 Latch Read Other Ins: P1.4 Pin Read**	**R/W RMW Ins: P13 Latch Read Other Ins: P1.3 Pin Read**	**R/W RMW Ins: P12 Latch Read Other Ins: P1.2 Pin Read**	**R/W RMW Ins: P11 Latch Read Other Ins: P1.1 Pin Read**	**R/W RMW Ins: P10 Latch Read Other Ins: P1.0 Pin Read**
Write by Hardware								

[Table: Definition of P1IO]

Address	**BAH**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**P1IO7**	**P1IO6**	**P1IO5**	**P1IO4**	**P1IO3**	**P1IO2**	**P1IO1**	**P1IO0**
Definition	**Port-1 I/O Control Register bit-7 0: Input Mode 1: Output Mode**	**Port-1 I/O Control Register bit-6 0: Input Mode 1: Output Mode**	**Port-1 I/O Control Register bit-5 0: Input Mode 1: Output Mode**	**Port-1 I/O Control Register bit-4 0: Input Mode 1: Output Mode**	**Port-1 I/O Control Register bit-3 0: Input Mode 1: Output Mode**	**Port-1 I/O Control Register bit-2 0: Input Mode 1: Output Mode**	**Port-1 I/O Control Register bit-1 0: Input Mode 1: Output Mode**	**Port-1 I/O Control Register bit-0 0: Input Mode 1: Output Mode**
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								

[Table: Definition of P1RD]

Address	**BBH**

Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P1RD7	P1RD6	P1RD5	P1RD4	P1RD3	P1RD2	P1RD1	P1RD0
Definition	Port-1 Resistor Disable Register bit-7 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-6 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-5 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-4 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-3 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-2 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-1 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-0 0: Resistor Enable 1: Disable
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of P1NOPN]

Address	B9H							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P1NOPN7	P1NOPN6	P1NOPN5	P1NOPN4	P1NOPN3	P1NOPN2	P1NOPN1	P1NOPN0
Definition	Port-1 Output Buffer bit-7 0: CMOS Push_Pull 1: N-ch open drain	Port-1 Output Buffer bit-6 0: CMOS Push_Pull 1: N-ch open drain	Port-1 Output Buffer bit-5 0: CMOS Push_Pull 1: N-ch open drain	Port-1 Output Buffer bit-4 0: CMOS Push_Pull 1: N-ch open drain	Port-1 Output Buffer bit-3 0: CMOS Push_Pull 1: N-ch open drain	Port-1 Output Buffer bit-2 0: CMOS Push_Pull 1: N-ch open drain	Port-1 Output Buffer bit-1 0: CMOS Push_Pull 1: N-ch open drain	Port-1 Output Buffer bit-0 0: CMOS Push_Pull 1: N-ch open drain
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

7.9. P3 (Port-3)

The Pin-3.0 to 3.7 have two functional modes, Special output Mode (BSYNC_OUT, ARX, ATX, SO, SCK) and Port Mode (Bi-directional Port Mode). Initial Staus of PCR3 (Port Control Register Bit-3) is 0 (low). The PCR3 must be set to high for any case. The direction of Port-3 can be decided bit-by-bit. The read policy in Port Mode follows that described before. Read-Modify-Write instructions read the port latch than the pin.

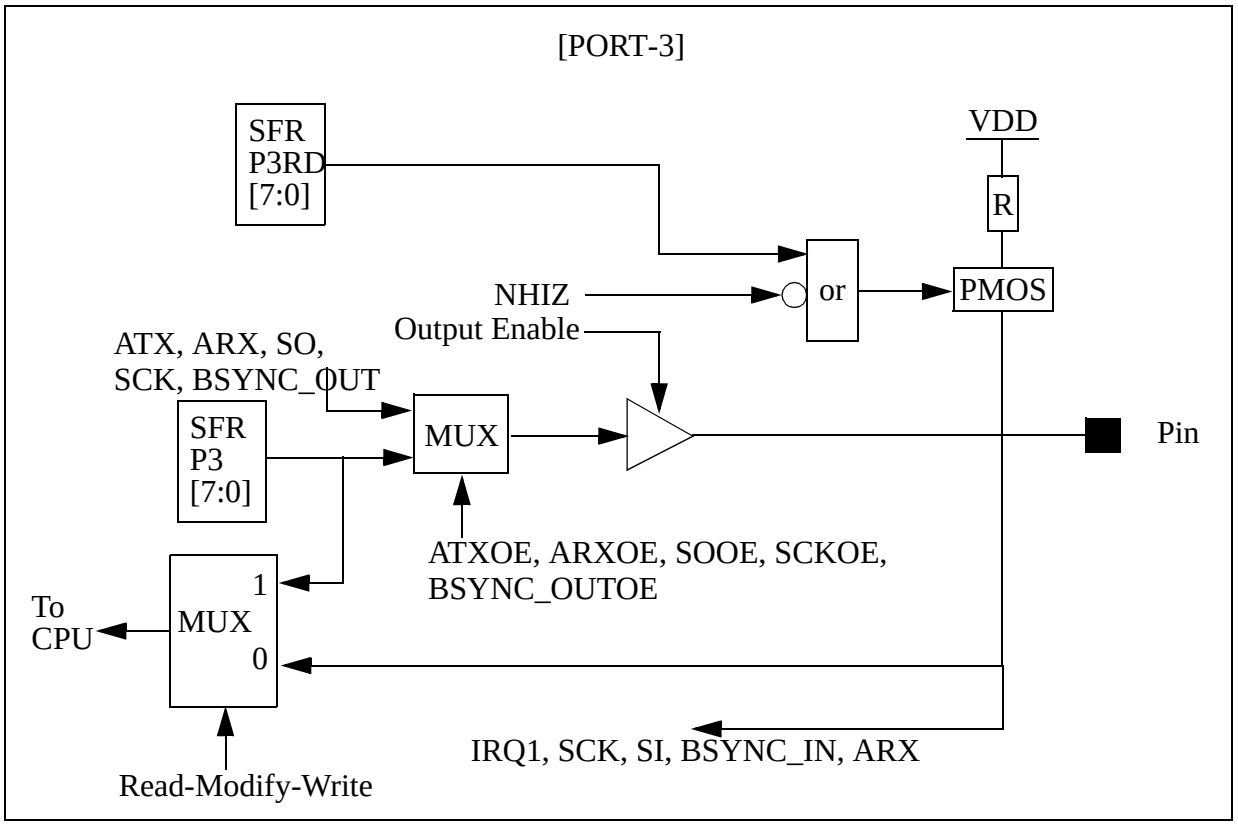
To use Pin-3.0 to 3.7 as a normal input port, PCR3 should be high. If PCR3 is high, the direction of each Port-3 pin is decided by each P3IO bit. If the P3IO bit-x is high, Port-3.x is output mode. If low, Port-3.x is input mode. Initial status is input mode because P3IO (Port-3 I/O Direction Register) is reset to 00000000B. In input mode, pull-up resistor can be connected by P3RD (Port-3 Resistor Disable Register). If the P3RD bit-x is high, Port-3.x pull-up resistor is disconnected. If low, Port-3.x pull-up resistor is connected. Initial status of P3RD is 11111111B, thus pull-up resistor is disconnected. If ZCR3 (High-Z Control Register Bit-3) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pull-up resistor is disconnected and pin status becomes high impedence. In input mode, P3.1/ARX, P3.2IRQ1, P3.5SCK, P3.6/BSYNC_IN, and P3.4/SI can be used special input pins.

To use P3.0/ATX, P3.1/ARX, P3.3/SO, P3.5/SCK, P3.7/BSYNC_OUT as a normal output port, PCR3 should be high. If the P3IO bit-x is high, Port-3.x is output mode. In output mode, pull-up resistor is not automatically disconnected regardless P3RD bit-x. If ZCR3 (High-Z Control Register Bit-3) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pin status becomes high impedence.

To use P3.3/TXEN, P3.4/MODOUT as a special output port, PCR3 should be high. And, a special output should be enabled in each block.

To use P3.6/NWR and P3.7/NRD as External Memory Read and Write Pins, PCR3 should be high. And, P3IO.6, P3IO.7, P3.6, and P3.7 latch should be high. To use P3.6/ NWR and P3.7/NRD as normal Port Pins, don’t use MOVX instructions that access External Data Memory.

When P3NOPNx = 0, Port-3.x output buffer will be CMOS Push-Pull. But, P3NOPNx = 1, Port-3.x output buffer will become N-channel Open Drain.



[Table: Definition of P3]

Address	B0H

Bit Addr.	B7H	B6H	B5H	B4H	B3H	B2H	B1H	B0H
BIT	7	6	5	4	3	2	1	0
NAME	P37	P36	P35	P34	P33	P32	P31	P30
Definition	Port-3 Pin or Latch bit-7	Port-3 Pin or Latch bit-6	Port-3 Pin or Latch bit-5	Port-3 Pin or Latch bit-4	Port-3 Pin or Latch bit-3	Port-3 Pin or Latch bit-2	Port-3 Pin or Latch bit-1	Port-3 Pin or Latch bit-0
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W RMW Ins: P37 Latch Read Other Ins: P3.7 Pin Read	R/W RMW Ins: P36 Latch Read Other Ins: P3.6 Pin Read	R/W RMW Ins: P35 Latch Read Other Ins: P3.5 Pin Read	R/W RMW Ins: P34 Latch Read Other Ins: P3.4 Pin Read	R/W RMW Ins: P33 Latch Read Other Ins: P3.3 Pin Read	R/W RMW Ins: P32 Latch Read Other Ins: P3.2 Pin Read	R/W RMW Ins: P31 Latch Read Other Ins: P3.1 Pin Read	R/W RMW Ins: P30 Latch Read Other Ins: P3.0 Pin Read
Write by Hardware								

[Table: Definition of P3IO]

Address	DAH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P3IO7	P3IO6	P3IO5	P3IO4	P3IO3	P3IO2	P3IO1	P3IO0
Definition	Port-3 I/O Control Register bit-7 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-6 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-5 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-4 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-3 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-2 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-1 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-0 0: Input Mode 1: Output Mode
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of P3RD]

Address	DBH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P3RD7	P3RD6	P3RD5	P3RD4	P3RD3	P3RD2	P3RD1	P3RD0
Definition	Port-3 Resistor Disable Register bit-7 0: Resistor Enable 1: Disable	Port-3 Resistor Disable Register bit-6 0: Resistor Enable 1: Disable	Port-3 Resistor Disable Register bit-5 0: Resistor Enable 1: Disable	Port-3 Resistor Disable Register bit-4 0: Resistor Enable 1: Disable	Port-3 Resistor Disable Register bit-3 0: Resistor Enable 1: Disable	Port-3 Resistor Disable Register bit-2 0: Resistor Enable 1: Disable	Port-3 Resistor Disable Register bit-1 0: Resistor Enable 1: Disable	Port-3 Resistor Disable Register bit-0 0: Resistor Enable 1: Disable
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of P3NOPN]

Address	ABH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P3NOPN7	P3NOPN6	P3NOPN5	P3NOPN4	P3NOPN3	P3NOPN2	P3NOPN1	P3NOPN0
Definition	Port-3 Output Buffer bit-7 0: CMOS Push_Pull 1: N-ch open drain	Port-3 Output Buffer bit-6 0: CMOS Push_Pull 1: N-ch open drain	Port-3 Output Buffer bit-5 0: CMOS Push_Pull 1: N-ch open drain	Port-3 Output Buffer bit-4 0: CMOS Push_Pull 1: N-ch open drain	Port-3 Output Buffer bit-3 0: CMOS Push_Pull 1: N-ch open drain	Port-3 Output Buffer bit-2 0: CMOS Push_Pull 1: N-ch open drain	Port-3 Output Buffer bit-1 0: CMOS Push_Pull 1: N-ch open drain	Port-3 Output Buffer bit-0 0: CMOS Push_Pull 1: N-ch open drain
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

7.10. P.4 (Port-4)

7.10.1 Overview

During External Memory Mode, P4.2 to P4.3 are used as ALE, and PSEN.

When External Memory Mode = 0, the Port-4(P4) is a 7-bit bidirectional port that can be used as special output pins (P4.6/PLLSWB).

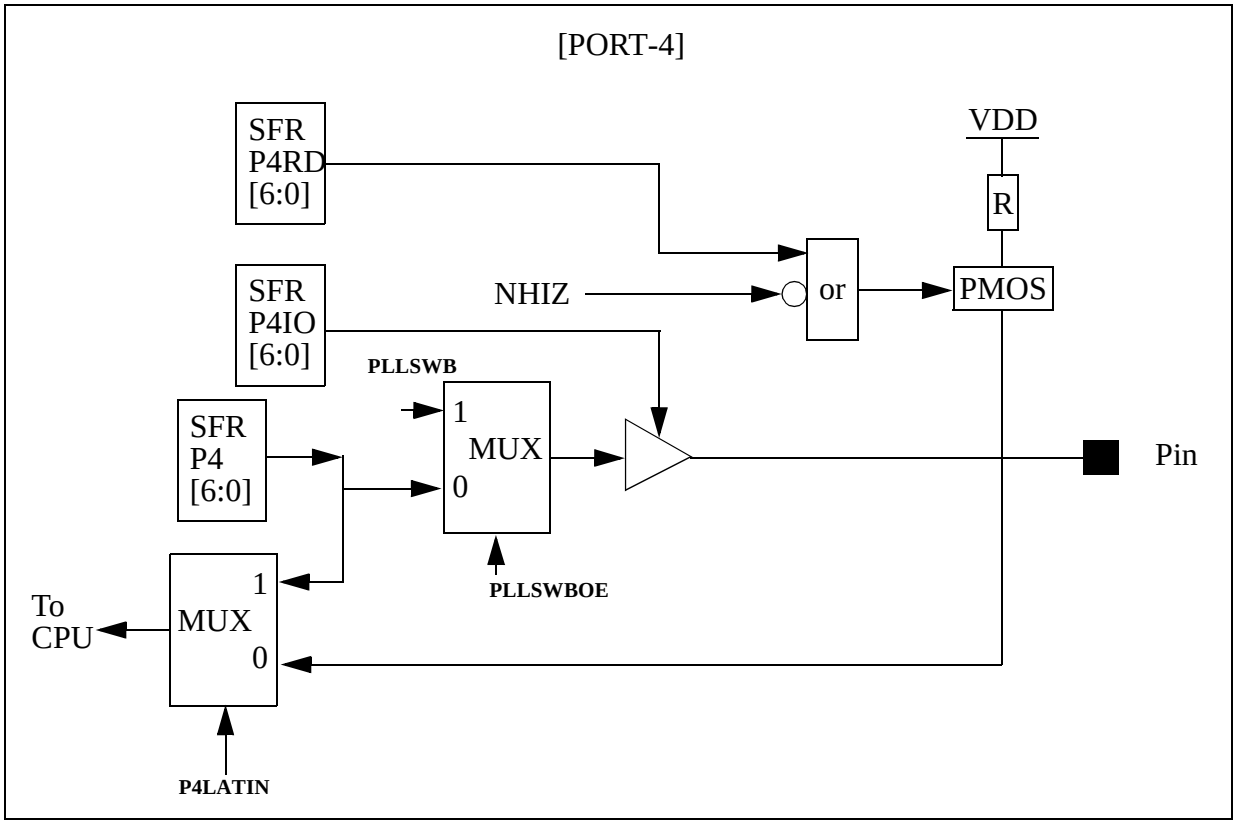
The direction of Port-4 can be decided bit-by-bit. If P4LATIN(PCR bit-4) = 0, CPU reads pin status. If P4LATIN(PCR bit-4) = 1, CPU reads port latch rather than pin.

To use Pin-4.x as a normal input port, P4IOx should be low. The direction of each Port-4 pin is decided by each P4IO bit. If the P4IO bit-x is high, Port-4.x is output mode. If low, Port-4.x is input mode. Initial status is input mode because P4IO (Port-4 I/O Direction Register) is reset to 00000000B. In input mode, pull-up resistor can be connected by P4RD (Port-4 Resistor Disable Register). If the P4RD bit-x is high, Port-4.x pull-up resistor is disconnected. If low, Port-4.x pull-up resistor is connected. Initial status of P4RD is 11111111B, thus pull-up resistor is DISconnected. If HIZ bit in the PSCR (Power Saving Control Register) becomes high, pull-up resistor is disconnected and pin status becomes high impedence.

To use Pin-4.x as a normal output port, P4IOx should be high. If the P4IO bit-x is high, Port-4.x is output mode. In output mode, pull-up resistor is not automatically disconnected regardless P4RD bit-x. If HIZ bit in the PSCR (Power Saving Control Register) becomes high, pin status becomes high impedence.

To use P4.6/PLLSWB as a special output port the output should be enabled in register SSTMCR of the SSTM block.

When P4NOPNx = 0, Port-4.x output buffer will be CMOS Push-Pull. But, P4NOPNx = 1, Port4.x output buffer will become N-channel Open Drain.



[Table: Definition of P4]

Address	C0H							
Bit Addr.		C6H	C5H	C4H	C3H	C2H	C1H	C0H
BIT		6	5	4	3	2	1	0
NAME		P46	P45	P44	P43	P42	P41	P40
Definition		Port-4 Pin or Latch bit-6	Port-4 Pin or Latch bit-5	Port-4 Pin or Latch bit-4	Port-4 Pin or Latch bit-3	Port-4 Pin or Latch bit-2	Port-4 Pin or Latch bit-1	Port-4 Pin or Latch bit-0
Reset Value		0	0	0	0	0	0	0

Read/Write by Software		**R/W P4latin=1: P46 Latch Read P4latin=0: P4.6 Pin Read**	**R/W P4latin=1: P45 Latch Read P4latin=0: P4.5 Pin Read**	**R/W P4latin=1: P44Latch Read P4latin=0: P4.4 Pin Read**	**R/W P4latin=1: P43 Latch Read P4latin=0: P4.3 Pin Read**	**R/W P4latin=1: P42 Latch Read P4latin=0: P4.2 Pin Read**	**R/W P4latin=1: P41 Latch Read P4latin=0: P4.1 Pin Read**	**R/W P4latin=1: P40 Latch Read P4latin=0: P4.0 Pin Read**
Write by Hardware								

[Table: Definition of P4IO]

Address	**EAH**							
Bit Addr.	**None**							
BIT		**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME		**P4IO6**	**P4IO5**	**P4IO4**	**P4IO3**	**P4IO2**	**P4IO1**	**P4IO0**
Definition		**Port-4 I/O Control Register bit-6 0: Input Mode 1: Output Mode**	**Port-4 I/O Control Register bit-5 0: Input Mode 1: Output Mode**	**Port-4 I/O Control Register bit-4 0: Input Mode 1: Output Mode**	**Port-4 I/O Control Register bit-3 0: Input Mode 1: Output Mode**	**Port-4 I/O Control Register bit-2 0: Input Mode 1: Output Mode**	**Port-4 I/O Control Register bit-1 0: Input Mode 1: Output Mode**	**Port-4 I/O Control Register bit-0 0: Input Mode 1: Output Mode**
Reset Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software		**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								

[Table: Definition of P4RD]

Address	**EBH**

Bit Addr.	None							
BIT		6	5	4	3	2	1	0
NAME		P4RD6	P4RD5	P4RD4	P4RD3	P4RD2	P4RD1	P4RD0
Definition		Port-4 Resistor Disable Register bit-6 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-5 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-4 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-3 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-2 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-1 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-0 0: Resistor Enable 1: Disable
Reset Value		0	0	0	0	0	0	0
Read/Write by Software		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of P4NOPN]

Address	E9H							
Bit Addr.	None							
BIT		6	5	4	3	2	1	0
NAME		P4NOPN6	P4NOPN5	P4NOPN4	P4NOPN3	P4NOPN2	P4NOPN1	P4NOPN0
Definition		Port-4 Output Buffer bit-6 0: CMOS Push_Pull 1: N-ch open drain	Port-4 Output Buffer bit-5 0: CMOS Push_Pull 1: N-ch open drain	Port-4 Output Buffer bit-4 0: CMOS Push_Pull 1: N-ch open drain	Port-4 Output Buffer bit-3 0: CMOS Push_Pull 1: N-ch open drain	Port-4 Output Buffer bit-2 0: CMOS Push_Pull 1: N-ch open drain	Port-4 Output Buffer bit-1 0: CMOS Push_Pull 1: N-ch open drain	Port-4 Output Buffer bit-0 0: CMOS Push_Pull 1: N-ch open drain
Reset Value		0	0	0	0	0	0	0
Read/Write by Software		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

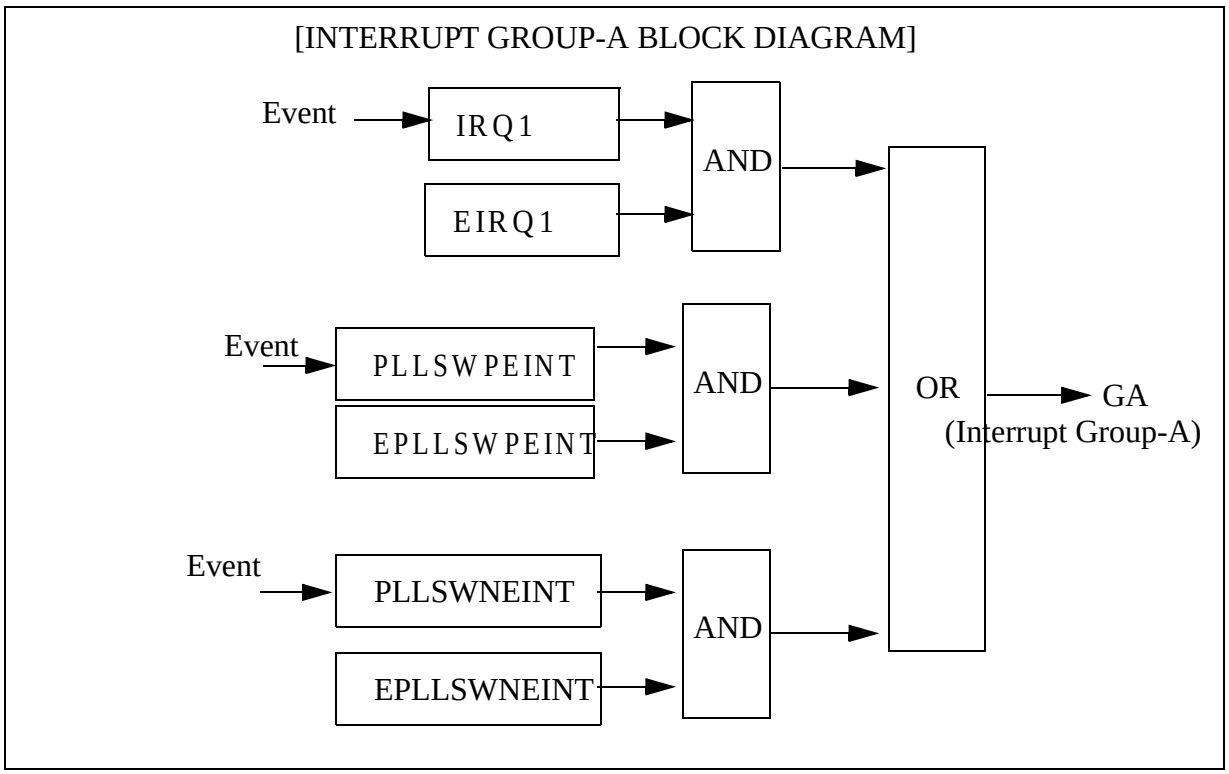
8. Interrupt Control Block

8.1. Overview

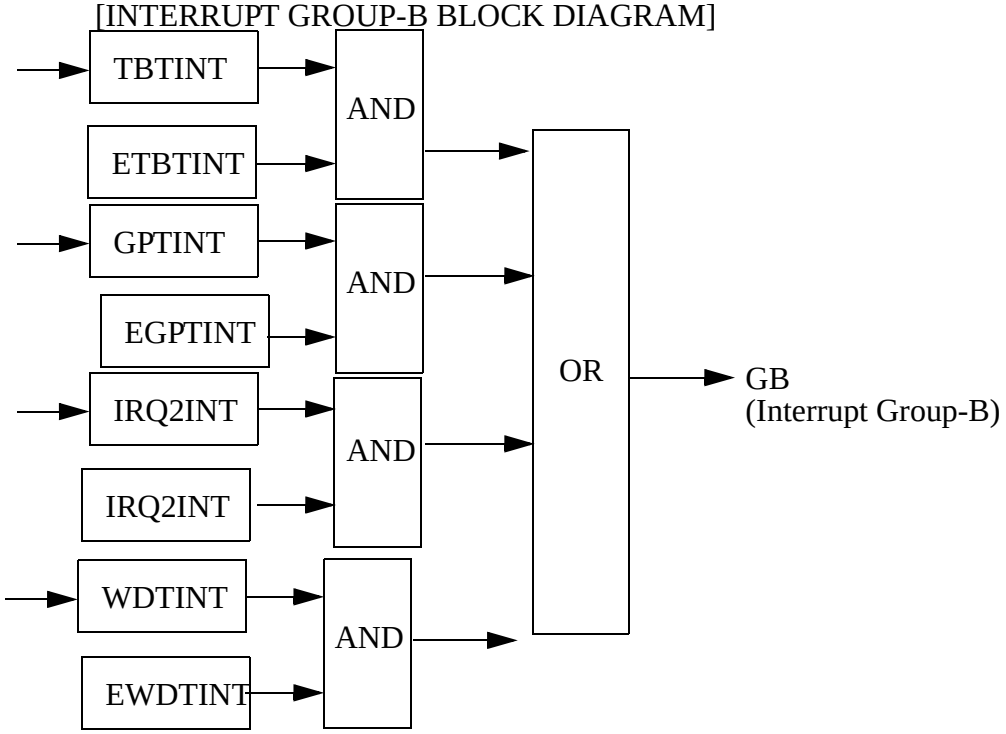
The SS1103 provides 18 interrupt sources (2 external interrupt and 16 internal interrupt). There are two external interrupt pins, IRQ0 to IRQ1. Following peripheral blocks may generate interrupt request, Watch-Dog Timer, Time Base Timer, General Purpose Timer, SPI, LBD, Signaling Word transmit or received, S/N Ratio, PLLSW positive edge, PLLSW negative edge, UART, SIO, KPD, DPF, RXF, TXF, and Lock. These interrupt sources are divided into 5 groups.

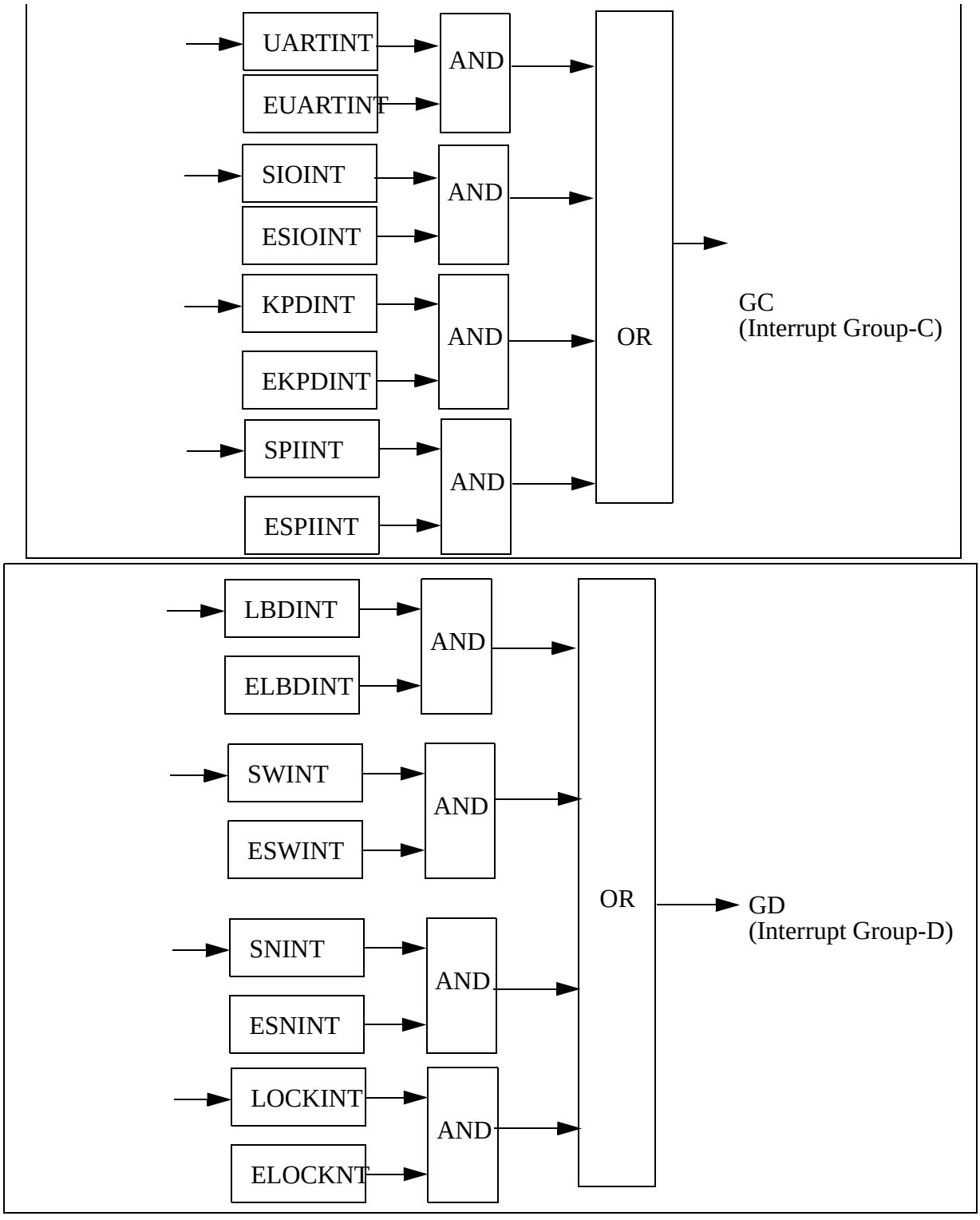
When an interrupt is generated, the interrupt request flag that generated it should be cleared by software when the service routine is vectored. All of the interrupt request flags can be set or cleared by software, with the same result as though it had been set or cleared by hardware. That is, interrupt can be generated or pending interrupts can be canceled in software. Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Registers ISE0 to ISE2. And, each of interrupt group can be enabled or disabled by setting or clearing a bit in Special Function Register IE. The bit EA in IE contains also a global disable bit (0: disable, 1: Enable), which disables all interrupts at once.

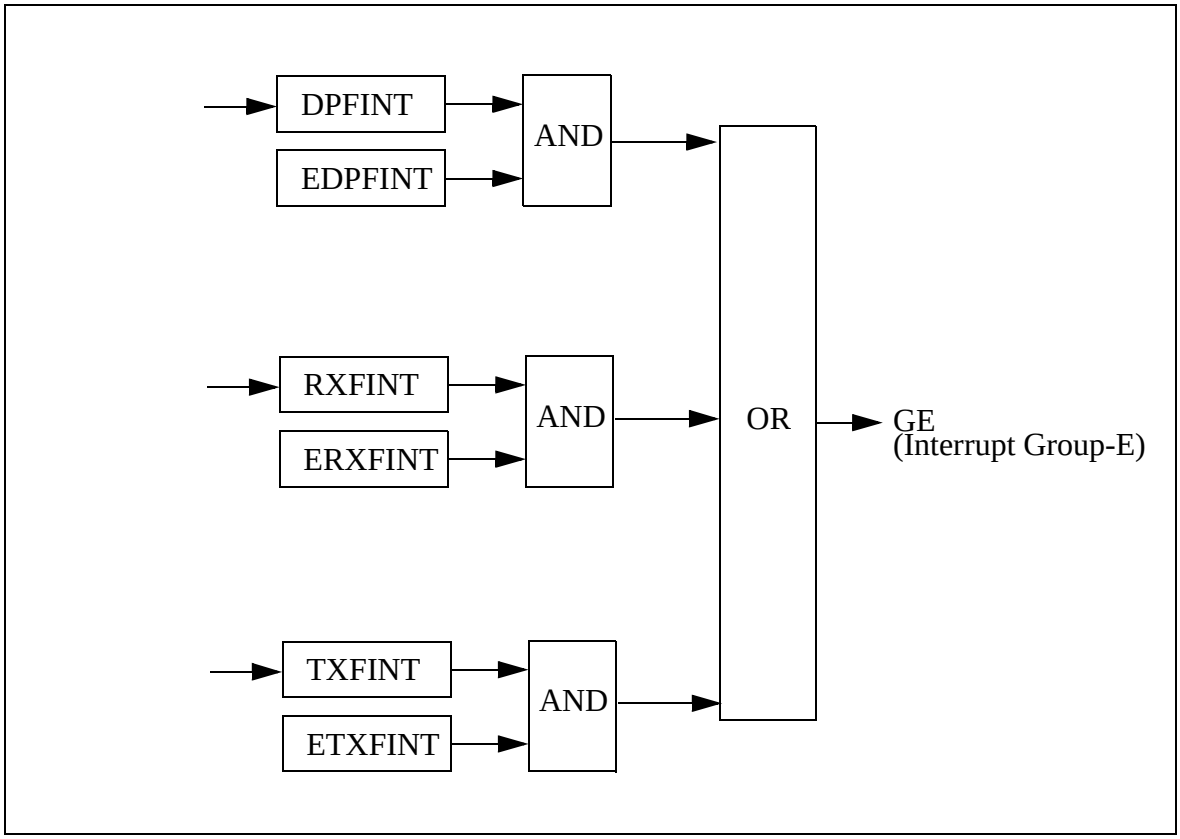
[INTERRUPT GROUP-A BLOCK DIAGRAM]

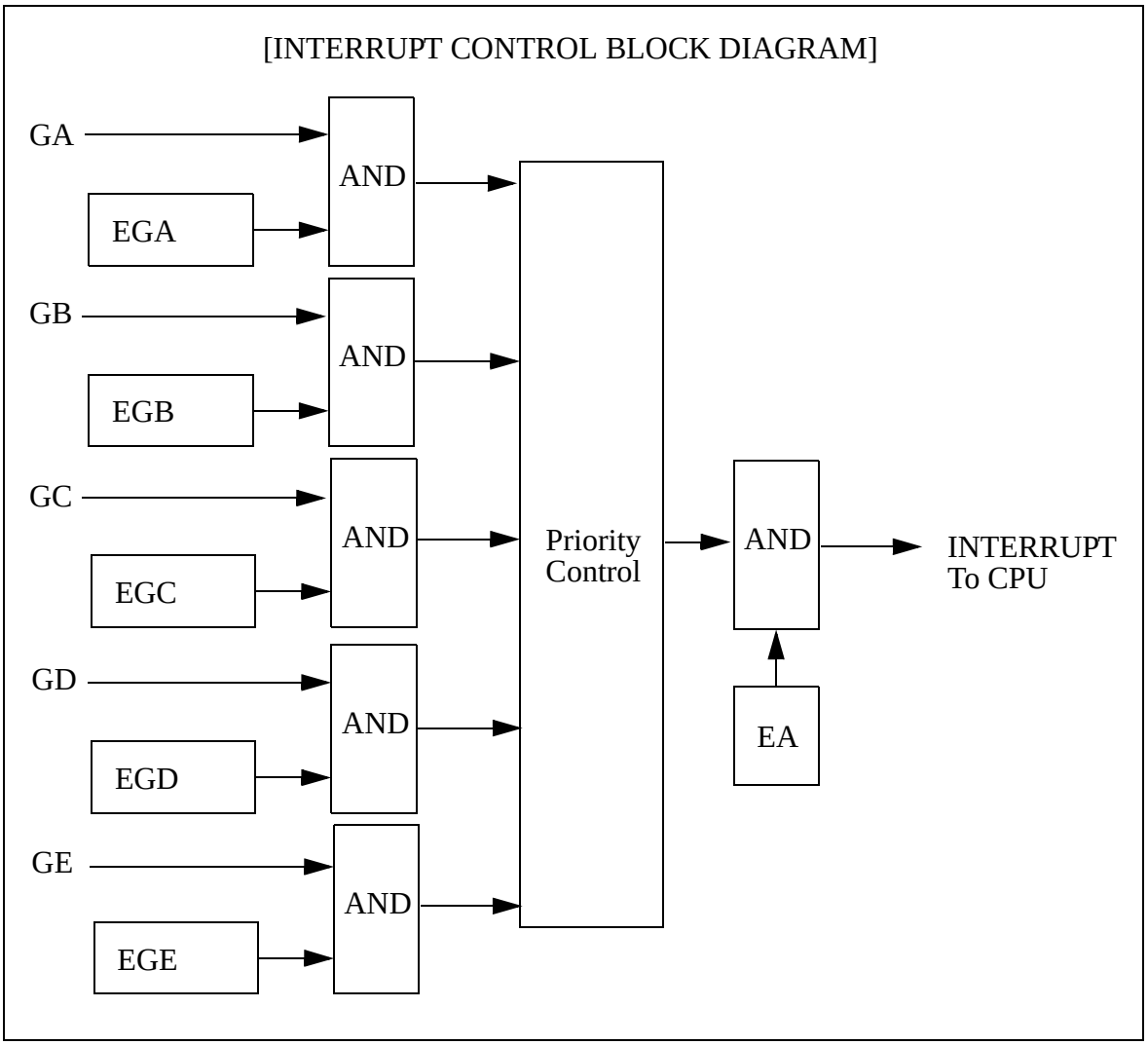


[INTERRUPT GROUP-B BLOCK DIAGRAM]




UARTINT
EUARTINT
AND
SIOINT
ESIOINT
AND
KPDINT
EKPDINT
AND
SPIINT
ESPIINT
AND
OR
GC
(Interrupt Group-C)
LBDINT
ELBDINT
AND
SWINT
ESWINT
AND
SNINT
ESNINT
AND
LOCKINT
ELOCKNT
AND
OR
GD
(Interrupt Group-D)


DPFINT
EDPFINT
AND
RXFINT
ERXFINT
AND
TXFINT
ETXFINT
AND
OR
GE
(Interrupt Group-E)


[INTERRUPT CONTROL BLOCK DIAGRAM]
GA
EGA
AND
GB
EGB
AND
GC
EGC
AND
GD
EGD
AND
GE
EGE
AND
Priority
Control
AND
EA
INTERRUPT
To CPU

8.2. External Interrupts

8.2.1 Overview

There are 2 external interrupts, IRQ0 and IRQ1. The external interrupts share pins with the Port-3.6 to Port-3.7. To use an IRQi (i = 0 to 1) pin as an external interrupt pin, the pin must be assigned to input mode by the Port-3 Control Register. The external interrupt sources can be programmed to be negative edge activated, low level activated, positive edge activated, or both edge activated by setting or clearing bit IRQi1 and IRQi0 in Register XICRn (External Interrupt Control Register). If IRQiA = 0 and IRQiB = 0, IRQi is negative edge triggered. In this mode if successive samples of the IRQi pin show a high in one sample and a low in the next cycle, interrupt request flag, IRQiF, will be set. Flag bit IRQiF then requests the interrupt. This bit must be cleared by software in the interrupt service routine. The IRQiF bit can be also set or cleared by software. If IRQiA = 1 and IRQiB = 0, IRQi is positive edge triggered. In this mode if successive samples of the IRQi pin show a low in one sample and a high in the next cycle, interrupt request flag IRQiF will be set. Flag bit IRQiF then requests the interrupt. If IRQiA = 1 and IRQiB = 1, IRQi is both (positive or negative) edge triggered. In this mode if successive samples of the IRQi pin show difference between one sample and the next sample, interrupt request flag IRQiF will be set. Flag bit IRQiF then requests the interrupt. If IRQiA = 0 and IRQiB = 1, IRQi is low level activated. If IRQi is low, interrupt request flag IRQiF will be set. In this case, software can not clear IRQiF if the pin IRQi is still low. Thus, make sure the pin IRQi becoming high level (inactivate state) in the interrupt service routine.

[Table: IRQi (i = 0 to 1) Mode Selection]

IRQiA:IRQiB	Active Edge or Level
[IRQiA:IRQiB] = 00	Negative Edge
[IRQiA:IRQiB] = 01	Low Level
[IRQiA:IRQiB] = 10	Positive Edge
[IRQiA:IRQiB] = 11	Both (Positive or Negative) Edge

8.2.2 External Interrupt Control Register (XICR0)

[Table: Definition of XICR0]

Address	A6H

Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME					IRQ2A	IRQ2B	IRQ1A	IRQ1B
Definition	Reserved bit	Reserved bit	Reserved bit	Reserved bit	IRQ2 Mode Select Bit-A	IRQ2 Mode Select Bit-B	IRQ1 Mode Select Bit-A	IRQ1t Mode Select Bit-B
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R	R	R	R	R/W	R/W	R/W	R/W
Write by Hardware								

8.3. Interrupt Request Registers (INT0, INT1, INT2)

[Table: Definition of INT0]

Address	D8H							
Bit Addr.	DFH	DEH	DDH	DCH	DBH	DAH	D9H	D8H
BIT	7	6	5	4	3	2	1	0
NAME						KPDINT	IRQ2F	IRQ1F
Definition	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	KPD Request 1: Request 0: No	IRQ1 Request 1: Request 0: No	IRQ0 Request 1: Request 0: No
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R	R	R	R	R	R/W	R/W	R/W
Write by Hardware						Set by Keypad Event	Set by IRQ2 Event	Set by IRQ1 Event

[Table: Definition of INT1]

Address	E8H							
Bit Addr.	EFH	EEH	EDH	ECH	EBH	EAH	E9H	E8H
BIT	7	6	5	4	3	2	1	0
NAME	UARTINT	SWINT	SNRINT	SPIINT	SIOINT	RXFINT	TXFINT	LOCKINT
Definition	UART Interrupt 1: Request 0: No	Signaling-Word Interrupt 1: Request 0: No	S/N Ratio Interrupt 1: Request 0: No	SPI Interrupt 1: Request 0: No	SIO Interrupt 1: Request 0: No	RXFIFO Interrupt 1: Request 0: No	TXFIFO Interrupt 1: Request 0: No	LOCK Interrupt 1: Request 0: No
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware	Set by data received or data sent	Set by SW Detect	Set by S/N Ratio Detect	Set by SPI data Ready	Set by data received or data sent	Set by RXFIFO Threshold	Set by TXFIFO Threshold	Set by LOCK Detect

[Table: Definition of INT2]

Address	F8H							
Bit Addr.	FFH	FEH		FCH	FBH	FAH	F9H	F8H
BIT	7	6	5	4	3	2	1	0
NAME	DPFINT	TBINT		GPTINT	PLLSW-NEINT	PLLSW-PEINT	LBDINT	WDINT
Definition	Dial pulse/ Flash Interrupt 1: Request 0: No	Time-Base Timer Interrupt 1: Request 0: No	Reservet Bit	General Purpose Timer Interrupt 1: Request 0: No	PLLSW Signal Interrupt 1: Request 0: No	PLLSW Signal Interrupt 1: Request 0: No	LBD Interrupt 1: Request 0: No	Watch-Dog Timer Interrupt 1: Request 0: No
Reset Value	0	0		0	0	0	0	0
Read/Write by Software	R/W	R/W		R/W	R/W	R/W	R/W	R/W

Write by Hardware	**Set by completion of pulse dialed digit**	**Set by TB-Timer Overflow**		**Set by GPT Overflow**	Set by falling edge of PLLSW	Set by rising edge of PLLSW	**Set by LBD Detect**	**Set by WDTimer Overflow**

8.4. Interrupt Source Enable Registers (ISE0, ISE1, ISE2)

[Table: Definition of ISE0]

Address	**D7H**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME						EKPDINT	**EIRQ1F**	**EIRQ0F**
Definition	**Reserved bit**	**Reserved bit**	**Reserved bit**	**Reserved bit**	**Reserved bit**	**Enable Kepad Interrupt 1: Enable 0: Disable**	**Enable IRQ1F 1: Enable 0: Disable**	**Enable IRQ0F 1: Enable 0: Disable**
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software	**R**	**R**	**R**	**R**	**R**	**R/W**	**R/W**	**R/W**
Write by Hardware								

[Table: Definition of ISE1]

Address	**E7H**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

NAME	EUAR-TINT	ESWINT	ESNRINT	ESPIINT	SIOINT	ERXFINT	ETXFINT	ELockINT
Definition	Enable UART Interrupt 1: Enable 0: Disable	Enable Signaling Word TX or RX Interrupt 1: Enable 0: Disable	Enable S/N Ratio Interrupt 1: Enable 0: Disable	Enable SPI Interrupt 1: Enable 0: Disable	Enable Serial IO Interrupt 1: Enable 0: Disable	Enable RXFIFO Interrupt 1: Enable 0: Disable	Enable TXFIFO Interrupt 1: Enable 0: Disable	Enable LOCK Interrupt 1: Enable 0: Disable
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of ISE2]

Address	F7H							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	EDPFINT	ETBINT		EGPTINT	EPLLSW-NEINT	EPLLSW-PEINT	ELDBINT	EWDINT
Definition	Enable DPF Inter-rupt 1: Enable 0: Disable	Enable Time-Base Timer Interrupt 1: Enable 0: Disable	Reserved Bit	Enable GPT Inter-rupt 1: Enable 0: Disable	Enable PLLSW Interrupt on falling edge 1: Enable 0: Disable	Enable PLLSW Interrupt on rising edge 1: Enable 0: Disable	Enable LDB Interrupt 1: Enable 0: Disable	Enable Watch-Dog Timer Interrupt 1: Enable 0: Disable
Reset Value	0	0		0	0	0	0	0
Read/Write by Software	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Write by Hardware								

8.5. Interrupt Group Enable Register (IE)

[Table: Definition of IE]

Address	A8H							
Bit Addr.	AFH	AEH	ADH	ACH	ABH	AAH	A9H	A8H
BIT	7	6	5	4	3	2	1	0
NAME	EA			EGE	EGD	EGC	EGB	EGA
Definition	Enable All Interrupt 1: Enable 0: Disable	Reserved bit	Reserved bit	Enable Group-E 1: Enable 0: Disable	Enable Group-D 1: Enable 0: Disable	Enable Group-C 1: Enable 0: Disable	Enable Group-B 1: Enable 0: Disable	Enable Group-A 1: Enable 0: Disable
Reset Value	0	unknown	unknown	0	0	0	0	0
Read/Write by Software	R/W			R/W	R/W	R/W	R/W	R/W
Write by Hardware								

8.6. Interrupt Priority Register (IP)

Each interrupt group (Group-A, B, C, D, and E) can also be individually programmed to one of two priority levels by setting or clearing a bit in Special Function Register IP. A low priority interrupt can be interrupted by a high priority interrupt, but not by another low priority interrupt. A high priority interrupt can not be interrupted by another interrupt group. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If request of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence, as follows.

[Table: Internal Priority and Vector Address]

Number	Group	Request Flags	Vector Addr.	Priority Within Level
1	Group-A	IRQ1, PLLSWNEINT, PLLSW-PEINT	0003H	Highest
2	Group-B	TBINT, GPTINT, WDINT, IRQ2	000BH	
3	Group-C	UARTINT, SPIINT, SIOINT, KPDINT	0013H	
4	Group-D	LBDINT, SWINT, SNINT, LOCKINT	001BH	
5	Group-E	DPFINT, RXFINT, TXFINT	0023H	Lowest

[Table: Definition of IP]

Address	**B8H**							
Bit Addr.	**BFH**	**BEH**	**BDH**	**BCH**	**BBH**	**BAH**	**B9H**	**B8H**
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME				**PGE**	**PGD**	**PGC**	**PGB**	**PGA**
Definition	**Reserved bit**	**Reserved bit**	**Reserved bit**	**Priority of Group-E 1: High Priority 0: Low Priority**	**Priority of Group-D 1: High Priority 0: Low Priority**	**Priority of Group-C 1: High Priority 0: Low Priority**	**Priority of Group-B 1: High Priority 0: Low Priority**	**Priority of Group-A 1: High Priority 0: Low Priority**
Reset Value	**unknown**	**unknown**	**unknown**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software				**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								

8.7. Interrupt Processing

The interrupt request flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware generated LCALL is blocked by any of the following conditions:

1. An interrupt of equal or higher priority level is already in progress

2. The current polling cycle is not the final cycle in the execution of the instruction in progress

3. The instruction in progress is RETI.

4. The instruction in progress is any access to the IE or IP registers.

Any of these four conditions will block the generation of the LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be completed before vectoring to any service routine. Condition 3 & 4 ensures that if the instruction in progress is RETI or any access to IE or IP, then at least one more instruction will be executed before any interrupt is vectored to.

The polling cycle is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. Note then that if an interrupt flag is active but not being responded to for one of the above conditions, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag once active but not serviced is not remembered. Every polling cycle is new.

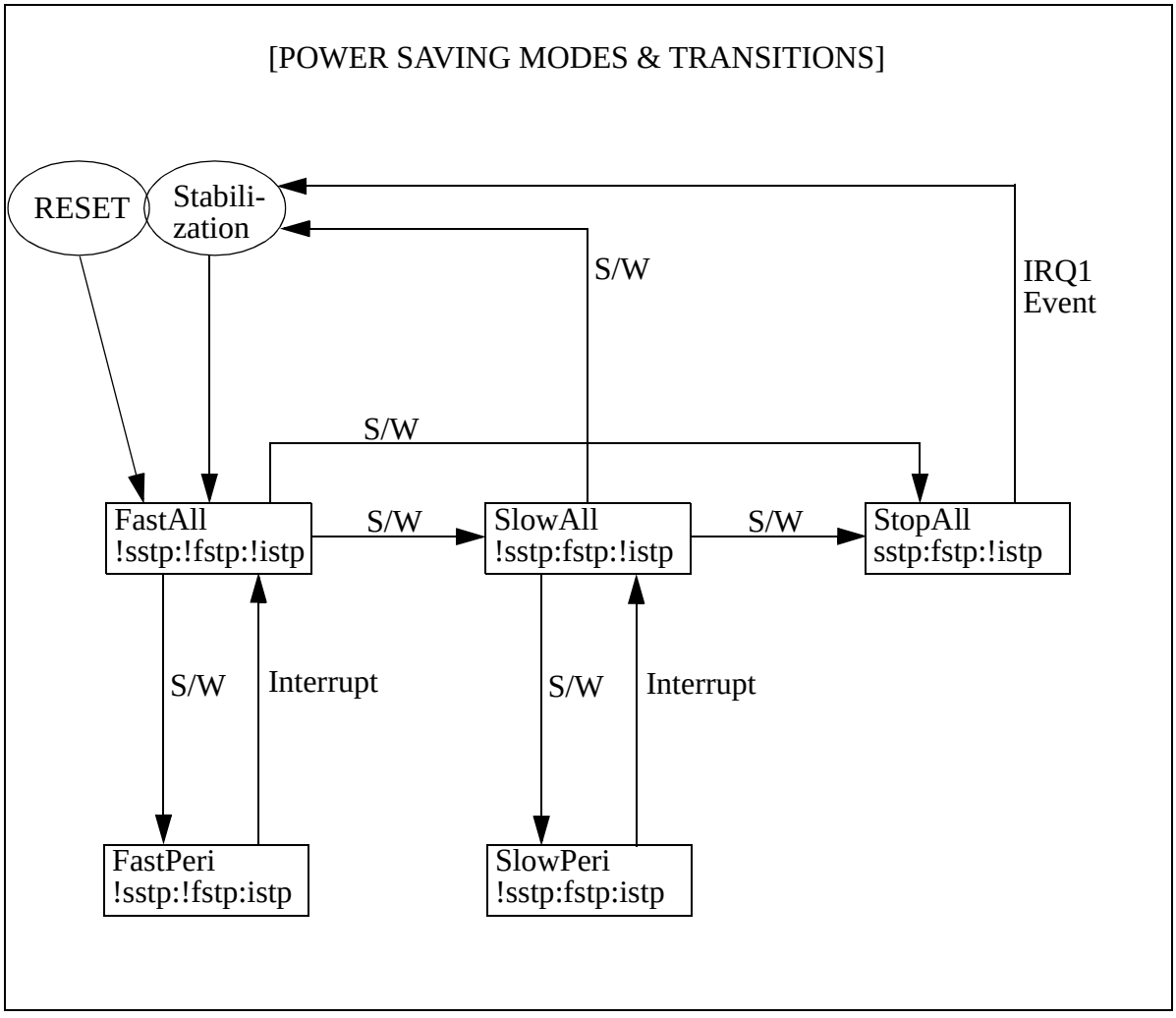
The processor acknowledges an interrupt request by executing a hardware generated LCALL to the appropriate service routine. It also clears the flag that generated the interrupt. The hardware generated LCALL pushes the contents of the Program Counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to.

Executing proceeds from that location until the RETI instructions is encountered. The RETI instruction informs the processor that this interrupt routine is no longer in progress, then pops the top two bytes from the stack and reloads the Program Counter. Execution of the interrupted program continues from where it left off. Note that a simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt was still in progress.

9. Power-Saving Modes

9.1. Overview

The MCU (Micro-Controller Unit) provides two kinds of methods to save power consumption. The first method is to stop clock operations partially or wholly. The result is to reduce switching current of CMOS. The other is to make pin status High-Z(impedance). This feature will remove static current through resistors on board. Two methods(clock control scheme and pin control scheme) can be combined together. The Power-Saving Modes are controlled by the PSCR(Power-Saving Control Register) that is an SFR(Special Function Register) mapped on memory address map. Any kind of instruction, whose destination is the PSCR, can change the PSCR content. Thus, the transitions of modes among normal and Power-Saving modes can be controlled by software. In some cases, when CPU stops, hardware signals such like interrupts, an IRQ1 Pin Event, and reset make the device change modes.



9.2. Mode Definition and Transition

There are five Clocking Modes, i.e. FastAll, SlowAll, StopAll, FastPeri, and SlowPeri modes. These are controlled by PSCR[2:0] (Power Saving Register bit 2 to 0). According to these bits, it is decided for the Fast Oscillator, Slow Oscillator(32.768KHz), and CPU operation or Instruction execution to run or stop.

There are two Pin State Modes, i.e. NorPin(Normal Pin operation mode) and HIZ(High-Z mode). The bit-4 of PSCR(HIZ) selects a mode between them.

In any mode of Clocking Modes, any Pin State Mode can be selected.

It is conceptually possible to make a new clocking power-saving mode because three bits of PSCR are assigned to select it. But, the other cases except listed five modes are never proven. If the user needs a new clocking Power-Saving mode other than listed five, to test and prove it is user's responsibility. We also recommend that only the listed mode transition is used. For other transitions than recommended transitions, user must carefully test it. When Clocking Power-Saving Mode is changed by Software, the next two instructions should be NOP(No Operation).

[Table: Clocking Power-Saving Mode Definition and PSCR]

PSCR bit	bit-2	bit-1	bit-0
Bit Name	SSTP	FSTP	ISTP
FastAll mode	0	0	0
SlowAll mode	0	1	0
StopAll mode	1	1	0
FastPeri mode	0	0	1
SlowPeri mode	0	1	1
Another Cases	Not Proven		

[Table: Clocking Power-Saving Mode Definition and PSCR]

PSCR bit	bit-4
Bit Name	HIZ
NorPin mode	0
HIZ mode	1

9.2.1 FastAll mode (a Clocking Mode)

This is a normal operation mode. All of MCU may operate normally. Both Fast and Slow oscillators generate clock signals. The Fast Clock is used as a System Clock to control the CPU and Peripherals.

In the FastAll mode, the content of the PSCR is xxxxx000B (x: don't care, B:binary). After Reset from any mode, the MCU goes into the FastAll mode.

The next available Clocking Modes are the SlowAll mode(PSCR[2:0] = 010B), FastPeri mode(PSCR[2:0] = 001B), and StopAll mode(PSCR[2:0] = 110B). All three mode transitions from FastAll mode are performed by software.

9.2.2 SlowAll mode (a Clocking Mode)

This is a slow operation mode. All of MCU may operate with low speed(32.768KHz). Fast clock generator is halted. Slow oscillator generate clock signals. The Slow Clock is used as a System Clock to control the CPU and Peripherals.

In the SlowAll mode, the content of the PSCR is xxxxx010B (x: don't care, B:binary). After Reset from this mode, the MCU goes into the FastAll mode.

Next available Clocking Modes are the FastAll mode, StopAll mode, and SlowPeri mode. All three mode transitions from SlowAll mode are performed by software.

9.2.3 StopAll mode (a Clocking Mode)

This is a perfect stop mode. All of MCU stop to operate. Both Fast and Slow clock generators are halted.

In the StopAll mode, the content of the PSCR is xxxxx110B (x: don't care, B:binary). After Reset from this mode the MCU goes into the FastAll mode. In this transition case, most SFR data will be initialized. By an External Event signal(IRQ1), the MCU goes into FastAll mode. In this transition case, all SFR and RAM data will be retained.

9.2.4 FastPeri mode (a Clocking Mode)

This is a fast Peripheral operation mode. The CPU is halted. All of Peripheral may operate with fast speed. Fast and Slow oscillators generate clock signals. The Fast Clock is used as a System Clock to control the Peripherals.

In the FastPeri mode, the content of the PSCR is xxxxx001B (x: don't care, B:binary). After Reset from this mode, the MCU goes into the FastAll mode.

Next available Clocking Modes is the FastAll mode only. The mode transition from FastPeri mode is performed by an interrupt. In this mode CPU SFRs(Special Function Registers such like PSW, ACC, and etc.) and RAM data will be retained.

9.2.5 SlowPeri mode (a Clocking Mode)

This is a slow Peripheral operation mode. The CPU is halted. All of Peripheral may operate with slow speed(32.768KHz). Fast oscillator is halted. Slow oscillators generate clock signals. The Slow Clock is used as a System Clock to control the Peripherals.

In the SlowPeri mode, the content of the PSCR is xxxxx011B (x: don't care, B:binary). After Reset from this mode, the MCU goes into the FastAll mode.

Next available Clocking Modes is the SlowAll mode. The mode transition from SlowPeri mode is performed by an interrupt. In this mode CPU SFRs(Special Function Registers such like PSW, ACC, and etc.) and RAM data will be retained.

9.2.6 NorPin mode (a Pin State Mode)

This is a normal operation mode. All of pin state can be controlled by software or hardware. This is an initial state after Reset. In the NorPin mode, the content of the PSCR is xxx0xxxxB (x: don't care, B:binary). The mode transition from NorPin mode to HIZ mode is performed by software. The NorPin mode can be combined with any kinds of Clocking Power-Saving modes.

9.2.7 HIZ mode (a Pin State Mode)

This is a Pin State Power-Saving mode. All of normal port pin state become high-impedance state to remove static current. Thus, port pin state can not be controlled by software or other hardware. In the HIZ mode, the content of the PSCR is xxx1xxxxB (x: don't care, B:binary). The mode transition from HIZ mode to NorPin mode is performed by software and reset. The HIZ mode can be combined with any kinds of Clocking Power-Saving modes. In the HIZ mode, the port register content will be retained if software or hardware don't change them. Please, refer PORT block specification.

[Table: Device States in Power-Saving Modes]

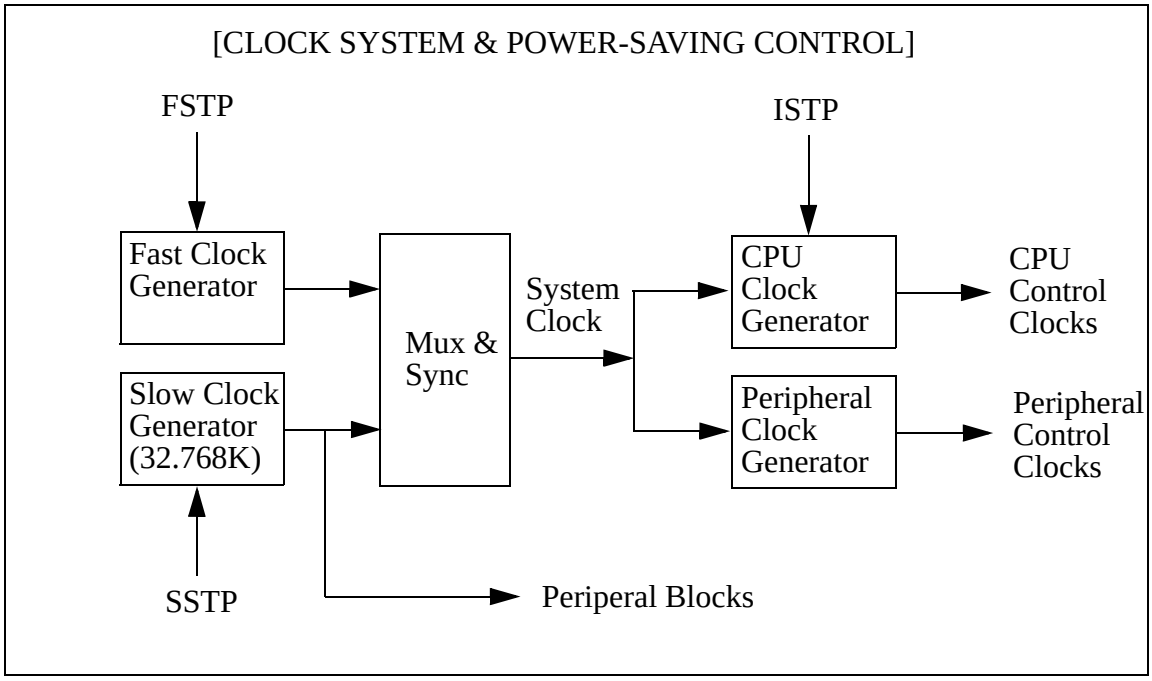
Block	FastAll	SlowAll	StopAll	FastPeri	SlowPeri
Fast Oscillator	Run	**Stop**	**Stop**	Run	**Stop**
Slow Oscillator	Run	Run	**Stop**	Run	Run
System Clock	from Fast OSC	from **Slow** OSC	**Stop**	from Fast OSC	from **Slow** OSC
CPU Clock	from Fast OSC	from **Slow** OSC	**Stop**	**Stop**	**Stop**
Peripheral Clock	from Fast OSC	from **Slow** OSC	**Stop**	from Fast OSC	from **Slow** OSC
Instruction	Run(fast)	Run(slow)	**Stop**	**Stop**	**Stop**
CPU SFR	Run(fast)	Run(slow)	**Retained**	**Retained**	**Retained**
RAM	Run(fast)	Run(slow)	**Retained**	**Retained**	**Retained**

Peripheral	Run(fast)	Run(slow)	**Stop**	Run(fast)	Run(slow)
Peri SFR	Run(fast)	Run(slow)	**Retained**	Run(fast)	Run(slow)

9.3. Power-Saving Control Register (PSCR)

[Table: Summary of PSCR]

Address	**97H**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**FSEL1**	**FSEL0**	**FTST**	**HIZ**	**NOTS**	**SSTP**	**FSTP**	**ISTP**
Definition	**Fast Clock Select Register bit-1**	**Fast Clock Select Register bit-0**	**Fast Stabilization Time for Test**	**High Impedance**	**Not Use Slow Clock**	**Slow clock SToP**	**Fast clock SToP**	**CPU clock SToP**
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Software	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware						**0 by An IRQ1 Event**	**0 by An IRQ1 Event**	**0 by Interrupt**



[Table: The Definition of Each PSCR bit]

Name	Bit	Definition
FSEL[1:0]	7 to 6	**Fast clock SELect bits** [Bit Status: 00] Fclk = 16.384 MHz [Bit Status: 01] Fclk = 8.192 MHz [Bit Status: 10] Fclk = 4.096 MHz [Bit Status: 11] Fclk = 2.048 MHz
FTST	5	**Fast Stabilization Time for Test** [Bit Status: 0] When the StopAll mode is released by an IRQ1 Event, fast oscillator stabilization time will be 12mSec (1/16.384MHz x ($2^{18-1}+2^{17-1}$)). [Bit Status: 1] When the StopAll mode is released by an IRQ1 Event, fast oscillator stabilization time will be 3.9uSec (1/16.384MHz x 2^{7-1}).

HIZ	4	**PIN State control bit** [Bit Status: 0] Normal Pin state. [Bit Status: 1] All normal I/O pins become High-Z(impedance) state.
NOTS	3	**Not Use Slow Oscillator bit** [Bit Status: 0] Slow oscillator (32.768KHz) is used. [Bit Status: 1] Slow oscillator is not used. The pin XSIN is connected to ground.
SSTP	2	**Slow clock SToP bit** [Bit Status: 0] Slow oscillator (32.768KHz) operates. [Bit Status: 1] Slow oscillator stops.
FSTP	1	**Fast clock SToP bit** [Bit Status: 0] Fast oscillator operates and drives all CPU and peripherals. [Bit Status: 1] Fast oscillator stops. Slow oscillator (32.768KHz) may or may not drive all CPU and peripherals.
ISTP	0	**Instruction SToP bit** [Bit Status: 0] CPU control clocks drive CPU. Thus, instructions may be executed its operations normally. [Bit Status: 1] CPU control clocks stop. Thus, CPU stops to execute instructions.

9.4. Stop Release Register (SREL)

[Table: Summary of SREL]

Address	**96H**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**SREL1**	**SREL0**
Definition							**Stop Release bit-1**	**Stop Release bit-0**
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Read/Write by Software	**R**	**R**	**R**	**R**	**R**	**R**	**R/W**	**R/W**
Write by Hardware								

[Table: The Definition of Each SREL bit]

Name	Bit	Definition
SREL[1:0]	1 to 0	**Stop Release Bit-1 to 0** [Bit Status: 01] IRQ1 Low Level enabled [Bit Status: 10] IRQ1 High Level enabled [Other Cases] StopAll Mode can not be released by IRQ1 pin event, can be released by only Reset. Stop Release by IRQ1 should be enabled just before going into the StopAll mode. If it is enabled in other mode, unexpected mode transition will be happened.

10. Direct Sequence Spread Spectrum Baseband Modem (SSTM)

10.1. General

The SSTM is a low-power, multi-purpose communication module designed to support spread spectrum digital voice communications. The SSTM contains all the baseband function required for an FCC Part 15 compliant device.

The SSTM supports 32Kbps ADPCM in full duplex operation. The full-duplex operation is achieved by using a time-division duplex (TDD) protocol and burst structure.

The SSTM is made up of five functional modules. These include the receiver, the transmitter, the time-division duplex (TDD) controller, the transmit and receive FIFOs, and the master clock generator.

10.1.1 Receiver

The receiver module performs all the digital signal processing required by the spread spectrum receiver, including de-correlation and demodulation.

The receiver samples the incoming baseband signal at two samples per PN chip. The samples are correlated with eight possible PN sequences in 64-bit parallel correctors. The de-correlated signal is demodulated via a digital phase locked loop. To reduce power consumption, the receiver is powered down while the SSTM is transmitting and consumes peak power only during the brief period of initial acquisition. After acquisition, the receiver goes into tracking/detection mode, where the power consumption of the receiver module is reduced by two orders of magnitude.

10.1.2 Transmitter

The transmit module generates the spread spectrum binary sequence for output to the RF modulator.

The transmitter logic encodes three consecutive bits of data into one of eight possible 32-bit PN sequences. The transmitted PN sequence is further randomized by modulus-2 addition with a fixed 2047-bit long PN sequence. This operation smooths the output spectrum of the transmitted signal and eliminates discrete spectral components. During TDD operation, the transmitter is powered off during the portion of the cycle when the SSTM is in receive mode in order to save power. The transmitter output is at high-impedance state during a receiving period.

10.1.3 TDD Controller

The time-division duplex (TDD) controller implements the “ping-pong” protocol that allows a full-duplex link to be emulated by a half-duplex radio. The TDD controller also generates the appropriate clock and control signals to other modules of the SSTM and multiplexes and de-multiplexes the overhead bits with the data bit-stream. The TDD controller also uses a digital phase locked loop to maintain an equal read and write rate to the FIFOs as to avoid FIFO overflow or underflow. In addition, the TDD controller contains logic to generate the proper handshaking signals .

10.1.4 FIFOs

The transmit and receive FIFOs are used to buffer the transmit and receive data. The SSTM includes a 30-byte transmit FIFO and a 30-byte receive FIFO to buffer the input and output data. The control signals for the FIFOs are generated by the TDD controller.

10.1.5 Master Clock Generator

The master clock generator generates the various clock signals required by the modules described above. It can be disabled in power saving mode by setting the SSTMCR bit 2 (ENABLE) to 0.

10.2. Voice Full-Duplex Operation

Although the SSTM actually only uses a half-duplex channel for communication with the remote device, full-duplex operation is provided by using a time-division duplex (TDD) protocol. The TDD protocol basically configures the SSTM alternatingly as a transmitter and as a receiver. When two devices are communicating with each other, one is programmed to be the master, while the other is programmed to be the slave. The TDD protocol ensures that while the master is transmitting, the slave is receiving and vice versa in a timely fashion. The end result is that as far as the user is concerned, the communication link appears to be full-duplex. In order to achieve this, it is necessary for the SSTM to transmit at a higher rate than the actual user data rate. Ideally, for TDD operation, with 100% efficiency and 0% overhead, the SSTM must transmit the data at twice the user data rate since the SSTM has only half the time to transmit the user data (during the other half time period, the SSTM is receiving from the remote station). Overhead such as preamble, unique word (UW), as well as other signaling information bits result in the SSTM transmitting at 4 times the effective user data rate. The size of the FIFOs on the SSTM is designed to provide sufficient buffer during both transmit and receive operations so that underflow or overflow of the FIFOs does not occur.

When communication between two devices first commences, the microprocessors must program one of the devices as the Master and the other device as the Slave. The master device transmits periodic bursts as soon as the SSTM is reset (SSTM should be reset after the loading the configuration parameters).

The burst timing of the Master is derived from its internal master clock oscillator and can be computed from below:

$$f_{burst} = \frac{f_{mosc}}{128}$$

In , f_{burst} is the burst rate and f_{mosc} is the master oscillator frequency. As the transmitter uses a three bit per symbol modulation scheme, the chip rate is 32/3 times the burst rate or

$$f_{chip} = \frac{f_{mosc}}{12} = \frac{32}{3} \times f_{burst}$$

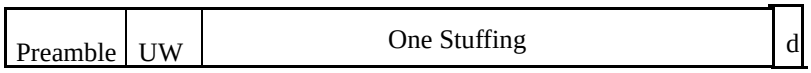
where f_{chip} is the chip rate and f_{mosc} is the master oscillator frequency. Effectively, the spread spectrum transceiver operates at 32/3 chips/bit or 32 bits/symbol where each symbol is composed of 3 bits.

The total number of bits per burst is fixed and equal for both the Master and the Slave. The Slave derives its burst timing from the Master by detecting the UW pulse transmitted by the Master.

10.3. TDD Protocol

Initially, the two communicating devices need to establish “sync”. The TDD protocol achieves this by using a special handshaking protocol. The Master first transmits an “acquisition burst”. The acquisition burst consists of 30 bits of preamble (binary 0’s), followed by 146 bits of “zero stuffing”, and four 22-bit unique words (UW). When the Slave receives the acquisition burst from the Master correctly (by decoding the 4 consecutive UWs), it sends an acquisition burst in response. When the Master receives the acquisition burst, it sends an “empty burst”. An empty burst contains a 30-bit preamble followed by a single 22-bit unique word, and 212-bit of “1” (One stuffing). In response to the master’s empty burst, the Slave also sends an empty burst back to the Master. When the Master receives the empty burst from the Slave, the communication link is considered to have been established and “sync” condition achieved. On the following burst, both the Master and the Slave start genuine data transmission by sending out “data bursts”. Each of the data bursts contain a 30-bit preamble, followed by a 22-bit UW, a 32-bit Signaling Word (SW), and 160 bits of user data, followed by 20 bits of the parity check (one parity check bit for each byte of data). The three different types of burst frame structures are shown below.

Acquisition Burst Frame Structure



Empty Burst Frame Structure

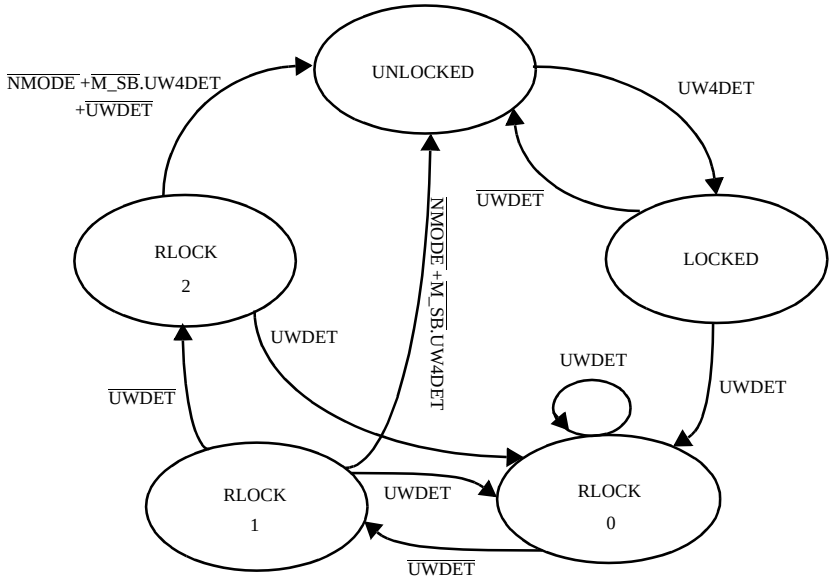
Data Burst Frame Structure

Field	Bits
Preamble	30
Unique Word (UW)	22
Signaling Word (SW)	32
Data	160
Parity Check (PC)	20
Internal Delay (d)	6

Burst Frame Structures

Each burst cycle also includes 2 “Guard” times to allow for both propagation and RF transceiver switching time. More specifically, G_1 is a 50-bit delay between the time the Master stops transmission and the Slave commences transmission; G_2 is a 50-bit delay between the time the Slave stops transmission and the Master commences transmission. These guard times allow for a minimum delay of 392µsec delay (for a master oscillator frequency of 16.384 MHz). The total burst cycle is 640 bits long, including 12 bits internal delay (the transmitter turns off 6 bits after the last data bit is latched into the transmitter, the master and slave therefore contribute a total of 12-bit internal delay).

During TDD operation, the receiver will go through several stages. Initially, when the 4 UWs of the acquisition burst has been received and decoded correctly, the receiver (either Master or Slave) declares “locked”. After the empty burst has been decoded, the receiver declares “rlocked” signifying that the remote device has locked. The behavior of the receiver after establishing the RLOCK condition depends on whether the internal state machine is turned on or not (determined by the setting of the bit CI_h[4] of the control register CI_h). When the state machine is turned off, transmission will be turned off whenever the UW is not detected. The Slave then waits for a new acquisition burst while the Master will start the acquisition cycle again by transmitting an acquisition burst. Note that the Master will continue to broadcast acquisition bursts until it has received a proper acquisition burst from the Slave in response. The Master will always revert back to the initial acquisition mode (broadcasting acquisition bursts), whenever it fails to detect the proper UWs from the slave.



Receiver Lock State Machine

If the state machine is turned on, then the receiver will not declare LOCK loss right after UW has not been detected. Instead, it will allow for UW errors in up to two further bursts before declaration LOCK loss. The state diagram for this lock state machine is shown in In the figure, UW4DET indicates the condition when the four UWs have been detected during acquisition burst, UWDET indicate the condition where the single UW in empty and data bursts has been detected. M_SB is the programmed bit (CI_h[0]) which is a binary “1” when the SSTM is programmed to be the master and a binary “0” when programmed as a slave.

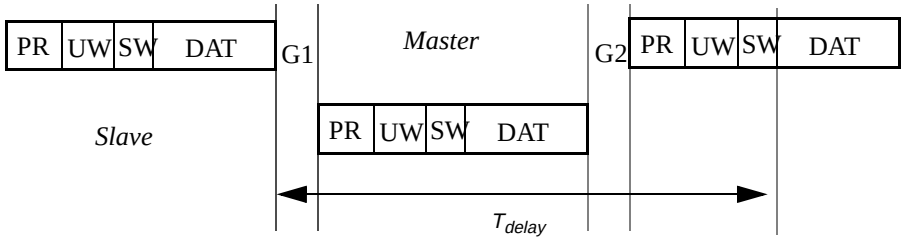
NMODE is a signal generated by the receive logic when the digital phase locked loop in the receiver has achieved lock in the half-duplex mode, it is similar to the LOCK signal in full-duplex. Note that in the half-duplex mode there is no an acquisition block or empty block. The NMODE signal is independent of the UW detection. Physically, when NMODE is asserted, it indicates that PN acquisition has been achieved. The LOCKED and RLOCK states are as described previously.

10.4. System Delay

To calculate the delay through the system (see FIGURE 3), assume that the transmit FIFO is almost empty at the end of a burst. Then the next bit that enters the transmit FIFO will experience a system delay (excluding propagation delay but including the internal logic delay) of approximately:

$$T_{delay} = 2 \times (T_G + T_{PR} + T_{UW} + T_{SW}) + T_{DAT} + T_{\Delta} \qquad \text{(EQ 3)}$$

where T_G is the time delay due to Guard Time (note: G = G1 = G2 = 50bits), T_{PR} is the time delay due to preamble, T_{UW} is the time delay of the UW, T_{SW} is the time delay for signaling word transmission, T_{DAT} is the time delay for data transmission, and T_{Δ} is the internal logic delay. For a 32 Kbps full duplex data rate signal, with a master oscillator (MO) of 16.384 MHz, this system delay translates into 3.55 msec.

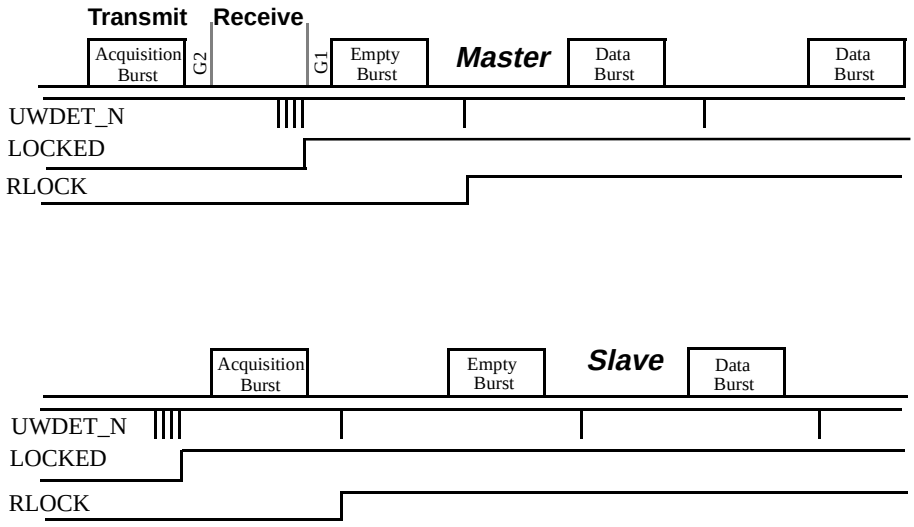


System Delay

10.5. Timing Information

Two chips communicating with each other should have RTS_N bit enabled (CI_h[7] bit should be set to 0). A chip which is configured as a Master starts the acquisition procedure and data transmission. A Slave waits for a valid spread spectrum signal to arrive.

A typical start-up of the data link is shown in Figure 4



Typical Communication Link Start-Up. Full Duplex.

In the full-duplex mode the SSTM when programmed as a Master, starts transmission as soon as the reset bit in SSTMCR is released (RTS_N is enabled). As long as the Master is powered-on the SSTM will send out the acquisition burst and try to establish a communication link with a remote Slave. Thus, the communication channel is occupied as soon as the Master resets, and this can occur before any data becomes available for transmission. Once the communication link is established, even when there is no data to be transmitted, the Master and Slave will remain in communication with each other (sending out “1” in the data field) indefinitely or until the Master is disabled.

10.6. Control Registers

One register is available for controlling the SSTM block within the SS1103. It is the SSTM control register (SSTMCR). This register provides the enable and software reset for the SSTM module. It also contains the control to enable certain outputs of the SSTM to the SS1103 port pins.

Table: Definition of SSTMCR

Address	**C1H**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME				**RESET**	**PLLSBOE**	**EN**	**BSYN-CLB**	**BSYNCOE**
Reset Value	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**
Read/Write by Software	**R**	**R**	**R**	**R**	**R/W**	**R/W**	**R/W**	**R/W**

Legend:

Bit7 - Bit4 Reserved. These bits always read "0".

RESET Reset. Writing a "0" to this bit resets the SSTM. The bit is set back to "1" by hardware.

EN Enable. Writing a "1" to this bit enables the SSTM. Writing a"0" to this bit disables the SSTM by stopping its clock.

BSYNCLB Bsync Loopback. Writing a "1" to this bit internally connects Bsync_out to Bsync_in. Those pins may then be used for GPIO.

BSYNCOE Bsync Output Enable. This bit must be set to a "1" to enable the Bsync_out signal to the Bsync_out pin. When this bit is a "0" the Bsync_out pin may be used for GPIO.

PLLSWBOE Writing a “1” to this bit enables the inverted PLLSW signal to the pin P4.6. When this bit set to “0” the P4.6 pin can be used as GPIO.

A total of sixty-two registers are available for storing the various programming parameters. They are listed below:

Name	Address	Bank Select CI_l[0]	Bank Select CI_l[1]	Index	Write/ Read	Functions
CI_h	8F	0	0	[7:0]	WR/ RD	CI_h[0]: Master/Slave Selection bit CI_h[3:1]:Number of errors allowed in the UW CI_h[4]:LockSMon CI_h[5]:Reserved CI_h[6]:Reserved CI_h[7]:RTS_N bit (0 to enable)
CI_l	8E	X Don't Care	X Don't Care	[7:0]	WR/ RD	CI_l[1:0]: Bank Select CI_l[3:2]:Width of ESD Window CI_l[4]: Set the Width of "Central Region" CI_l[5]: DPLL Accumulator 1 Reset CI_l[7:6]: Set the Width of "Detection Window"
	FE	0	0	[7:0]		Reserved
IS	C8	0	0	[7:0]	RD	IS[0]: RXSW Interrupt Pending IS[1]: S/N Interrupt Pending IS[6:2]: Reserved IS[7]: TXSW Transmit Interrupt Pending
LCK	9E	0	0	[1:0]	RD	LCK[0]: LOCK Achieved LCK[1]: RLOCK Achieved
	AE	0				Reserved
S/N	AF	0	0	[7:0]	Read	Signal/Noise indicator
PNA0	BE	0	0	[7:0]	WR/ RD	PNA[7:0]
PNA1	CE	0	0	[7:0]	WR/ RD	PNA[15:8]
PNA2	DE	0	0	[7:0]	WR/ RD	PNA[23:16]

Name	Address	Bank Select CI_l[0]	Bank Select CI_l[1]	Index	Write/ Read	Functions
PNA3	EE	0	0	[7:0]	WR/ RD	PNA[31:24]
PNB0	BF	0	0	[7:0]	WR/ RD	PNB[7:0]
PNB1	CF	0	0	[7:0]	WR/ RD	PNB[15:8]
PNB2	DF	0	0	[7:0]	WR/ RD	PNB[23:16]
PNB3	EF	0	0	[7:0]	WR/ RD	PNB[31:24]
UW0	8F	0	1	[7:0]	WR/ RD	UW[7:0]
UW1	FE	0	1	[7:0]	WR/ RD	UW[15:8]
UW2	C8	0	1	[7:0]		UW[21:16]
	9E	0	1	[7:0]		Reserved
	9F	0	1	[7:0]		Reserved
	AE	0	1	[7:0]		Reserved
	AF	0	1	[7:0]		Reserved

Name	Address	Bank Select CI_l[0]	Bank Select CI_l[1]	Index	Write/ Read	Functions
PNC0	BE	0	1	[7:0]	WR/ RD	PNC[7:0]
PNC1	CE	0	1	[7:0]	WR/ RD	PNC[15:8]
PNC2	DE	0	1	[7:0]	WR/ RD	PNC[23:16]
PNC3	EE	0	1	[7:0]	WR/ RD	PNC[31:24]
PND0	BF	0	1	[7:0]	WR/ RD	PND[7:0]
PND1	CF	0	1	[7:0]	WR/ RD	PND[15:8]
PND2	DF	0	1	[7:0]	WR/ RD	PND[23:16]
PND3	EF	0	1	[7:0]	WR/ RD	PND[31:24]
TXSW0/ RXSW0	8F	1	0	[7:0]	WR/ RD	Less Significant Byte of SW. Transmitted/ Received first.
TXSW1/ RXSW1	FE	1	0	[7:0]	WR/ RD	Second Byte of SW
TXSW2/ RXSW2	C8	1	0	[7:0]	WR/ RD	Third Byte of SW.
TXSW3/ RXSW3	9E	1	0	[7:0]	WR/ RD	Fourth, Most Significant Byte of SW.

Name	Address	Bank Select CI_l[0]	Bank Select CI_l[1]	Index	Write/ Read	Functions
	AE	1	0	[7:0]		Reserved
	AF	1	0	[7:0]		Reserved
PNE0	BE	1	0	[7:0]	WR/ RD	PNE[7:0]
PNE1	CE	1	0	[7:0]	WR/ RD	PNE[15:8]
PNE2	DE	1	0	[7:0]	WR/ RD	PNE[23:16]
PNE3	EE	1	0	[7:0]	WR/ RD	PNE[31:24]
PNF0	BF	1	0	[7:0]	WR/ RD	PNF[7:0]
PNF1	CF	1	0	[7:0]	WR/ RD	PNF[15:8]
PNF2	DF	1	0	[7:0]	WR/ RD	PNF[23:16]
PNF3	EF	1	0	[7:0]	WR/ RD	PNF[31:24]
NSCTRL	8F	1	1	[7:0]	WR/ RD	NSCTRL[1]: Enable NSCTRL[0]: Mode
NSVAL	FE	1	1	[7:0]	WR/ RD	Noise Value

Name	Address	Bank Select CI_l[0]	Bank Select CI_l[1]	Index	Write/ Read	Functions
PER-RCNT	C8	1	1	[7:0]	R	Parity Check Error Count
	9E	1	1	[7:0]		Reserved
	9F	1	1	[7:0]		Reserved
	AE	1	1	[7:0]		Reserved
	AF	1	1	[7:0]		Reserved
PNG0	BE	1	1	[7:0]	WR/ RD	PNG[7:0]
PNG1	CE	1	1	[7:0]	WR/ RD	PNG[15:8]
PNG2	DE	1	1	[7:0]	WR/ RD	PNG[23:16]
PNG3	EE	1	1	[7:0]	WR/ RD	PNG[31:24]
PNH0	BF	1	1	[7:0]	WR/ RD	PNH[7:0]
PNH1	CF	1	1	[7:0]	WR/ RD	PNH[15:8]
PNH2	DF	1	1	[7:0]	WR/ RD	PNH[23:16]

Name	Address	Bank Select CI_l[0]	Bank Select CI_l[1]	Index	Write/ Read	Functions
PNH3	EF	1	1	[7:0]	WR/ RD	PNH[31:24]

10.7. Configuration Information Bits and Registers Description

The configuration information bits are used to set the various programmable parameters in the SSTM:

CI_h[0]M/SB. Set the SSTM to be a Master (HI) or Slave (LO).

CI_h[3:1]T. Number of errors allowed in the UW. CI_h[1]is LSB, CI_h[3] is MSB.

T	Allowable UW Errors
0	0 bit
1	1 bit
2	2 bits
3	3 bits
4-7	4 bits

CI_h[4]LockSMon. Enables the Locking State Machine when set to HI (see for Locking State Machine state diagram).

CI_l[0] Should be set to LO .

CI_l[3:2]PLSL. Sets the width of the ESD window. CI_l[2] is LSB, CI_l[3] is MSB. See Application Section.

PLSL	Width of ESD window
0	8 samples wide
1	10 samples wide

2	12 samples wide
3	14 samples wide

CI_l[4]CNTLR. Sets the width of the “Central Region”. (**NOTE**: CNTLR size must be ≤ PLSL size).See Application Section.

CNTLR	**Width of Central Region**
0	10 samples wide
1	12 samples wide

CI_l[5]ACC1RES. DPLL Accumulator 1 reset. See Application Section.

ACC1RES	**Accumulator 1 Reset**
0	ACC1 NOT reset.
1	Reset ACC1.

CI_l[7:6]WSL. Sets the width of the “Detection Window”. CI_l[6] is LSB, CI_l[7] is MSB. See Application Section.

WSL	**Width of Detection Window**
0	4 samples wide
1	6 samples wide
2	8 samples wide
3	10 samples wide

CI_h[0]M/SB. Set the SSTM to be a Master (HI) or Slave (LO).

CI_h[3:1]T. Number of errors allowed in the UW. CI_h[1]is LSB, CI_h[3] is MSB.

T	Allowable UW Errors
0	0 bit
1	1 bit
2	2 bits
3	3 bits
4-7	4 bits

CI_h[4] LockSMon. Enables the Locking State Machine when set to HI (see for Locking State Machine state diagram).

IS Interrupt Status register. Presents the status of interrupts which corresponding bits are enabled in the Interrupt control module. The SSTM interrupts from different sources are multiplexed. To find which service phase generated the interrupt, the IS should be read (see section “Interrupt Control Block).

PNx0-3 PN sequences store registers. Each register stores one byte of 4-byte corresponded PN sequence. Eight PN sequences shoud be stored (PNA, PNB, PNC, PND, PNE, PNF, PNG, and PNH). The same PN sequences should be stored for a Master and for a Slave.

LCK[1,0] When LCK[0] high indicates that LOCK is achieved. When LCK[1] high indicates that RLOCK is achieved. To enable this indication the LOCKINT bit of INT1 register should be set to 1.

NSCTRL[1:0] Parity Check Error Contro Register. See Section “Error Detection and Control”

NSVAL[7:0] Replacement value for the erroneously received byte. See Section “Error Detection and Control”

PERRCNT[7:0] Parity Check Errors counter. Counts the number of parity errors received during one frame. See Section “Error Detection and Control”

10.8. Programming the SSTM

10.8.1 Overview

The SSTM should be programmed by reading and writing data into the control registers. The use of the control registers is provided in the sections above. In this section the operations with a signaling word, S/N ratio, Error Detection and Control, and SSTM parameters are described.

The configuration change based on the configurations information bits written into the control registers takes place after the reset.

10.8.2 Read/Write the Signaling Word

Once every burst the 32-bit Signaling Word (SW) data is sent from or updated in the TXSW0-3/RXSW0-3 control registers.

When all four bytes of a Signaling Word have been received by the SSTM, the SWINT interrupt is generated and the interrupt pending RXSW bit is asserted in the IS register. Once the interrupt bit has been asserted, no new data will be loaded onto the register until the interrupt has been read (the interrupt is cleared automatically by the hardware when all four bytes are read. The bytes can be read in any order).

On the transmit side when all four bytes of a Signaling Word have been sent, the same SWINT interrupt is generated and the TXSW interrupt pending bit is asserted in the IS register. The SWINT on the transmit side will be cleared by hardware when the new four bytes of a signaling word will be loaded into the TXSW control register (they can be loaded in any order).

If there are less than four bytes to be sent, the registers shoud be loaded anyway. All “0”s can be used or any protocol can be defined by the user.

It should be noted that the SWINT is multiplexed. To find which service phase (transmit or receive) generated the interrupt, the IS (interrupt status) register should be read when the SWINT interrupt is generated.

If a signaling word is not read when received, or it is not written for transmission, the SWINT will not be cleared by hardware. In this case there is no inducation that a signaling word on the trasmit side is sent, or if a signaling word on the receive side is received, accordingly. The user can synchronize the SW read/write procedures by using the SWINT interrupt enable feature.

The SWINT interrupt enable is controlled by the ESWINT bit of ISE1. If the interrupt generations is disabled by the ESWINT, no interrupt will be generated neither by the receive side, nor by the transmit side.

10.8.3 Read the S/N Ratio

The S/N data is calculated from the AGC circuit inside the SSTM once every 128 data bits (including overhead bits). Once a S/N value has been received by the SSTM, the SNINT interrupt is generated and the S/N interrupt pending bit is asserted in the IS register. The interrupt will be cleared by hardware and a new S/N data will be written into the register when a S/N data is read.

The SNINT interrupt enable is controlled by the ESNINT bit of ISE1.

10.8.4 Error Detection and Control

The error detect and control block, provides one bit parity check for each byte of the voice data. The block consists of NSCTRL control register, NSVAL data register, and PERRCNT data register.

The transmit side adds one parity check bit to each byte, thus for 160 bits transmitted in one frame, 20 bits are added. The receive side checks if there is a parity check error and applies predefined by the user erroro control mode.

The NSCTRL register controls the modes as follows:

- When NSCTRL[0] set to “1”, the block is enabled. Reset value is “0” - disabled.
- When NSCTRL[1] set to “0”, the Mode 0 is enabled. Otherwise the Mode 1 enabled.

When the block is disabled, all bytes, error or no error, go directly to the codec.

The block, when enabled, provides two error control modes:

- Mode 0. In this mode each nibble of the erroniously received byte is replaced by the last nibble received without error;
- Mode 1. In this mode the erroneously received byte is replaced by the byte from the NSVAL data register. If there is no data written into the NVSAL, all “0” will be sent to the codec.

The PERRCNT register provides a value of the parity errors counter. This counter is reset to “0” by hardware at the end of the transmit phase. The counter counts all parity check errors during the receive phase. It can be read at any time.

10.8.5 SSTM Parameters

In the following, a brief discussion on programming the SSTM for the various modes of operation is presented.

The programming of the PLSL, CNTLR, ACC1RES, and WSL depend on several environmental and system related factors. For example, the sizing of PLSL and CNTLR windows involves trade-off considerations in the PLL’s dynamic performance. In general, if smaller window size is used, the PLL will behave as if it has a smaller loop bandwidth with higher noise filtering but at the expense of slower dynamic response. If larger window size is used, the PLL will respond quicker dynamically but its performance will be degraded because more noise is allowed to enter the system. ***Please note that the width of the Central Zone must be smaller than or equal to the size of the ESD window*** (this means that the ESD window size should NOT be set to 8, it was included on the chip for testing purpose only).

Similarly, the width of the detection window, WSL, should be large enough to take advantage of multipath combining but should not be so large that excessive noise is allowed into the receiver causing receiver sensitivity degradation. In general, these parameters can be experimentally optimized for a particular environment. Otherwise, it is recommended that these parameters be programmed to values in the middle of the

programmable range (for example, set PLSL to 12 samples wide, CNTLR to 10 samples wide, and WSL to 8 samples wide).

In the full-duplex or TDD mode, ACC1RES should normally be set to “0” for no ACC1 reset during each “freeze PLL” period. The only instance where ACC1RES should be set “1” to reset ACC1 is if the frequency offset between the transmitter and receiver is known to be very small. In this case, the performance of the PLL will be slightly enhanced if ACC1 is reset during each “freeze PLL” period.

CI_h[0] is used to set the SSTM to be either a master or a slave. Typically the unit that initiates the signalling process should be programmed to become the master.

The number of allowable errors in UW depends on the application. For example, applications that can tolerate a larger BER can usually allow more UW errors while still maintaining a reasonable communication link as in the case of voice applications.

Finally, CI_h[4] enables or disables the Locking State Machine. The locking state machine when used in conjunction with the programmable allowable UW errors gives the system designer the flexibility to tailor the SSTM for a particular operating environment. Typically, by enabling the Locking State Machine and by allowing more UW errors, the SSTM will continue to operate normally even in a marginal communication link channel without repeatedly loosing lock and going into acquisition. The disadvantage is the corresponding increase in the data errors; for some critical applications, this might not be tolerable. In this case, the number of allowable UW errors can be reduced and the locking state machine turned off.

11. Voice Module

11.1. General

The voice module is a single channel ADPCM Codec incorporating a sigma-delta PCM codec filter complying with G.721 and G.726 standards. In addition, this module also meets the PCM conformance specification of the G.714 recommendation.

The ADPCM CODEC is a low power, full duplex telephony CODEC with inte-grated ADPCM compression and decompression. A tone generator and voice/silence detection circuit are also integrated.

Features

- ADPCM Algorithms – G.721 (32kbps), G.723 (24kbps) G.726 (16kbps). G.711-PCM
- Built in DTMF transmitter with various single tone options
- Built in VOX control, voice detect and back-ground noise generation
- Built in microphone amplifier and sounder driver
- Programmable transmit, receive and sidetons gain controls

11.2. Control Registers

The nine control registers are used to contro the voice module. One control register (VMINTCR) is for the control of the voice activity detection, reset/power down and to cofigure the SIO module to control the codec control registers. The eight control registers in the codec are programmable through the Serial I/O module. The Serial I/O module should be configured to control the Voice Module by the setting the Bit0 in SFR VMINTCR to 1.

The power down state and reset is controlled by the VMRESETN bit (Bit 1). Control registers are reset to initial states. The power down state is controlled as a logical OR with Control bit CR0-B5.

All control registers are set to their default state upon a hardware reset. Initial values after reset are all zero's except for some bits of CR2. Reserved or unused bits of Control registers should be set ot 0.

11.2.1 VMINTCR Description

	Bit7	Bit6	Bit5-Bit2	Bit1	Bit0
	VOXI	VOXO	Reserved for Future Use	VMRESETN	DEN
Value after reset	0	0	0	1	0
	R/W	R	R	R/W	R/W

TABLE 9.

Bit 7 -- VOXI - Logic control for receive voice detection. Should be set by software. A "0" at this pin will generate background noise into the receive path if control bit CR6-B3 is set to "0". The background noise amplitude is set by CR6.

Bit 6 -- VOXO - Voice detection logic output signal. The signal is generated by the codec hardware. The "1" and "0" values indicate the presence, or absence, of the transmit voice signal. The detection threshold is set by CR6-B6,B5.

Bit 1 -- VMRESETN - Power down and reset. The signal is generated by hardware from the NRESET pin status. Control registers are reset to initial values. The power down state is controlled as a logical OR with control bit CR0-B5.

Bit 0 -- DEN - DEN value for Codec interface. Writing "1" will enable the voice interface between SIO and codec. Writing "0" will make SIO be a general purpose SIO.

Bit 2 to Bit 5 are reserved for future use.

11.2.2 Codec Eight Control Registers Index Table

TABLE 10. *Control Registers Index*

Name	**A2**	**A1**	**A0**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**R/W**
CR0	0	0	0	A/μ SEL		PDN all	PDN TX	PDN RX			PDN SAO/ AOUT	R/W
CR1	0	0	1	Mode1	Mode 0	RESET					RX PAD	R/W
CR2	0	1	0	TX ON/ OFF	TX GAIN 2	TX GAIN 1	TX GAIN 0	RX ON/ OFF	RX GAIN 2	RX GAIN 1	RX GAIN 0	R/W
CR3	0	1	1	SIDE TONE GAIN 2	SIDE TONE GAIN 1	SIDE TONE GAIN 0	TONE ON/ OFF	TONE GAIN 3	TONE GAIN 2	TONE GAIN 1	TONE GAIN 0	R/W
CR4	1	0	0	DTMF/ ALT SEL	TONE SEND	SAO/ AFRO	TONE 4	TONE 3	TONE 2	TONE 1	TONE 0	R/W
CR5	1	0	1		PCM RX MUTE	PCM TX MUTE						R/W
CR6	1	1	0	VOX ON/ OFF	ON LVL 1	ON LVL 2	OFF TIME	VOX IN	RX NOISE LVL SEL	RX NOISE LVL1	RX NOISE LVL 0	R/W
CR7	1	1	1									

11.2.3 Eight Control Registers Description

1. Control Register 0

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
A/μ SEL	RESERVED	PDN ALL	PDN TX	PDN RX			PDN SAO/ AOUT

BIT 0 0=power on, 1=Power down for sound amp outputs or receiver amps depending os state of CR4-B5.

CR0-B0	**CR4-B5**	
0	0	SA Mute, RA active
0	1	SA active, RA mute
1	0	SA power down, RA active
1	1	SA active, RA power down

SA - Sounder amplifier. RA - Receive amplifier

CR0-Bits 1, 2, 6 - Reserved. Normally zero.

CR0-B3 1 = Power down for receive only. 0= power on.

CR0-B4 1 = Power down for transmit only. 0= power on.

CR0-B5 1 = Power down for whole system. 0= power on. Thsi bit is ORed with VMRESETN bit. When using this bit for power down control, set VMRESETN=1 in the VMINTCR. The control registers are not reset by CR0-B5.

CR0-B7 PCM mode select. 1=A-law, 0=m-law.

2. Control Register 1 (ADPCM Coder/Decoder Setting)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode 1	Mode 0	Reset					RX PAD

CR1-B0 1= Analog O/P attenuated by 12dB.

CR1-B1 Reserved

CR1-B2 Reserved

CR1-B3 Reserved

CR1-B4 Reserved

CR1-B5 1=ADPCM reset

CR1-B6,B7 ADPCM algorithm selection

Mode 1	Mode 0	Algorithm
0	0	32kbps(G.721)
0	1	64kbps(G.711)
1	0	24kbps(G.723)
1	1	16kbps(G.726)

3. Control Register 2 PCM Block&Tx-Rx Gain Control Settigns

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX ON/ OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/ OFF	RX GAIN2	RX GAIN1	RX GAIN0
0	0	1	1	0	0	1	1

NOTE: Last row above, shows bit values after reset.

CR2-B0-B2 Receive gain adjustment see table below.

CR2-B3 1=Disable PCM decoder (receive PCM idle pattern). 0= enable.

CR2-B4-B6 Transmit gain adjustment see table below.

CR2-B7 1=Disable PCM coder (transmit PCM idle pattern). 0= enable.

B6	B5	B4	TRANSMIT GAIN	B2	B1	B0	RECEIVE GAIN
0	0	0	-6dB	0	0	0	-6dB
0	0	1	-4dB	0	0	1	-4dB
0	1	0	-2dB	0	1	0	-2dB
0	1	1	0dB	0	1	1	0dB
1	0	0	+2dB	1	0	0	+2dB
1	0	1	+4dB	1	0	1	+4dB
1	1	0	+6dB	1	1	0	+6dB
1	1	1	+8dB	1	1	1	+8dB

The output of the DTMF tone generator is -16dBmO for low group tones and -14dBmO for the high group and alternative tones. The gain shown above must be added to these levels to calculate the amplitude of the final output signal. For example if the +4dB setting is selected, the DTMF output at PCMSO will be equivalent to -12dBmO for the low group and -10dBmO for the high group. This applies to transmitted tones.

4. Control Register 3 Side Tone and Tone Generator Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Side Tone GAIN2	Side Tone GAIN 1	Side Tone GAIN 0	TONE ON/OFF	TONE CAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN 0

CR3-B0-B3 Tone generator gain adjustment for receive side. See table below.

B3	B2	B1	B0	TONE GENERATOR RX GAIN	B3	B2	B1	B0	TONE GENERATOR RX GAIN
0	0	0	0	-36dB	1	0	0	0	-20dB
0	0	0	1	-34dB	1	0	0	1	-18dB
0	0	1	0	-32dB	1	0	1	0	-16dB
0	0	1	1	30dB	1	0	1	1	-14dB
0	1	0	0	-28dB	1	1	0	0	-12dB
0	1	0	1	-26dB	1	1	0	1	-10dB
0	1	1	0	-24dB	1	1	1	0	-8dB
0	1	1	1	-22dB	1	1	1	1	-6dB

The output of the DTMF tone generator is -2dBmO for low group tones and 0dBmO for the high group and alternative tones. The gain shown above must be added to these levels to calculate the amplitude of the final output signal. For example if the -14dB setting is selected, the DTMF output at SAOP/SAON or AFRO will be -14dBmO for the high group and -16dBmO for the low group.

CR3-B4 1=Tone generator enable. 0=disable.

CR3-B5-B7 Side tone gain setting. See table below.

B7	B6	B5	SIDE TONE PATH GAIN
0	0	0	OFF
0	0	1	-21dB
0	1	0	-19dB
0	1	1	-17dB
1	0	0	-15dB
1	0	1	-13dB
1	1	0	-11dB
1	1	1	-9dB

5. Control Register 4

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTMF/ ALT SEL	TONE SEND	SAO/ AFRO	TONE 4	TONE 3	TONE 2	TONE 1	TONE 0

CR4-B0-B4 Tone frequency setting. See table below.

CR4-B5 Tone output pin select (receive side). 0= AFRO, 1=SAOP/SAON.

CR4-B6 Tone output pin select (transmit side). 0= Voice signal (transmit), 1=Tone signal.

CR4-B7 DTMF or alternative tones select. 1=DTMF, 0=Alternate.

(a) B7=1 DTMF Tones

B3	B2	B1	B0	TONES LOW GROUP/HIGH GROUP Hz	KEY	B3	B2	B1	B0	TONES LOW GROUP/HIGH GROUP Hz	KEY
0	0	0	0	697/1209	1	1	0	1	0	852/1477	9
0	0	0	1	697/1336	2	1	1	0	1	941/1336	0
0	0	1	0	697/1477	3	1	1	0	0	941/1209	*
0	1	0	0	770/1209	4	1	1	1	0	941/1477	#
0	1	0	1	770/1336	5	0	0	1	1	697/1633	A
0	1	1	0	770/1477	6	0	1	1	1	770/1633	B
1	0	0	0	852/1209	7	1	0	1	1	852/1633	C
1	0	0	1	852/1336	8	1	1	1	1	941/1633	D

(b) B7=0 Alternative Tones

B4	B3	B2	B1	B0	F	B4	B3	B2	B1	B0	F
0	0	0	0	0	1K/ 1333Hz, 16Hz	1	0	0	0	0	2500Hz
0	0	0	0	1	800/1KHz, 16Hz mode	1	0	0	0	1	2600Hz
0	0	0	1	0	800/1KHz, 8Hz mode	1	0	0	1	0	2670Hz
0	0	0	1	1	400Hz, 16Hz mod	1	0	0	1	1	2700Hz
0	0	1	0	0	2700Hz, 16Hz mode	1	0	1	0	0	2800Hz
0	0	1	0	1	400Hz	1	0	1	0	1	2910Hz
0	0	1	1	0	800Hz	1	0	1	1	0	3000Hz
0	0	1	1	1	1KHz	1	0	1	1	1	3110Hz
0	1	0	0	0	1333Hz	1	1	0	0	0	3200Hz
0	1	0	0	1	1440Hz	1	1	0	0	1	
0	1	0	1	0	1900Hz	1	1	0	1	0	

B4	B3	B2	B1	B0	F	B4	B3	B2	B1	B0	F
0	1	0	1	1	2000Hz	1	1	0	1	1	
0	0	1	0	0	2100Hz	1	1	1	0	0	
0	0	1	0	1	2180Hz	1	1	1	0	1	
0	0	1	1	0	2300Hz	1	1	1	1	0	
0	0	1	1	1	2400Hz	1	1	1	1	1	

6. Control Register 5

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PCM RX MUTE	PCM TX MUTE					

CR5-B0-B4 Test Control pins Must be zero for normal operation.

CR5-B5 1=Mute RX PCM signal at PCM decoder.

CR5-B6 1=Mute TX PCM signal at PCM coder.

CR5-B7 Reserved.

7. Control Register 6. VOX Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LVL SEL	RX NOISE LVL1	RX NOISE LVL0

CR6-B1-B0 Background noise amplitude setting. See table below.

RX NOISE LVL1	RX NOISE LVL0	RX NOISE POWER
0	0	NO NOISE
0	1	-55dBmO
1	0	-45dBmO
1	1	-35dBmO

CR6-B2 Rx Background noise amplitude setting.1=programmable using B1, B0. Do not clear this bit.

CR6-B3 Receive VOX function. 0=background noise transmit, 1=voice signal transmit. To use this

data, set VOXI to zero.

CR6-B4 Hang over time. 1=320ms, 0=160ms. (T VXOFF , Fig 5.)

CR6-B5,B6 Select Transmit signal energy detect (transmit VOX) threshold. See table below.

ON LVL1	ON LVL0	TX VOX TRESHOLD
0	0	-30dBmO
0	1	-35dBmO
1	0	-40dBmO
1	1	-45dBmO

CR6-B7 VOX function enable. 0=disable. 1=enable

8. Control Register 7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VOXO							

CR7-B0-B4 Factory test control pins. Must be zero for normal operation.

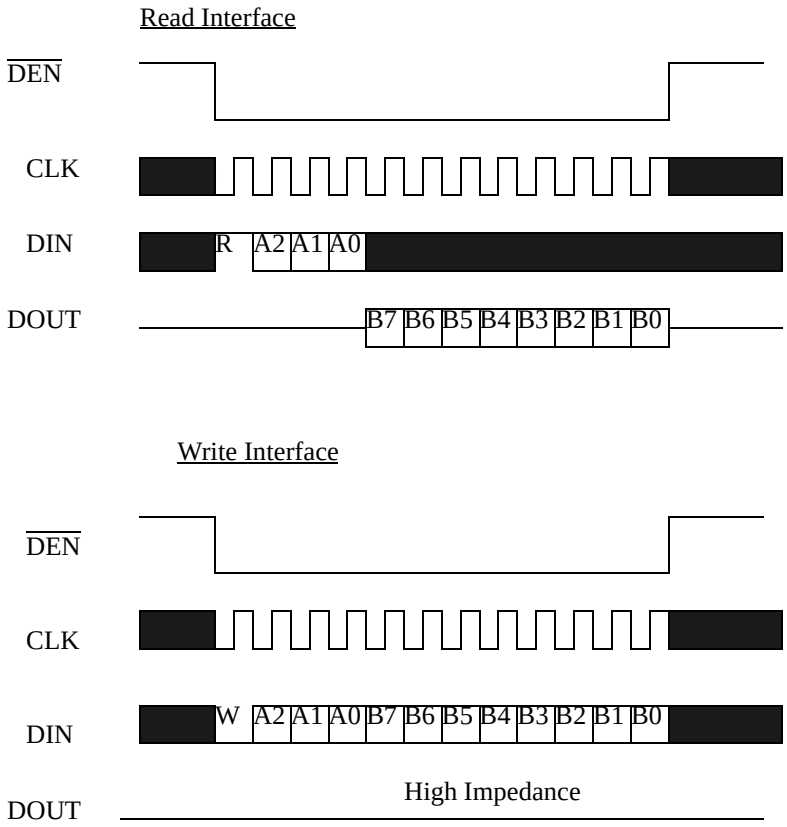
CR7-B5-B6 Reserved.

CR7-B7 Transmit VOX (VOXO) status bit. Same as VOXO bit of VMINCR.

NOTE: 0dBmO = -7.7dBm(600Ω)

11.3. Serial Interface to the Eight CRs

The following figure shows the timing for the serial interface to the eight control registers in the Voice Module. The SIO block of SS1103 is used to program the codec registers. The SIO block is configured to interface the Voice Module by the setting the DEN bit of VMINTCR to “1”. When the SIO block is configured to program the Voice Module, the SIO block is not available for the external circuits.



11.4. Voice Analog Circuits Interface

The voice analog input and ouptuts of the SS1103 are designed to provide flexibility for use with different telecom systems. Figure below shows the typical connections to other applications.

The follwing calculations provides values for the components:

Receive Gain: Vo/Vafro=2x(R6/R5)

Transmit Gain: Vxga2/Vin=(R2/R1)x(R4/R3)

Note: Transmit path referes to the upper portion of block diagram (with the ADC) and the Receive path referes toe the lower position (with DAC).

The voice interface circuits are shown on Figure 1.

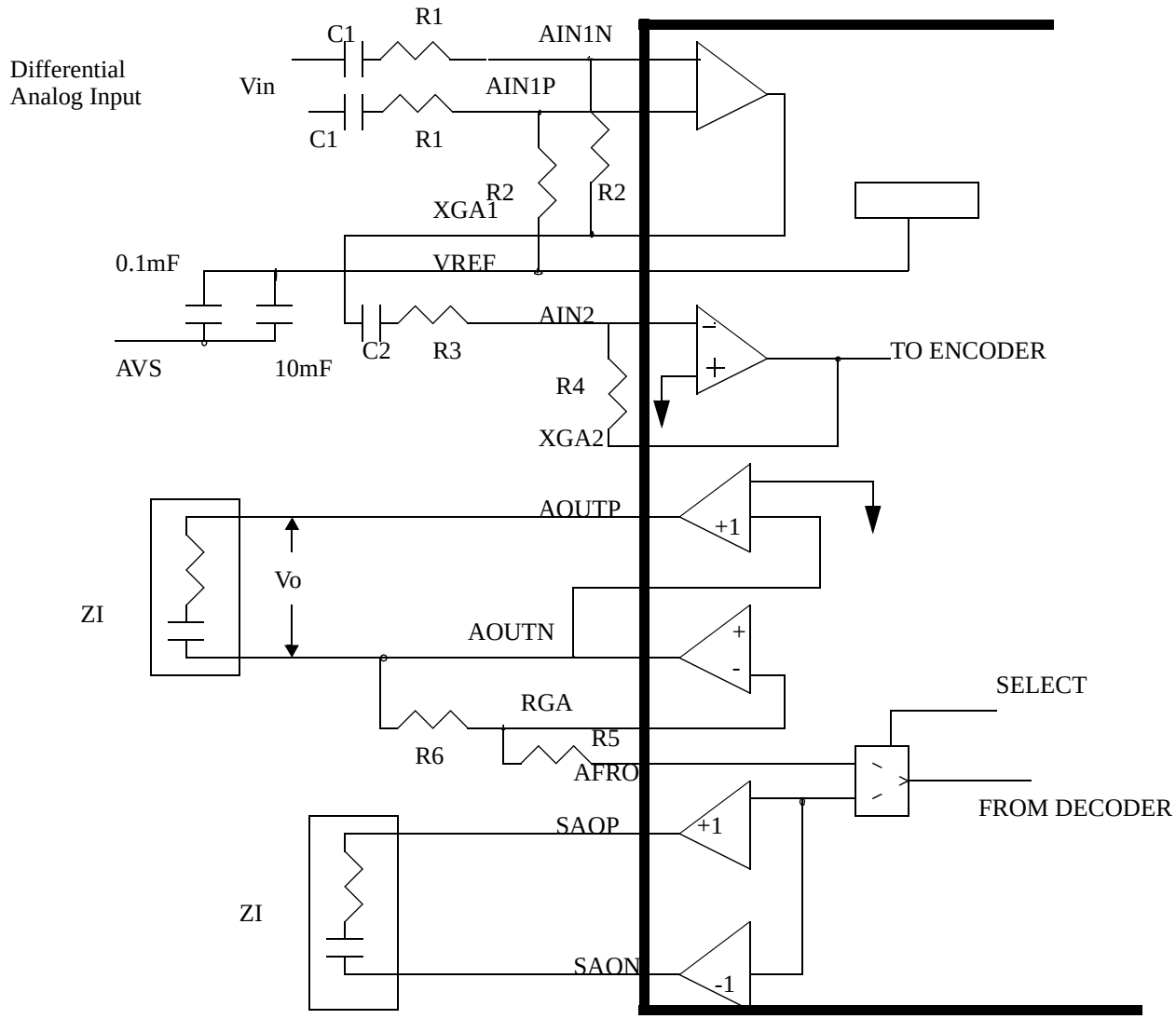


Figure 1. *Voice Analog Interface Circuits*

11.5. Reset and Power Down

The total RESET and Power Down modes of the Voice Module are controlled by the NRESET pin of SS1103, by the VMRESET bit of VMINTCR, and by the PDN ALL bit of CR0 (CR0-B5 bit).

There are also power down modes for the TX, RX and SAO circuits. These modes are controlled by the bits in the CR0. The functions of these bits are described in the Control Register 0 section of the spec.

The NRESET pin is an active low pin. On the power-on the NRESET pin resets the chip. When the NRESET value goes high, the value of the VMRESETN bit goes high, also. All control registers are reset to their reset value.

After power-on reset, the Voice Module can be put into the power down state without resetting the control registers values. The CR0-B5 bit should be set to 1to power down the Voice Module without the resetting the CRs.

If there is a requirement to put the Voice Module into the power down state and to reset the control registers values, the VMRESETN bit should be set to 0. The 0 value of the bit can be changed to 1 by setting it to 1 by the software, or by the resetting the SS1103 by the NRESET pin. To power down the Voice Module by the CR0-B5 bit, the VMRESETN value should be set to 1.

The NRESET pin low always (even if the VMRESETN bit is high) resets the Voice Module and sets the control registers values to the reset values.

The reset values for the contol registers bits all zero's with the exeption for:

- VMRESETN
- CR2-B5,B4,B1,B0

The reset values for these bits are 1.

11.6. VOX system

11.6.1 General

VOX system provides for the user the ability to control the transmit and receive paths of the codec. The control is based on the presence or absence of a voice on the path. The VOX function can be enabled by setting the CR6-B7 bit to 1. When the CR6-B7 is set to "0", the voice signal is transmitted through and VOXO is high.

When the CR6-B7=1, the VOXO bit of VMINTCR presents the presence of voice (the same value of the VOXO is provided by CR7-B7 bit). The bit is high when the detected by the codec logic voice signal level is higher than a threshold. It is low, when a voice signal level is lower then the threshold. The threshold value for the detection is defined by CR6-B6,B5.

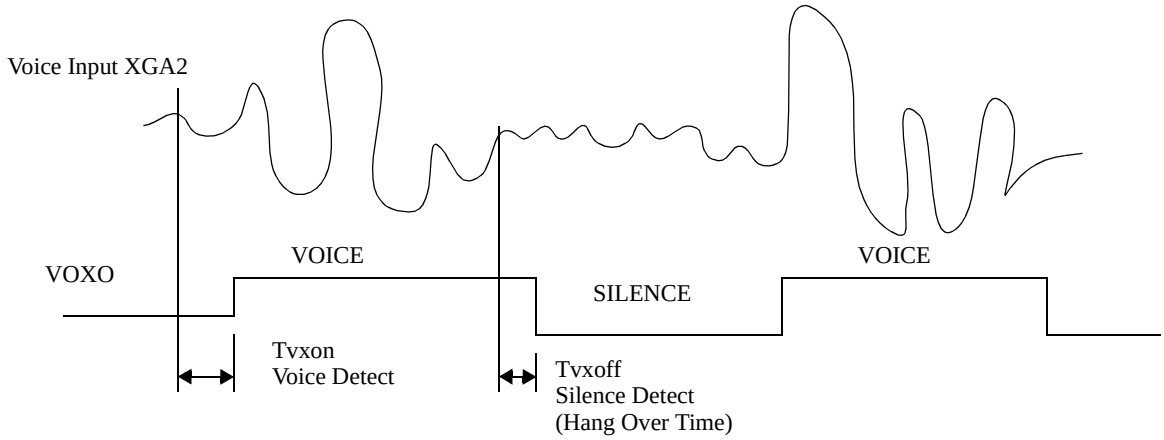
The VOXI bit of VMINTCR controls the receive path of the codec. When set to "1", the received voice signal is transmitted to the output analog circuits.

When the VOXI bit is set to "0", the codec logic will transmit the background noise to the output analog circuits if the CR6-B3 is set to "0". The codec logic will transmit the received voice signal to the output analog circuits if the CR6-B3 is set to "1".

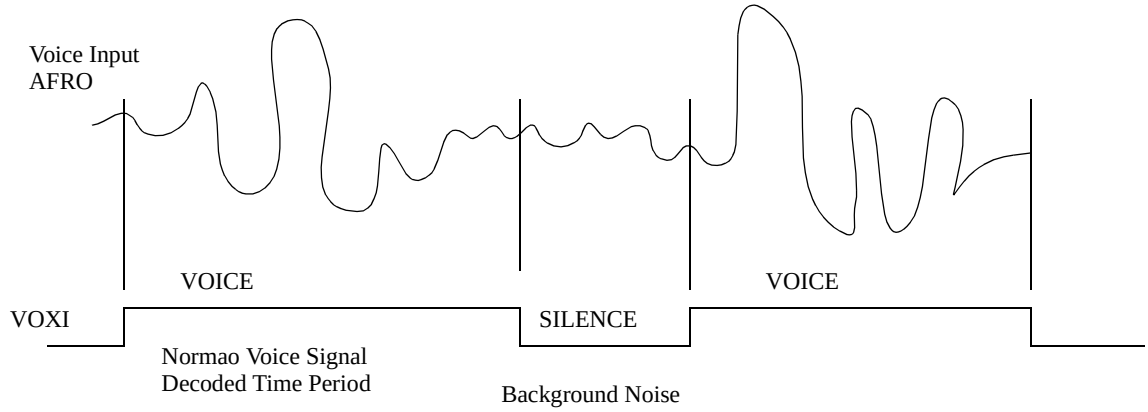
11.6.2 AC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max ‘	Unit
Tvxon	Transmit VOX detect time	off - to - on		5		mS
Tvxof	Transmit VOX detect time	on - to - off		160/ 320		mS
Dvx	VOX detected level accuracy	CR6-B6,B5	-2.5	0	+2.5	dB

Transmit VOX function timing



Receive VOX function timeing (CR6-B3=0)



12. RF Modue Interface

12.1. SSTM RF Interface

The SSTM interfaces with the RF/IF analog radio through the following pins: DI, MODOUT, PLLSW, and RFPWR.

Also, two interrupts, PLLSWPEINT and PLLSWNEINT, provide an identification of the start of the transmission phase and the end of the transmission phase (begining of the receiving phase). The PLLSWPEINT interrupt bit of INT2 register is set by the rising edge of the PLLSW signal and it is cleared by software. The PLLSWNEINT interrupt bit of INT2 register is set by the falling edge of the PLLSW signal and it is cleared by software.

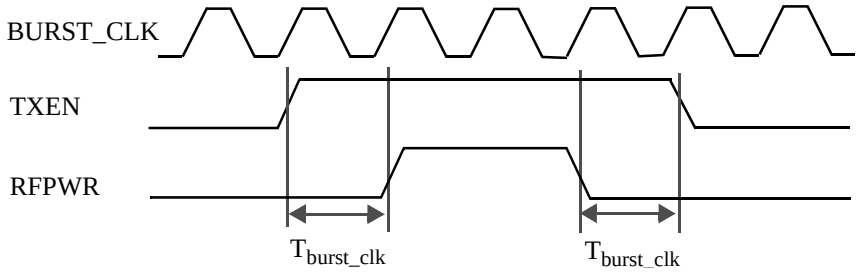
DI is a CMOS-level input fed by the RF receiver. The signal can be configured as an external input (bit 0 of CMPRCR set to 0) or connected to the output of internal comparator (bit 0 of CMPRCR set to 1).

MODOUT is a tri-state output to the RF transmitter. It is in high-impedance state when the SSTM is in the receive mode (TXEN is LO). PLLSW and RFPWR are used respectively to switch the PLL of the analog radio and to power on/off the transmitter power amplifiers. The timings for the RFPWR and PLLSW are shown in Figure 5 and Figure 6 respectively.

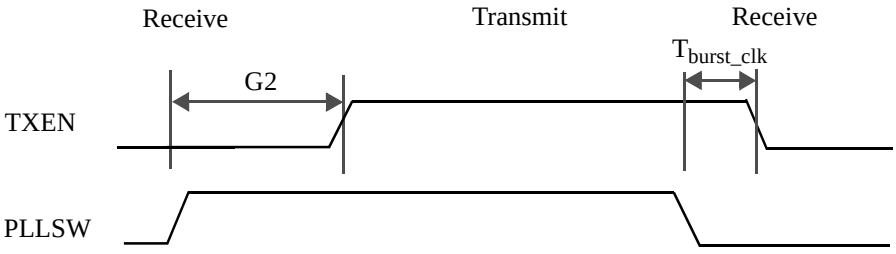
The RFPWR switch timing is designed to avoid damage to the sensitive analog receiver. When switching from receive to transmit, RFPWR is delayed relative to TXEN (which can be used for switching the antenna between transmit and receive chain) to ensure that the receiver has been turned off before the transmitter is turned on. Similarly, when switching from transmit to receive, RFPWR is turned off first, before TXEN, to allow extra time for the transmitter to turn off prior to turning on the receiver circuits.The BURST_CLK shown in Figure 5 is the burst rate clock which depends on the frequency of the fast oscillator. For example, for the oscillator of 16.384 MHz, the burst rate is 85.333 KHz. Thus, the RFPWR signal will be asserted one burst clock cycle or 11.72 μsec after TXEN assertion and will be de-asserted one burst clock cycle or 11.72 μsec prior to TXEN de-assertion.

The PLLSW signal is designed to switch the RF PLL when different frequencies are used for transmit and receive operation. In this instance, PLLSW is turned on right at the end of receive operation and prior to TXEN assertion to allow the RF PLL to stabilize. Similarly, the PLLSW changes to a LO as soon as transmission is finished and before receiving commences.

The PLLSW is asserted 28 burst clock cycles (duration of G2) prior to TXEN assertion and is de-asserted 1 burst clock cycle before TXEN is de-asserted in the full-duplex mode. Thus, for a master oscillator of 16.384 MHz (corresponding to a burst rate of 85.333 KHz or a burst period of 11.72 μsec), the PLLSW signal will be asserted 328 μsec (28*11.72=328) prior to TXEN assertion.



RFPWR Timing



Note: G2=28xT_{burst_clk} Not drawn to scale.

PLLSW Timing (Full-Duplex Mode)

12.2. Gain Control Module (GCM)

12.2.1 Overview

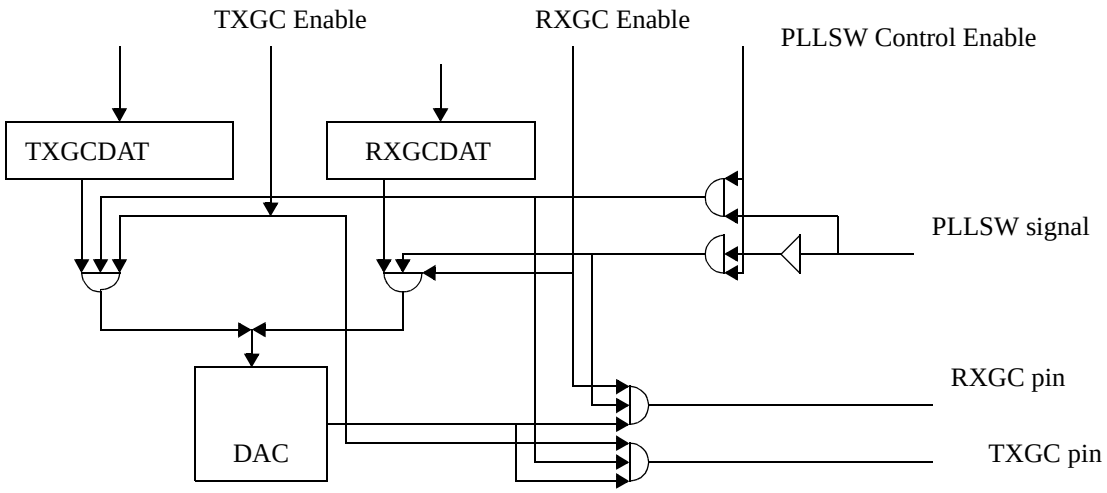
The module provides analog signals to control the gain circuits of RF module. The module includes the 8-bit digital-to-analog converter. The converter's output is demultiplexed to the two output pins - TXGC and RXGC. Two control registers TXGCDAT and RXGCDAT are used to control values of the analog signals on the TXGC and RXGC pins, accordingly.

The module operates in three modes: TXGC only, RXGC only, and TXGC and RXGC controlled by the PLLSW signal. The modes are configured by the bit2, bit1, and bit 0 , accordingly, of the GCMCR register.

The last mode provides user with ability for the fast switching. This mode does not require the CPU to write the DAC value for each frame, thus the user can keep the CPU in one of the power saving modes.

The RXGC and TXGC pins in the idle mode (when there are not used) is tied to the analog ground.

The block diagram of the module is shown on Figure below.



12.2.2 Digital to Analog Converter Specification

Parameter	Min	Typ	Max	Units
Resolution		8		bits
Integral Non-Linearity		1		LSB
Differential Non-Linearity		0.5		LSB
Settling Time		100		ns
Zero Error at 25^0 C		0.004		LSB
Full Scale Error at 25^0 C		0		LSB
VREF Input Resistance		84.2		Kohms
VREFP Range		AVD		V
VREFN Range		AVS		V

12.2.3 Gain Control Module Control Register

Bit/Name	7	6	5	4	3	2	1	0
CMPCR	-	-	-	-	-	TXGCEN	RXGCEN	PLLSWEN
	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Address: 93H

Bit7 - Bit3 Reserved. These bits always read "0".

TXGCEN Transmit Gain Control Enable. Writing a "1" to this bit enables the D-to-A conversion of the 8-bit data contained in register TXGCDAT.

RXGCEN Receive Gain Control Enable. Writing a "1" to this bit enables the D-to-A conversion of the 8-bit data contained in register RXGCDAT.

PLLSWEN PLLSW Enable. When this bit is enabled the source for the D-to-A conversion is controlled by the state of the PLLSW pin. When PLLSW is a "1", TXGCDAT is converted while when PLLSW is a "0", RXGCDAT is converted.

Transmit Gain Control Data

Bit/ Name	7	6	5	4	3	2	1	0
TXG-DAT	Dat7	Dat6	Dat5	Dat4	Dat3	Dat2	Dat1	Dat0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Address: 93H

Dat7-Dat0 Transmit Contro Data bits.

Bit/ Name	7	6	5	4	3	2	1	0
RXG-DAT	Dat7	Dat6	Dat5	Dat4	Dat3	Dat2	Dat1	Dat0
	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Address: 94H

Dat7-Dat0 Receive Gain Control Data bits

12.3. RSSI ADC Module

12.3.1 Overview

The receive signal strength indicator (RSSI) determines the value of the RSSI analog input pin, representing the level of the received RF signal. The module includes a 10-bit

successive approximation A/D converter requiring approximately 14 clock frequency cycles for conversion. The clock frequency is 2 Mhz.

The input is a high impedance, so the RSSI level may be developed across an external resistance driven by a current source.

The Module controlled by setting of ADCCR register. When the ADC module is enabled the converted value is returned in ADCDAT. Hardware signifies the end of the conversion by setting the bit 2 in the ADCCR. The software should poll this bit to read the RSSI value.

The RSSI output voltage range is the power supply rail-to-rail range.

12.3.2 ADC Control Register

Bit/ Name	7	6	5	4	3	2	1	0
ADCCR	Dat1	Dat0	-	-	-	RDY	ST	EN
	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Address: A3H

Dat1-Dat0 ADC Data. These two bits are the two LSB's of the latest 10-bit analog to digital conversion.

RDY Ready. This bit indicates the end of the A-to-D conversion sequence.

Bit5-Bit 3 Reserved. These bits always read "0".

ST Start. Writing a "1" to this bit initiates teh A-to-D conversion sequence. Hardware will reset this bit to a "0" after the conversion is initiated.

EN Enable. This bit enables the ADC. Writing a "0" to this bit disables the ADC and cuts the power of this block to zero.

12.3.3 ADC Data Register

Bit/ Name	7	6	5	4	3	2	1	0
ADC-Dat	Dat9	Dat8	Dat7	Dat6	Dat5	Dat4	Dat3	Dat2
	R	R	R	R	R	R	R/W	R/W

Bit/ Name	7	6	5	4	3	2	1	0
Reset Value	0	0	0	0	0	0	0	0

Address: A4H

Dat9-Dat2 ADC data. These 8 bits are the eight MSB's of the latest 10-bit analog to digital conversion.

12.4. DI Comparator

12.4.1 General Information

The DI comparator provides 1 bit AD conversion of the analog output of the RF module.

If the RF module has a slicer, the DI input of SS1103 should be used to input the digital data from the slicer.

12.4.2 Functional Description

The comparator is a a rail to rail, single supply comparator. It is also high speed and low power. In this comparator, both inputs can change. It has the following features:

supply voltage (Vdd)	3.0 V and 3.6 V
conversion time	200 nS
input offset voltage	10 mV
current usage (in active mode)	1 mA max. for 3.3V
current usage (in sleep mode)	negligible
input voltage range	0 to supply voltage
output voltage range	rail to rail
temperature range	0 - 70

TABLE 11. *DI Comparator features*

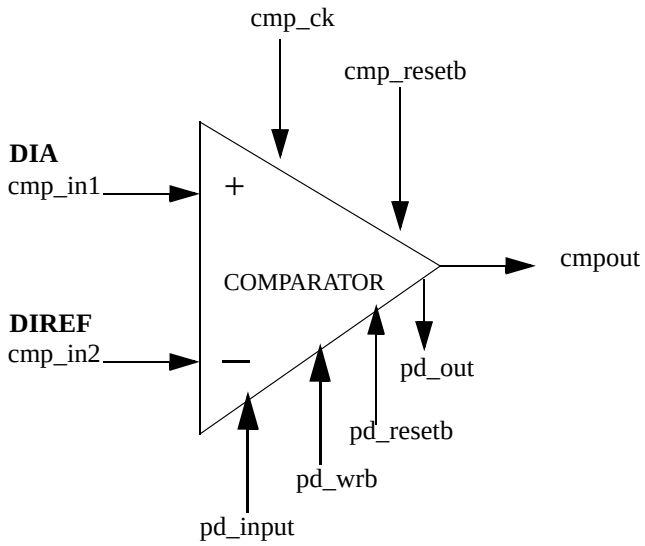


Figure 2. *DI Comparator block diagram*

12.4.3 Comparator I/O signal names and descriptions

PIN NAME	SIGNAL	DESCRIPTION
VDDA	input	Positive power supply
VSSA	input	Ground
CMP_IN1	input	Positive input to the comparator (DIA pin)
CMP_IN2	input	Negative input to the comparator (DIREF pin)
CMP_CK	input	Clock signal to generate different phases for comparator’s operation
CMP_RESETB	input	Reset signal for the comparator’s output register
PD_INPUT	input	Power-down signal to put the comparator in the sleep mode
PD_WRB	input	Write signal for the power-down register
PD_RESETB	input	Reset signal for the power-down register
PD_OUT	output	Output of pd register
CMPOUT	output	Output of the comparator

12.4.4 Timing diagrams

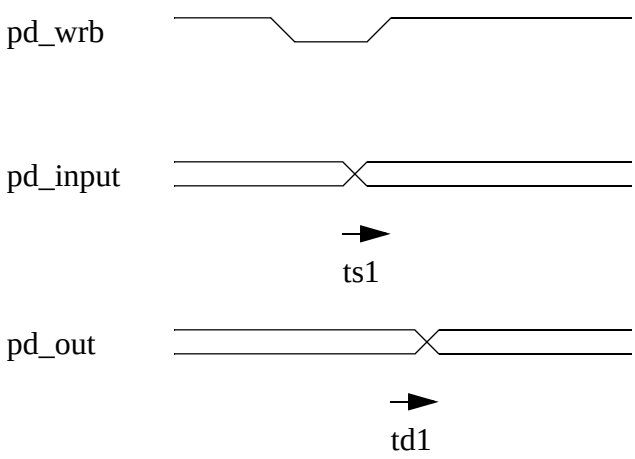


Figure 3. *Power-down register timing*

ts1 = set up time for pd_input =1 nS

td1 = delay time from pd write signal to output = 1.5 nS

When pd_out goes high, the comparator goes into power down (sleep) mode.

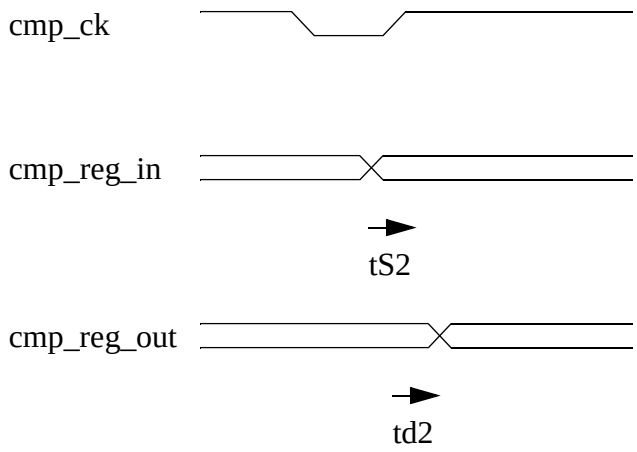


Figure 4. *Comparator output register timing*

tS2 = set up time from input to cmp_ck = 1 nS

td2 = delay time from cmp_ck to output = 1.5 nS

When the signal cmp_ck goes high, the comparator output is read and it also starts the next comparison cycle, the outcome of which is read at the next rising edge of cmp_ck.

12.4.5 Comparator I/O plot

The following shows a plot of cmpout with respect to cmp_in1, if cmp_in2 is kept constant at 2.5 V.

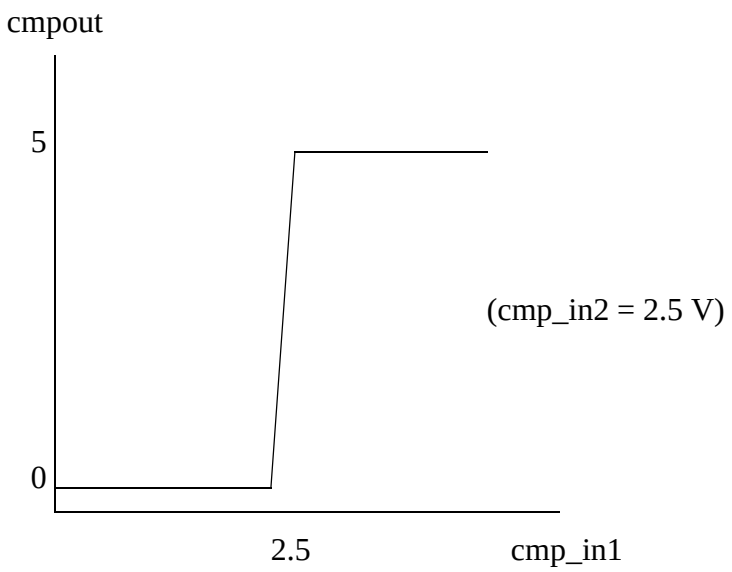


Figure 5. *DI Comparator plot*

12.4.6 Comparator Control Register

Bit/Name	7	6	5	4	3	2	1	0
CMPCR	-	-	-	-	-	CMPOUT	DSEL	EN
	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Address: 85H

Bit7 - Bit3 Reserved. These bits always read "0".

CMPOUT Comparator Output. This bit shows the status of the Comparator output.

DSEL Data Select. When this bit is set to "1" the data to the SSTM is the Comparator output. When this bit is set to "0" the input is from the DI (digital) pin.

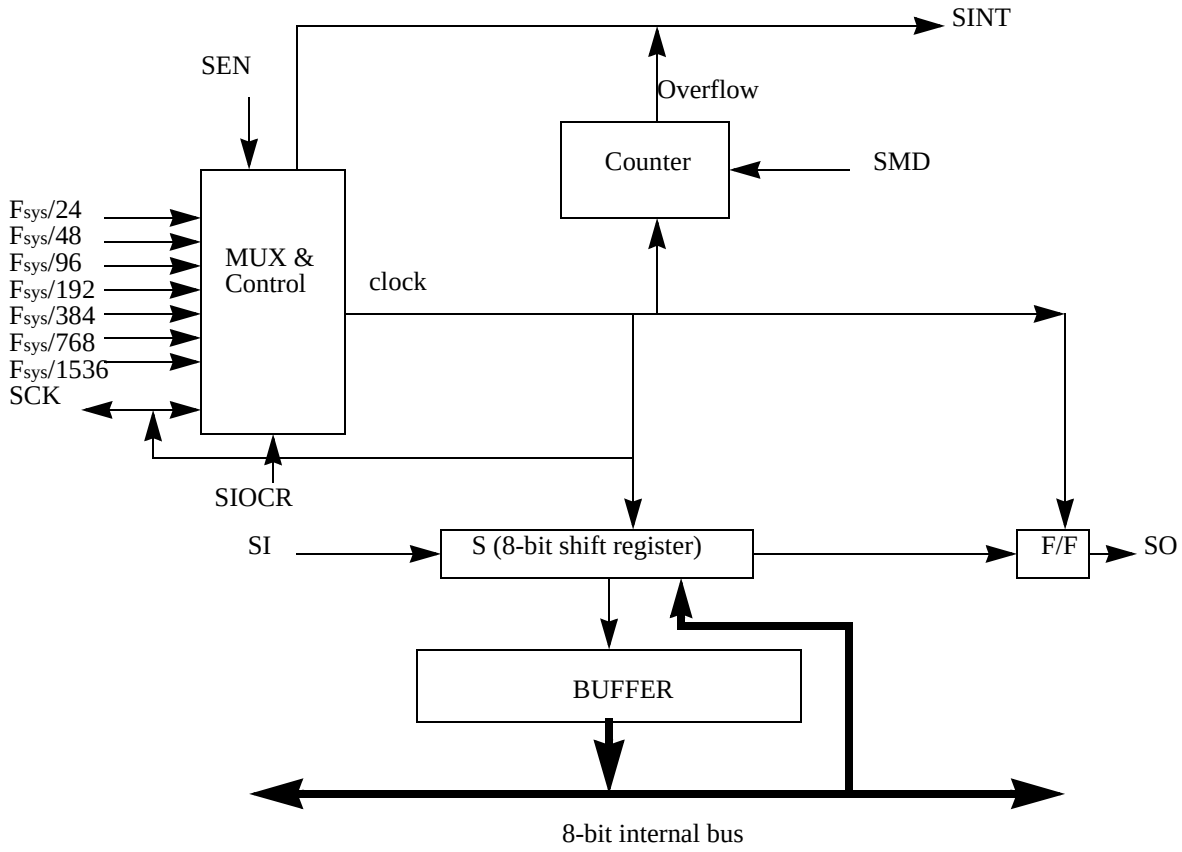
EN Enable. Writing a "1" to this bit enables the Comparator. Writing a "0" to this bit disables the Comparator and cuts the power to zero.

13. Serial I/O Module

13.1. Overview

There is the 8-bit SIO (Serial In-Out) Module the SS1103. The SIO can be used as a 8-bit serial-in, 8-bit serial-out, and 8-bit serial-I/O. SIO is receive buffered, meaning it can commence reception before a previously received data has been read from the register. (However, if the data still hasn't been read by the time reception of the next data is complete, one of the data will be lost). The SIO is composed of an input frequency select MUX and control, an up-counter, a 8-bit shift register, a 1-bit flip-flop for serial output synchronization, a control register (SIOCR), and a buffer. The SIO Module is controlled also by the DEN bit in VMINTCR of the Voice Module. The SO, SI, and SCK pins can be configured as GPIO pins by programming the P3.3, P3.4, and P3.5 bits of the P3 port.

[SIO (8-bit) Block Diagram]



13.2. 8-bit Serial-Output Mode

[Table: Control Bits of SIOCR for 8-bit Serial-Output Mode]

Control Bit	SOOE (bit-1)
Content	1

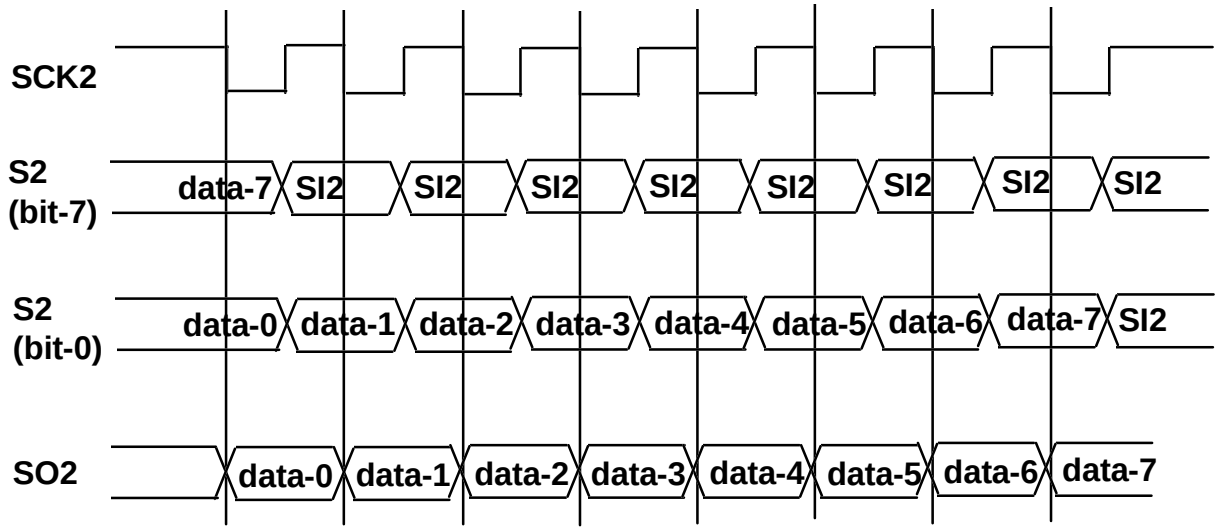
[Table: Pin Configuration of SIO for 8-bit Serial-Output Mode]

Pin	In/Out Mode	Note
SI	Serial input	The I/O mode of the pin is decided by a port control register.
SO	Serial output	SOOE = 1
SCK (SFS[2:0] = ‘000’)	SCK input mode	The pin SCK should be assigned as input mode by the port control register.
SCK (SFS[2:0] = ‘1 or 1 or 1’)	SCK output mode	The pin SCK is assigned as the SCK output pin automatically by the SFS[2:0].

[Table: Shift Registers of SIO for 8-bit Serial-Output Mode]

Shift Register	S
Operation	The MSB (bit-7) is connected to SI. The SI input signal should be synchronized to negative edge of the SCK if it needed. The S should be loaded with 8-bit data to be serial output before operation. The LSB(bit-0) is connected to the output flip-flop. The flip-flop is connected to the SO pin. The shift operation is performed on positive edge of the SCK. The SO output synchronized to the just next negative edge of the SCK. After 8-bit shift, S will have new content from SI pin.

[SO(Serial-Output) Mode: SIO-2]



13.3. 8-bit Serial-Input Mode

[Table: Control Bits of SIOCR for 8-bit Serial-Input Mode]

Control Bit	SOOE (bit-1)
Content	0

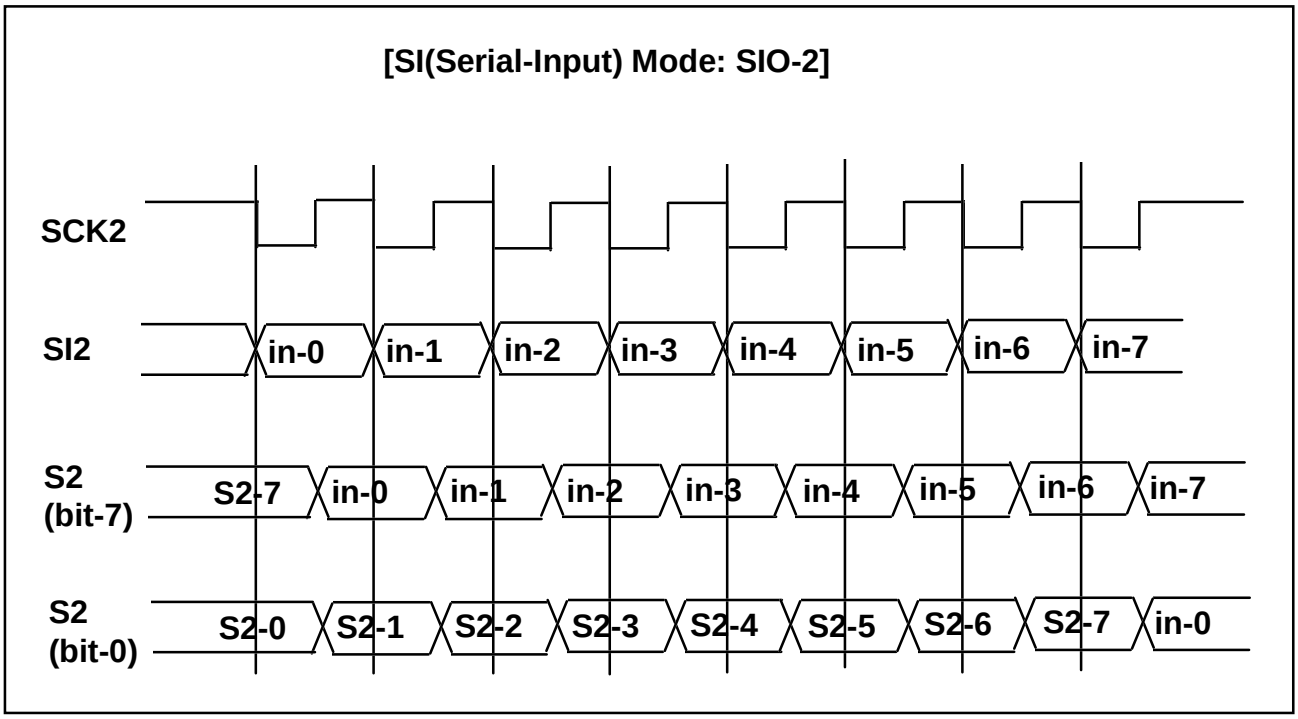
[Table: Pin Configuration of SIO for 8-bit Serial-Input Mode]

Pin	In/Out Mode	Note
SI	Input Mode	The pin SI must be assigned to input mode by a port control register.
SO	Normal Port	SOOE = 0. This pin can be used as a normal input or output port.

SCK (SFS[2:0] = ‘000’)	SCK input mode	The pin SCK should be assigned as input mode by the port control register.
SCK1 (SFS[2:0] = ‘1 or 1 or 1’)	SCK output mode	The pin should be assigned as output mode by the port control register

[Table: Shift Registers of SIO for 8-bit Serial-Input Mode]

Shift Register	S
Operation	The MSB (bit-7) is connected to SI. The SI input signal should be synchronized to negative edge of the SCK. The shift operation is performed on positive edge of the SCK. After 8-bit shift, the S will have 8-bit serial input data.



13.4. 8-bit Serial-I/O Mode

[Table: Control Bits of SIOCR for 8-bit Serial-I/O Mode]

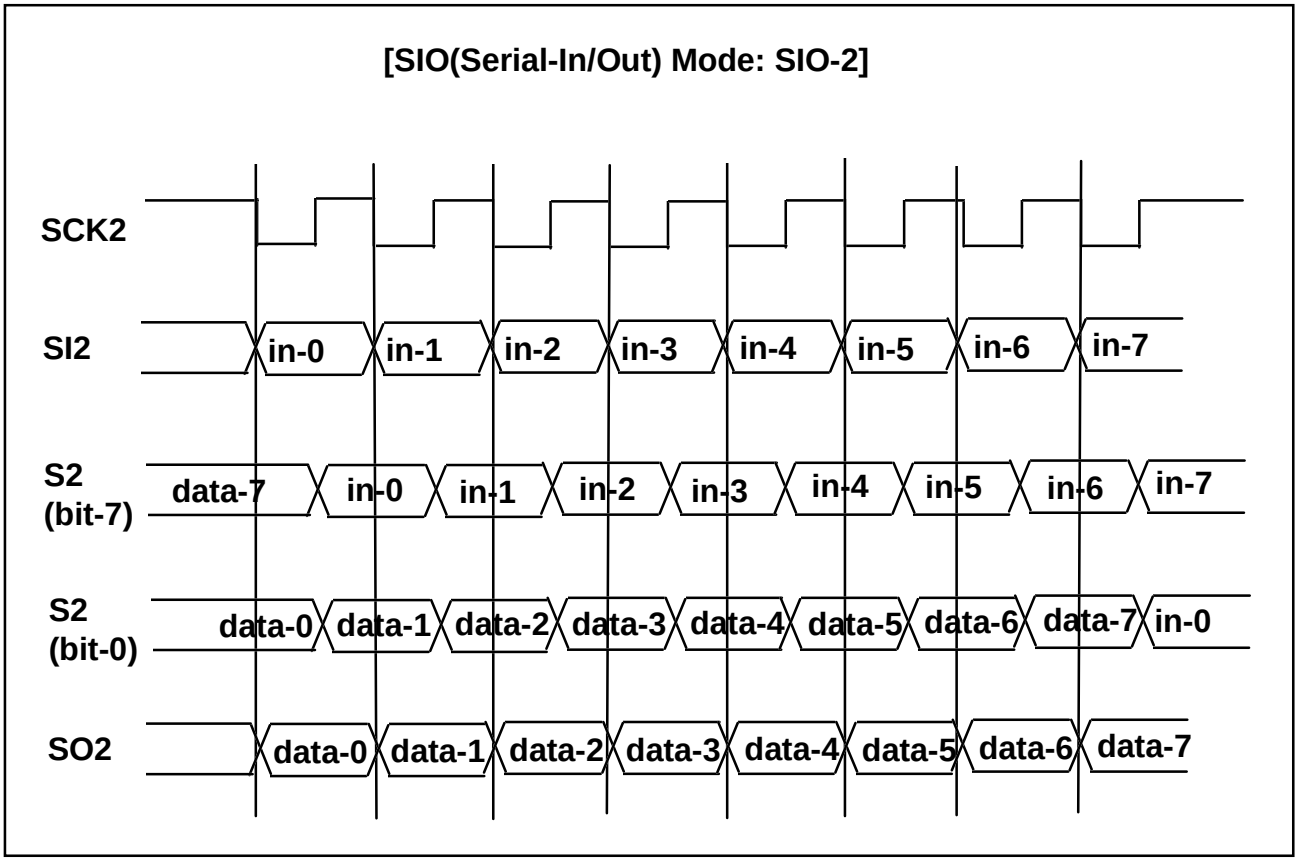
Control Bit	SOOE (bit-1)
Content	1

[Table: Pin Configuration of SIO for 8-bit Serial-I/O Mode]

Pin	In/Out Mode	Note
SI	Serial Input	The pin SI must be assigned to input mode by a port control register.
SO	Serial output	SOOE = 1
SCK SIOCR	SCK input mode	The pin SCK should be assigned as input.
SCK SIOCR	SCK output mode	The pin SCK is assigned as the SCK output pin

[Table: Shift Registers of SIO for 8-bit Serial-I/O Mode]

Shift Register	S
Operation	The MSB (bit-7) is connected to SI. The SI input signal should be synchronized to negative edge of the SCK. The S should be loaded 8-bit data to be serial output before operation. The LSB(bit-0) is connected to the output flip-flop. The flip-flop is connected to the SO pin. The shift operation is performed on positive edge of the SCK. The SO output synchronized to the just next negative edge of the SCK. After 8-bit shift, the S will have 8-bit serial input data.



13.5. SIO Control Register (SIOCR)

[Table: Definition of SIOCR]

Address	F4H							
Bit Addr.								
BIT	7	6	5	4	3	2	1	0
NAME	SEN		SFS	SFS1	SFS0		SOOE	
Definition	SIO ENable	Reserved bit	SIO input Frequency Select bit-2	SIO input Frequency Select bit-1	SIO input Frequency Select bit-0	Reserved bit	SIO SO Output En-able	Reserved bit
Reset Value	0	unknown	0	0	0	0	0	unknown

Read/ Write by Software	**R/W**		**R/W**	**R/W**	**R/W**	**User MUST write a '0' to this bit. This bit is readable and writable.**	**R/W**	
Write by Hardware	**0 by SIO overflow or S/W**							

[Table: The Description of SIOCR]

Name	Bit	Description
SEN	7	SIO ENable bit [Bit Status: 0 (Initial Value)] A selected input clock is halted to high. The SIO counter is cleared to 0. [Bit Status: 1] A selected input clock is run. The SIO counter counts up the negative edge of the selected clock.
Reserved	6	
SFS[2:0]	5 to 3	SIO input clock Frequency Select bits [Bit Status: 000 (Initial Value)] SCK (from external input) [Bit Status: 001] $F_{sys}/24$ [Bit Status: 010] $F_{sys}/48$ [Bit Status: 011] $F_{sys}/96$ [Bit Status: 100] $F_{sys}/192$ [Bit Status: 101] $F_{sys}/384$ [Bit Status: 110] $F_{sys}/768$ [Bit Status: 111] $F_{sys}/1536$ To use the SCK pin as an external clock input, the SCK pin should be assigned to input mode by a port control register.
Reserved	2	User **MUST** write a '0' to this bit. **NEVER** write a '1' to this bit.

SOOE	1	SO Output Enable [Bit Status: 0 (Initial Value)] The pin SO can be used as a normal I/O port. [Bit Status: 1] The pin SO is used as the serial output pin.
Reserved	0	

13.6. SIO Shift Register (SIODAT)

[Table: Definition of SIODAT]

Address	F5H							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**S[7:0]**							
Definition	**Shift register** **8-bit SO Mode: 8-bit output buffer** **8-bit SI Mode: 8-bit input buffer** **16-bit SIO Mode: 8-bit output buffer & 8-bit input buffer**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Software	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**

13.7. SIO Module Functional Description

13.7.1 Serial In

STEP-1:

Before the SIO clock signal get transmitted through SCK pin, SCK pin should set to high. This is necessary only when internal clock is used (SIO1CR[5:3] not equal to 000).

STEP-2:

Then, user should enable the SIO. This is done by writing the SIOCR with proper value.

STEP-3:

If internal clock is used, SIO will generate the appropriate clock signal for interfacing with the external chip. If external clock is used, user will need to signal the external chip that SIO is ready to take data and clock signal.

STEP-4:

After receiving the data, SINT(interrupt signal) will set to high. At that time, SIO waits for the CPU to read the received data.

13.7.2 Serial Out

STEP-1:

Before the SIO clock signal get transmitted through SCK pin, SCK pin should set to high. This is necessary only when internal clock is used (SIOCR[5:3] not equal to 000).

STEP-2:

Then, user should write the data to SIODAT..

STEP-3:

Next, user should enable the SIO. This is done by writing the SIOCR with proper value.

STEP-4:

If internal clock is used, SIO will generate the appropriate clock signal for interfacing with the external chip. If external clock is used, user will need to signal the external chip that SIO is ready to transmit the data and is waiting for their clock signal.

STEP-5:

After transmitting the data, SINT will set to high.

13.7.3 Serial-I/O

Before the SIO clock signal get transmitted through SCK pin, SCK pin should set to high. This is necessary only when internal clock is used (SIOCR[5:3] not equal to 000).

STEP-2:

Then, user should write the data to SIODAT.

STEP-3:

Next, user should enable the SIO. This is done by writing the SIOCR with proper value.

STEP-4:

If internal clock is used, SIO will generate the appropriate clock signal for interfacing with the external chip. If external clock is used, user will need to signal the external chip that SIO is ready to do transmission and reception, and is waiting for their clock signal.

STEP-5:

After the operation, SINT will set to high. At this time, SIO waits for CPU to read the received data.

13.7.4 Voice Module Control

When the DEN bit of VMINTCR is set to “1”, the SI, SO, and SCK signals are connected interrnally to the Voice Module. The SI, SO, and SCK pins of SS1103 should be configured by the software to avoide conflicts with the devices connected to these pins. After the programming of the Voice Module these pins should be configured back into the states used before the programming of the Voice Module.

14. SPI (Serial Peripheral Interface)

14.1. Overview

The Serial Peripheral Interface (SPI) module is a serial interface module useful for communicating with other microcontroller and peripherals. The module may be configured for a point to point or for a point to multipoint connection containing one master device and several slave devices. In SST1103, the SPI can only be a master. The SPI allows 8-bits of data to be synchronously transmitted and received simultaneously.

14.2. SPI Pin Description

There are three pins (SO, SI, SCK) are used to accomplish communication. The SI pin is configured as a data input. The most significant data bit is sent first.

The SO is configured as a data output. The most significant data bit is sent first.

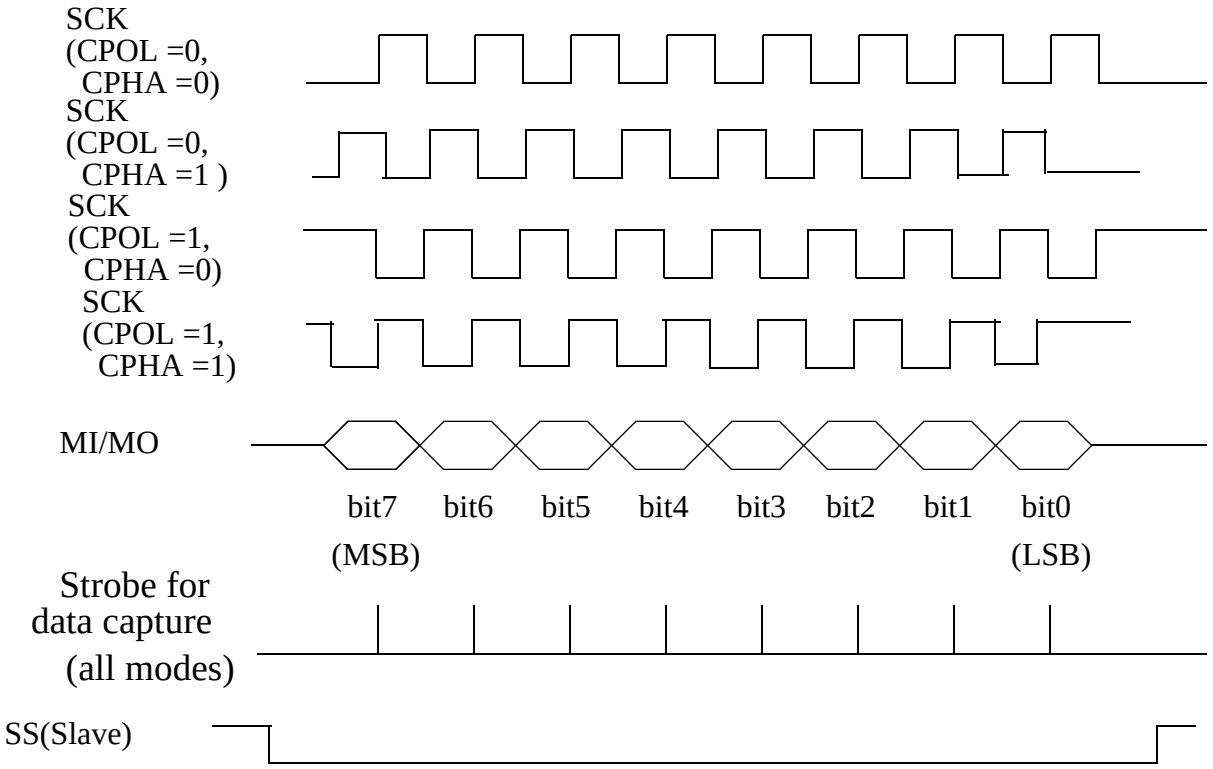
The SI is configured as a data input. The most significant data bit is received first.

The SCL is used to synchronize data transfer through SI and SO. Since SCK is generated by the master device, this pin is configured as an output.

In the SPI communications the clock is generated by master and this clock is used to synchronize data transfer through SI and SO. Since SCK is generated by the master device, this pin is configured as an output.

As shown in Fig. 1, four possible timing relationships may be chosen by using control bits CPOL(clock polarity) and CPHA(clock phase) in the serial peripheral control register (SPI1CR). Both master and slave device must operate with the same timing.

The clock frequency is selected by using control bits SPR0 and SPR1 in the SPI1CR of the master device. The slave device has no control of the clock frequency.



SPI Timing Diagram

14.3. SPI Operation

The SPI has a shift register and a receive buffer. The shift register shifts data in and out of the device. The data byte transmitted is replaced by the data byte received. The SPI data register(SPI1DAT) actually represents two distinct devices. Writes to SPI1DAT are writes to the shift register itself. On the other hand, reads of SPI1DAT do not read from the shift register, but rather from a buffer register which is automatically loaded from the shift register upon the completion of a data transfer. This double buffering allows the next data byte to start reception before reading the data that was just received.

Any write to the SPI1DAT during data transfer will be ignored, and will cause the write collision(WCOL) status bit in the SPI1SR to be set. After the data transfer is

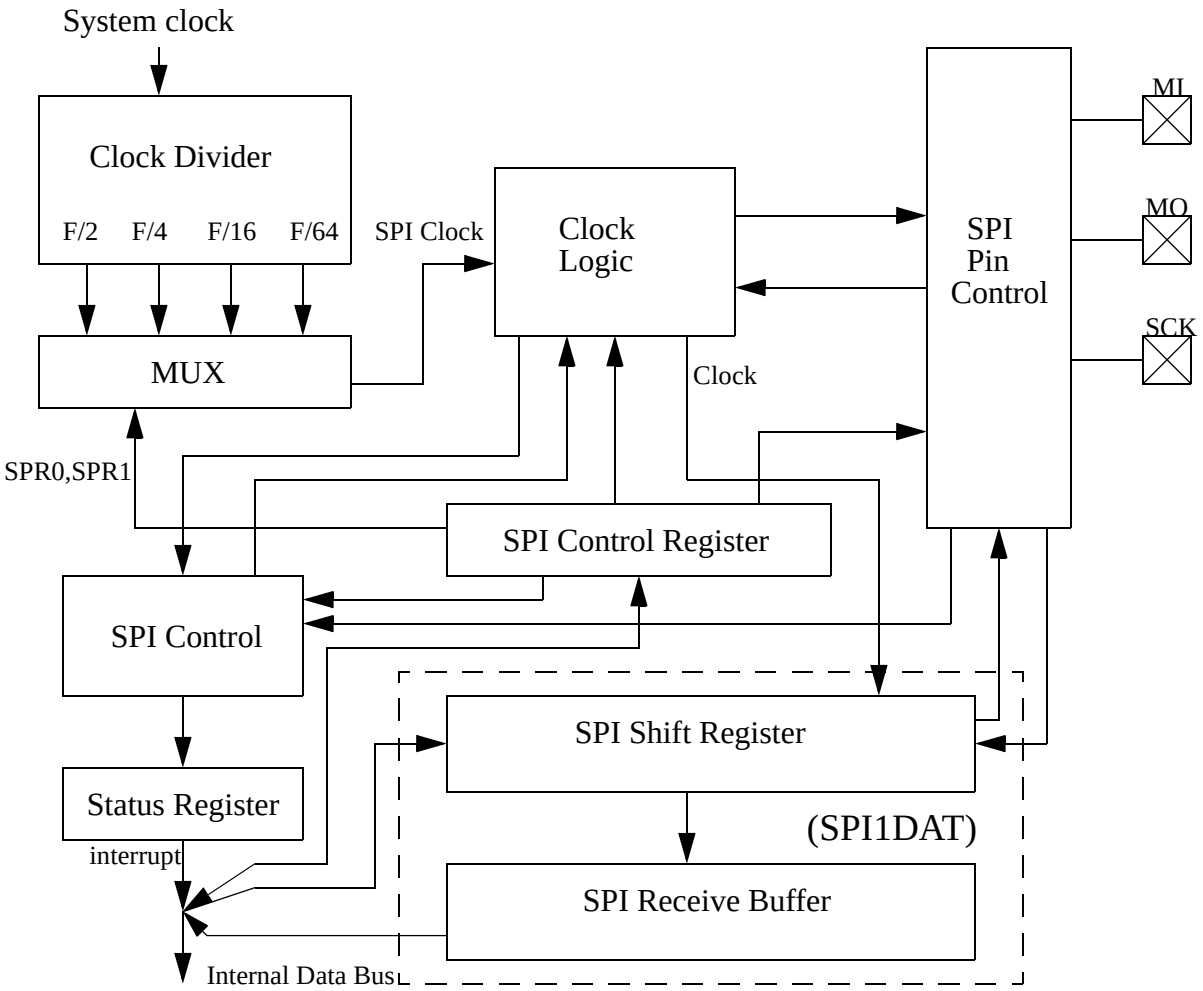


Fig. 3 shows the interconnections for one master and one slave.

completed, internal interrupt is generated and the SPIF flag of the SPI1SR is set. Clock is generated and data is shifted as soon as data is written to the shift register.

For SPI to start its function, writing value to the data register will start the SPICLK and data output. Therefore, user has to write the control register value to enable the SPI before writing the data register value, hterwise there will be the wrong data output from SPI.

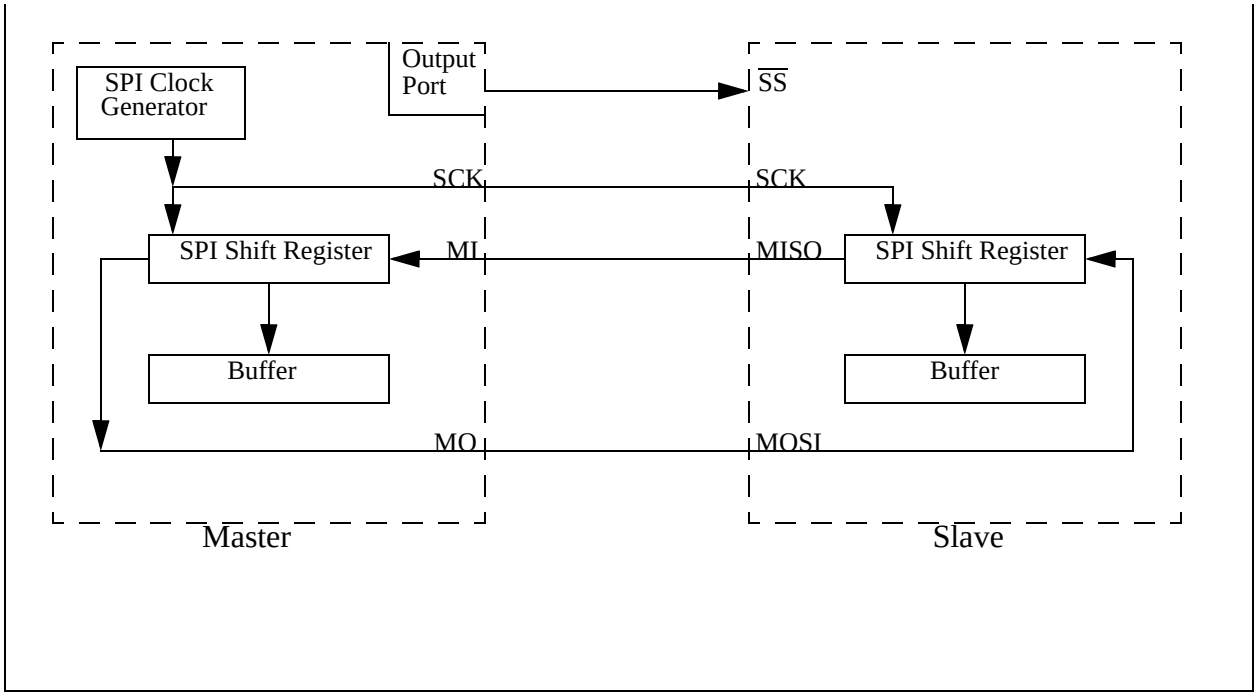
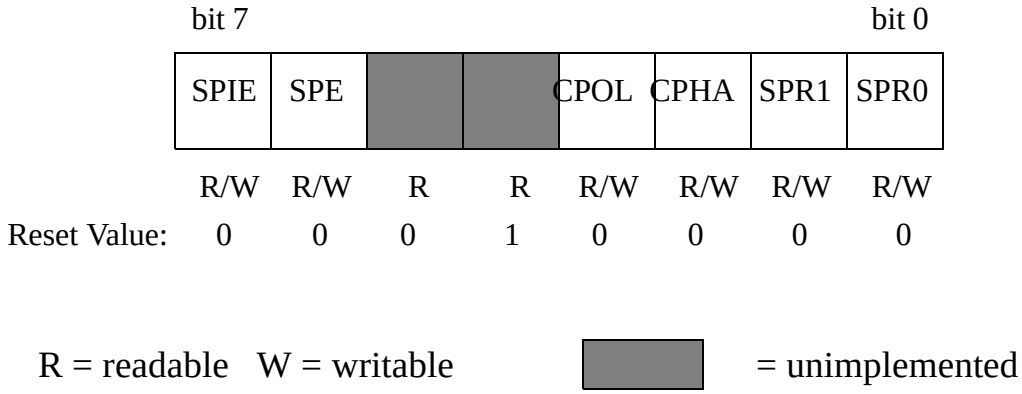


Figure3. SPI Master-slave Interconnection

14.4. Serial Peripheral Control Register (SPI1CR)



bit 7: SPIE: Serial Peripheral Interrupt Enable

0 = Disables internal SPI interrupt

1 = Enables internal SPI interrupt

bit 6: SPE: Serial Peripheral System Enable

0 = Turn off SPI system

1 = Turn on SPI system

bit 3: CPOL: Clock Polarity (See Fig. 1)

0 = Idle state for clock is high

1 = Idle state for clock is low

bit 2: CPHA: Clock Phase

0 = Transmit data on falling edge and receive data on rising edge

1 = Transmit data on rising edge and receive data on falling edge

When CPHA = 0, as soon as SS(Slave Select in slave device) goes low, the transaction begins and data will be sampled on first edge of SCK.

When CPHA = 1, the SS(Slave Select in slave device) may be thought of as simple enable control.

bit 1-0: SPR1 and SPR0: SPI Clock Rate Select

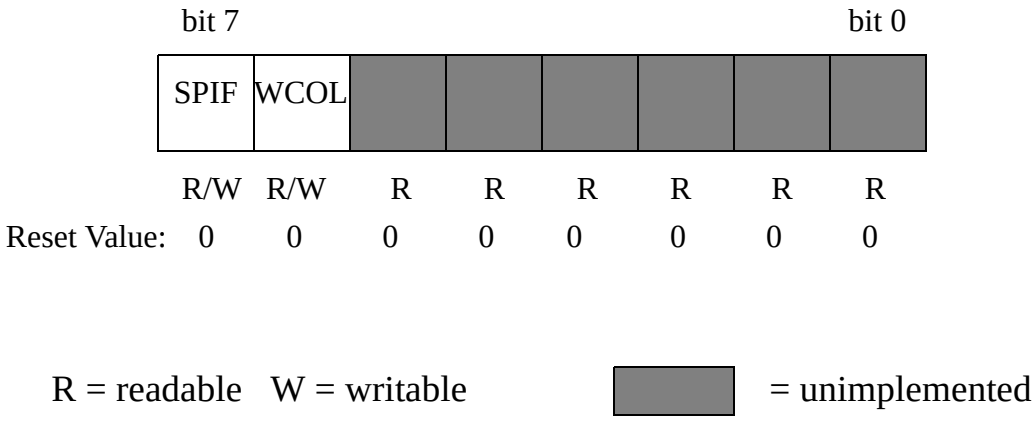
00 = Fosc/2

01 = Fosc/4

10 = Fosc/16

11 = Fosc/64

14.5. Serial Peripheral Status Register (SPI1SR)



bit 7: SPIF: SPI Transfer Complete Flag

0 : Data transfer not complete

1 : Data transfer complete

If SPIF goes high and if SPIE is set, an internal interrupt is generated. SPIF can be cleared by reading SPI1SR followed by an read of the SPI1DAT. A write to SPI1DAT will be ignored if SPIF is set.

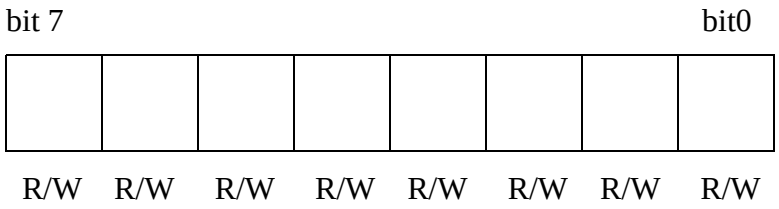
bit 6: WCOL: SPI Write Collision Detect

0: No collision

1: Collision, Attempt to write to SPI1DAT while data transfer is still in progress.

When CPHA is low, a transfer starts when SS(Slave Select in slave device) goes low and finishes when SS(Slave Select in slave device) goes high. When CPHA is high, a transfer starts when SCK first becomes active while SS(Slave Select in slave device) is low. The transfer finishes when SPIF is set. WCOL can be cleared by reading SPI1SR followed by a read of the SPI1DAT.

14.6. SPI Data Register (SPI1DAT)



R= readable W=writable

15. Universal Asynchronous Receiver Transmitter (UART)

The module is a standard full-duplex asynchronous serial two-wire communications interface with programmed baud rates (standard UART) compatible with the Standard Serial Interface for 8051.

The serial data format provides one start bit, eight or nine data bits and one stop bit.

15.1. Features

- Full-duplex operations (simultaneous transmit and receive)
- 8 software selectable baud rates
- Software selectable word length (eight or nine bits)
- Interrupt drive capability
- Receiver wake-up
- Idle line detection
- Framing error detection
- Overflow and register full detection
- Transmit complete flag
- Send break

15.2. Baud Rate and UartTimer Matching Value

15.2.1 For UART Mode 1 and Mode 3

Fsys = 4.096 MHz.

Baud Rate	Measured Baud Rate	Osc. Frequency	SMOD	Uarttimer Reload Value
19.2 KHz	18.96 KHz	3.641 MHz	1	0BH
9.6 KHz	9.48 KHz	3.641 MHz	0	0BH
4.8 KHz	4.74 KHz	3.641 MHz	0	17H
2.4 KHz	2.37 KHz	3.641 MHz	0	2FH
1.2 KHz	1.185 KHz	3.641 MHz	0	5FH

TABLE 12.

15.2.2 For UART Mode 0

The Baud Rate is Uart Oscillator Frequency / 12. With Oscillator Frequency at 3.641MHz, the baud rate is 3.641 MHz/12 or 303.4 KHz.

15.2.3 For UART Mode 2

With SMOD = 0, the baud rate is 1/64 of the oscillator frequency. If SMOD = 1, the baud rate is 1/32 of the Uart oscillator frequency. With Oscillator Frequency at 3.641MHz, the baud rate is 56.89KHz with SMOD = 0, and 113.78 KHz with SMOD = 1 respectively.

15.3. UART Control Register

	7	6	5	4	3	2	1	0
UACR	CEN	EN	-	-	-	-	-	SMOD
	R/W	R/W	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0

TABLE 13.

Address:B6H

CENCounter Enable. This bit is used to enable the UART counter. Writing “0” will disable the Uart counter.

ENEnable. This bit is for enabling the UART Block. Writing “0” will halt the UART block.

Bit 5 - Bit 1Reserved. These bits will always be read as “0”.

SMODSMOD value. Write “0” or “1” to SMOD depending on the output Baud Rate.

15.4. UART Counter Matching Register

	7	6	5	4	3	2	1	0
UACNT	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Address:B5H

Data7 to Data0Data bits. These bits represent the matching value for the UART Counter.

16. Keypad Control

16.1. Overview

Two ports of SS1103 are used to provide an interface to a keypad. These two ports support 6x6 keypad. The ports can be configured as keypad interface ports or as GPIO. Each port and each pin of a port can be configured independently by setting the corresponding bits in KPDCR register.

When configured as the keypad interface, one port (Port R) is configured as an input with the pull-up resistors enabled, while another port (PortC) is configured as the output low. The internal pull-up resistors of the PortR will cause all lines to be logic one when no key is pressed.

When a key is depressed an interrupt is initiated by the high to low transition on PortR.

The software should provide all requirement debouncing periods and scanning.

16.2. Keypad Control Register

Bit/ Name	7	6	5	4	3	2	1	0
KPDCR	R5EN	R4EN	R3EN	R2EN	R1EN	R0EN	REI	FEI
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Address: C2H

Legend:

R5EN - R0EN Row Enables. Writing a "1" enables that row for keypad use by enabling both its rising and falling transition detectors. Writing a "0" disables the row and allows it to be used as a GPIO.

REI Rising Edge Row Interrupt. This bit is set to a "1" when the pending keypad interrupt was caused by a key release. It must be cleared by software by writing a "0".

FEI Falling Edge Row Interrupt. This bit is set to a "1" when the pending keypad interrupt was caused by a key depression. It must be cleared by software by writing a "0".

17. Dial Pulse Generation

17.1. General

The Dial Pulse/Flash generator provides the pulse dialing and mute control for the pulse dialing.

The software initiates the Pulse Dialing Block (PDB) for the pulse dialing. The software should use the PDB and the Time Base Timer (TBT) for the generation of the Mute1 and Mute2 pulses.

The generated dialing pulses are output to the DP/FL pin. The generated Mute1 and Mute2 pulses are output to the MT1 and MT2 pins, accordingly.

17.2. Pulse Dialing

The PDB consist of PWM timer and a counter. Three SFR: DPFCR, DPFDAT, and DPFINT are provided to control the PDB.

The valid keys in the pulse dialing mode are the 10 numeric dial keys (0 to 9). The non-numeric dial keys have no effect on the dialling or the redial.

The timing diagram and signal parameters for the pulse dialing are shown in Figure. “Timing diagram for pulse dialing”. All programmable parameters should be set into control registers. The PDB generates and interrupt when the number of pulses, corresponded to the key depressed, is dialed. The software can start now the dialing of the next digit.

17.3. Flash Output Control

When the “Flash” pin is depressed on a keypad, the flash should be generated by the software on the DP/FL pin by setting the Bit 0 of DPFCR control register. Flash pulse can be initiated either in DTMF or in the pulse dialing mode. The pulse and the hold-over time should be specified by the software.

17.4. DTMF Timing Control

In the DMF mode the single and dual tones which are generated by the codec are timed. In manual dialing the duration of bursts and pauses is not the actual key depression time, but rather the time calibrated by the application software. The duration should not be less than the minimum transmission time (Tt) or minimum pause time (Tp).

When the redial feature is used, the transmission time is calibrated by the application software in the same manner as it is for the manual dialing.

In the DTMF mode the output signals of the module should be output to the codec control circuits instead of connection to the pins.

Timing diagram for the DTMF control signals is shown in Figure . “Timing Diagram for the DTMF and Flash signals”.

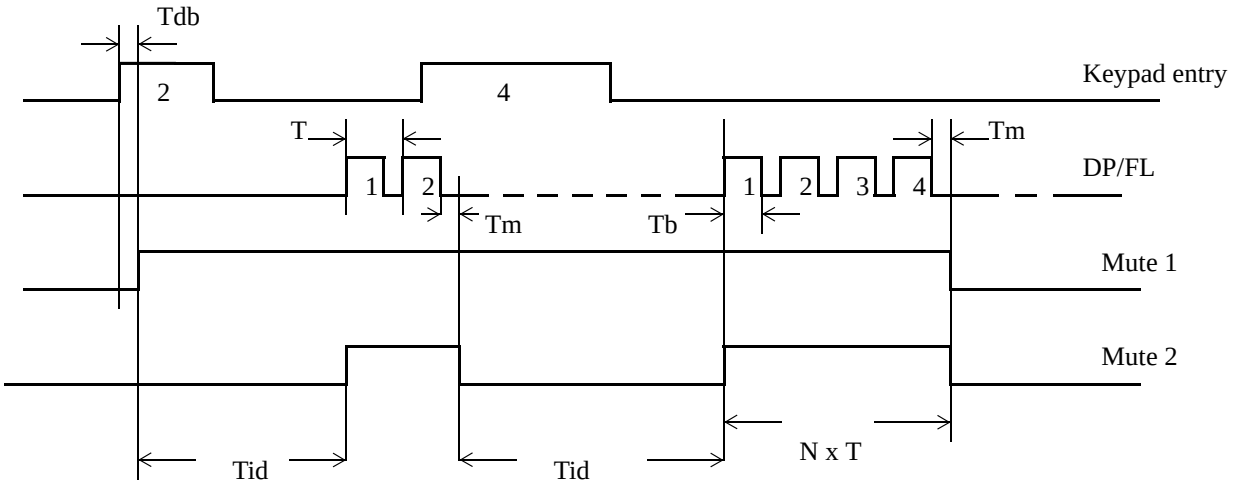
17.5. Mute Signals

Two kinds of mute signal should be provided by the software - Mute 1 and Mute 2. The TBT should be used to generate these signals.

The Mute 1 signal indicates when the speech should be muted. This signal is active during dialing including interdigit pauses. The Mute 1 output can be used to disable the microphone during dialing. It remains active until the last digit is pulsed out. The last digit is defined by the application software.

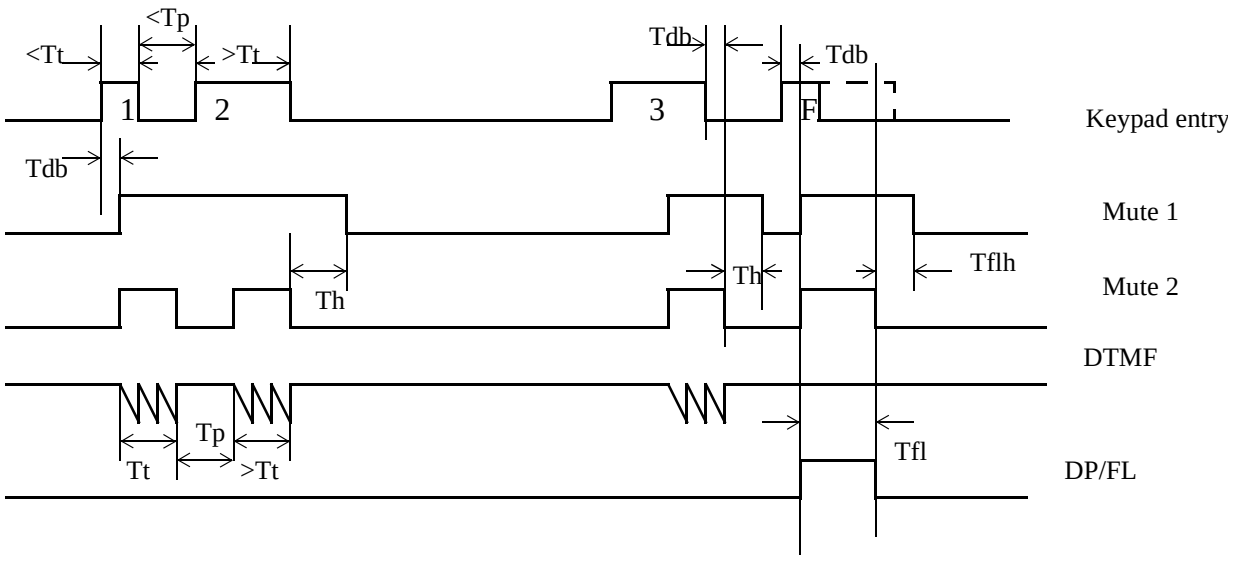
The Mute 2 signal is a digit mute signal. The Mute 2 output is active during actual dialing; i.e. during break or make time in pulse dialing, or during tone ON/OFF in DTMF dialing. It is not active during interdigit pauses.

The mute signal or signas can be output to the pins or they can be delivered to the codec. When the signal or signals are output to the codec, the MT pin or pins can be used as GPIO pins.



Tdb - Debouncing time (software defined, not less than 12ms)
T - Dialing pulse period (100ms). Automatically controlled by PDB.
Tid- Inter-digit pause (840ms). Automatically controlled by PDB.
Tm - Make time (programmable. 40msec default)
Tb - Break time (programmable. 60msec default)

Figure. Timing Diagram for the Pulse Dialing.



Tdb - Debouncing time (software defined, not less than 12ms)
Tt, Tp - Transmission and pause time (min 68ms)
Th - Hold-over time (muting on Mute 1- 80ms)
Tflh -Flash hold-over time
Tfl - Flash pulse duration (>100ms)

Figure . Timing Diagram for the DTMF and Flash signals.

17.6. Dial Pulse/Flash Control Register

Bit/Name	7	6	5	4	3	2	1	0
DPFCR	EN	CLR						FLASH
	R/W	R/W	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0

Address: D1H

Legend:

EN Enable. This bit enables the Dial Pulse Flash Generator Block. Writing a "0" to this bit disables the block by halting the inputclock.

CLR Clear. Writing a "1" to this bit clears the DPFCNT to 00H. This bit always reads a "0".

Bit5 - Bit1 Reserved. These bits always read "0".

Bit 0. FLASH Flash output. This bit determines the value of the DP/FL pin when outputting a FLASH pulse.

17.7. Dial Pulse/Flash Data Register

Bit/Name	7	6	5	4	3	2	1	0
DPFDAT	Dat7	Dat6	Dat5	Dat4	Dat3	Dat2	Dat1	Dat0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Address: D2H

Legend:

Dat7-Dat0 Data bits. These bits determine the make time and break time of the dialed pulse at the DP/FL pin.

17.8. Dial Pulse/Flash Counter Register

Bit/Name	7	6	5	4	3	2	1	0
DPFCNT					Cnt3	Cnt2	Cnt1	Cnt0
	R	R	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Address: D3H

Legend:

Cn3-Cn0 Counter bits. These four bits determine the number of pulses produced at the DP/FL pin during the pulse dialing.

18. WatchDog Timer

18.0.1 Overview

The WD-Timer (WatchDog Timer) can be used as a watch-dog timer or as a basic interval timer for monitoring the software malfunctioning. The WD-Timer re-initializes the MCU from an unexpected device upset state. For instance, if a program falls into an infinite loop because of noise, the WD-Timer will wake up the CPU. By enabling the WatchDog Reset, this feature will be active. By disabling the WatchDog Reset and enabling the WatchDog Interrupt, the WD-Timer can be used as a basic interval timer. Only Fsys/12 is supported while under SlowAll or SlowPeri modes.

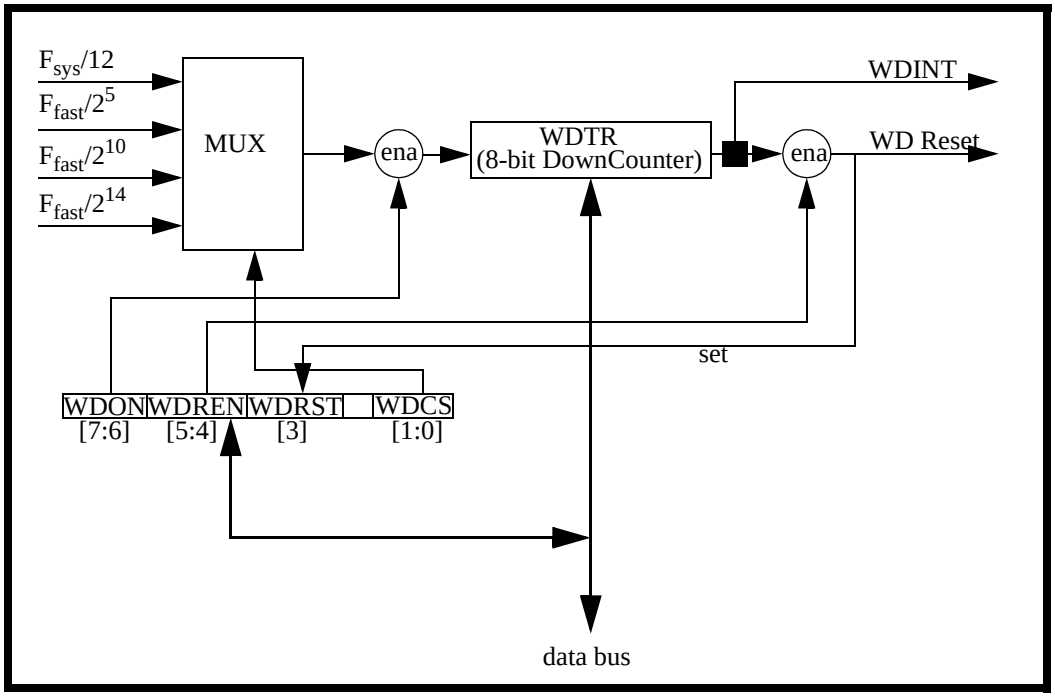


Figure 6. *Watchdog timer block diagram*

19. Time Base Timer

19.1. Overview

The Time Base Timer (TB-Timer) is an 8-bit auto-reload timer. The TB-Timer is composed of a input frequency select MUX, an 8-bit up-counter (TBCNT), a Comparator, an 8-bit data register (TBDAT), and a control register(TBCR).

The TB-Timer has 8 counting clocks that can be selected by TBFS[2:0]. Four of the clocks come from the System Clock block, i.e. F_{1SEC}, F_{1MIN}, F_{1HOUR}, and F_{125mS}. If the slow oscillator is stopped, these four clocks will stop too. These four clocks will be very useful to generate a real time interval and to minimize the number of CPU wake-ups. The period of the $F_{sys}/12$ clock is one machine cycle or one fastest instruction cycle. This clock will run during any power-saving mode except the StopAll mode. During the FastAll or FastPeri mode, the $F_{sys}/12$ clock is equal to $F_{fast}/12$. During the SlowAll or SlowPeri mode, the $F_{sys}/12$ clock is equal to $F_{slow}/12$. The $F_{fast}/2^4$, $F_{fast}/2^{14}$, and $F_{fast}/2^{18}$ can be used during the FastAll or FastPeri mode only.

After the TBEN bit is set to high, the TBCNT will start to count the negative edge of an input clock. When the TBEN bit is low, the Match signal is never generated even though the contents of the TBDAT and TBCNT are the same. The TBCNT is the 8-bit up-counter that can be cleared by the TBCLR bit or the Match signal. The TBCNT is a modulo-N counter (from 0 to N-1), N is the content of the TBDAT. The match signal will always set the TBINT bit to high. The TBINT bit can be cleared by the TB-Timer Interrupt Acknowledge or by software.

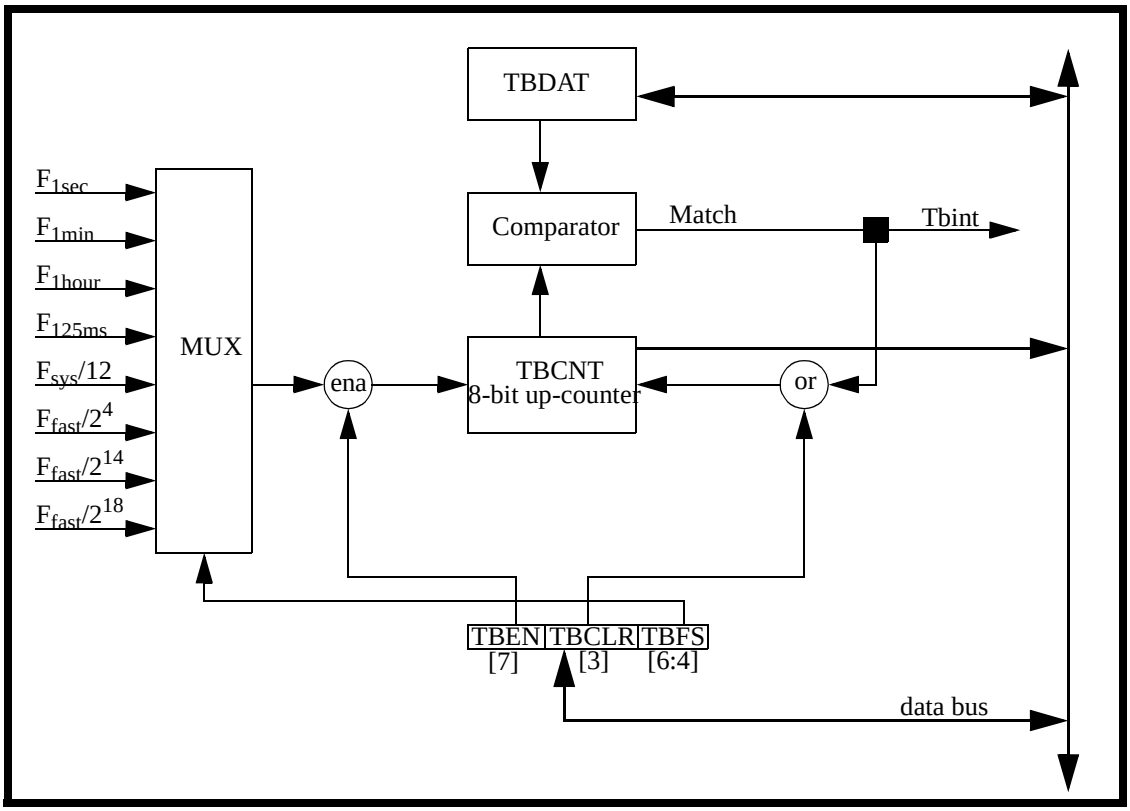


Figure 7. *Time Base timer*

19.2. Time Base Timer Control Register (TBCR)

[Table: Definition of TBCR]

Address	**B1H**							
Bit Addr.								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**TBEN**	**TBFS2**	**TBFS1**	**TBTFS0**	**TBCLR**	**HTST**	**MTST**	
Definition	**TB timer ENable**	**TB timer input Frequency Select bit-2**	**TB timer input Frequency Select bit-1**	**TB timer input Frequency select bit-0**	**TB counter CLeaR**	**Hour Clock Test**	**Minute Clock Test**	**Reserved**
Reset Value	**0**	**0**	**0**		**0**	**0**	**0**	**0**
Read/ Write by Software	**R/W**	**R/W**	**R/W**		**R/W Always 0 read.**	**R/W**	**R/W**	**R**
Write by Hardware								

[Table: The Description of TBCR]

Name	Bit	Description
TBEN	7	**TB timer ENable bit** [Bit Status: 0 (Initial Value)] A selected input clock is halted. The TBCNT keeps the counter value. [Bit Status: 1] A selected input clock is run. The TBCNT counts up the negative edge of the selected clock.

TBFS[2:0]	6 to 4	**TB timer input clock Frequency Select bits** [Bit Status: 000 (Initial Value)] F_{1SEC} [Bit Status: 001] F_{1MIN} [Bit Status: 010] F_{1HOUR} [Bit Status: 011] F_{125mS} [Bit Status: 100] $F_{sys}/12$ [Bit Status: 101] $F_{fast}/2^4$ [Bit Status: 110] $F_{fast}/2^{14}$ [Bit Status: 111] $F_{fast}/2^{18}$
TBCLR	3	**TB counter CLeaR bit** If this bit is written with high, the TBCNT (8-bit up-counter) of the TB Timer will be cleared to 00H. Writing low will not affect anything. When read, a low(0) will be always read.
HTST	2	**Hour clock Test bit** [Bit Status: 0 (Initial Value)] Normal hour clock signal is used for F_{1hour} . [Bit Status: 1] A test mode using XSout (32.768KHz) for F_{1hour} . Note: The bit can only be set either under FastAll or FastPeri modes. User should write a 0 to this bit.
MTST	1	**Minute clock Test bit** [Bit Status: 0 (Initial Value)] Normal minute clock signal is used for F_{1min} . [Bit Status: 1] A test mode using the XSout (32.768KHz) for F_{1min} . Note: The bit can only be set either under FastAll or FastPeri modes. User should write a 0 to this bit.
TBINT	0	**Reserved bits**

19.3. TB-Timer Counter Register (TBCNT)

[Table: Definition of TBCNT]

Address	**B2H**
Bit Addr.	**None**

BIT	7	6	5	4	3	2	1	0
NAME	TBCNT[7:0]							
Definition	TB-timer CouNTer register bit 7 to 0 (Modulo N Up-counter: 00 to N-1, N is the content of TBDAT)							
Reset Value	0	0	0	0	0	0	0	0
Read/ Write by Software	R	R	R	R	R	R	R	R
Write by Hardware	Written with a new count value 0 or 1. 0 by TBCLR.	Written with a new count value 0 or 1. 0 by TBCLR.	Written with a new count value 0 or 1. 0 by TBCLR.	Written with a new count value 0 or 1. 0 by TBCLR.	Written with a new count value 0 or 1. 0 by TBCLR.	Written with a new count value 0 or 1. 0 by TBCLR.	Written with a new count value 0 or 1. 0 by TBCLR.	Written with a new count value 0 or 1. 0 by TBCLR.

[Table: The Description of TBCNT]

Name	Bit	Description
TBCNT[7:0]	7 to 0	**TB-timer CouNTer bits** A Modulo-N (00 to N-1) up-counter. N is the content of TBDAT. This counter counts up from 00H to N-1. Then, the counter will go back to 00H and the comparator will generate match signal. The counter will not stop after the Match. Thus, the TB-Timer will generate continuous Match signals with a fixed period. The TB-Timer is an auto-reload timer.

19.4. TB-Timer Data Register (TBDAT)

[Table: Definition of TBDAT]

Address	B3H							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	TBDAT[7:0]							
Definition	TB-timer DATa register bit 7 to 0							
Reset Value	0	0	0	0	0	0	0	0
Read/ Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware	none	none	none	none	none	none	none	none

[Table: The Description of TBDAT]

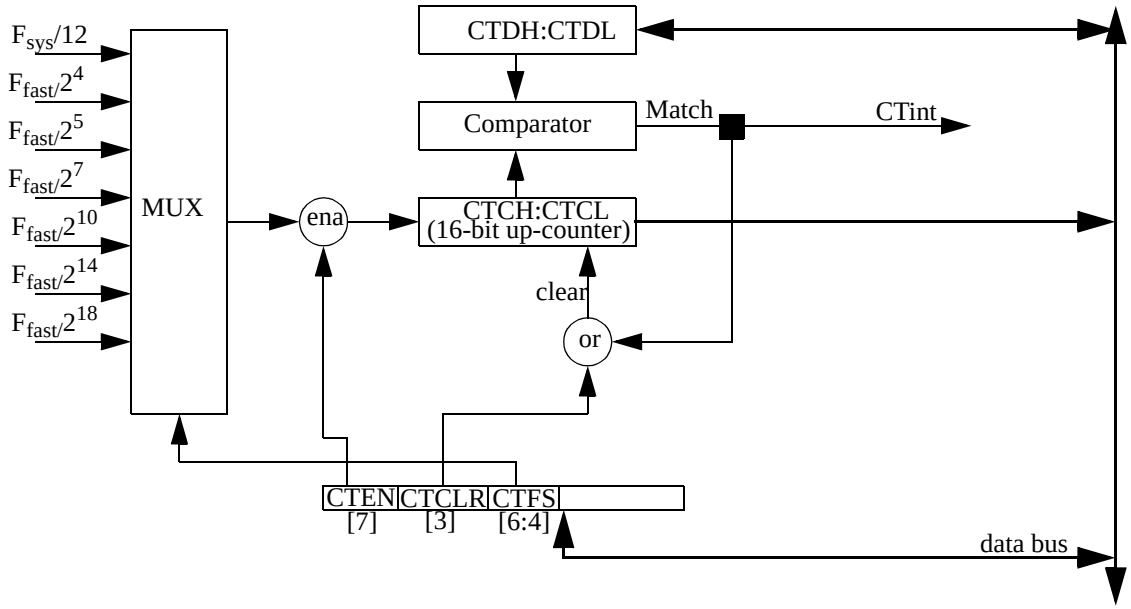
Name	Bit	Description
TBDAT[7:0]	7 to 0	**TB-timer DATa bits** [The first Match period] TB-Timer Match signal period = (1 / $F_{selected\text{-}clock}$) X (TBDAT + 1) - Deviation period 0 <= Deviation period < (1 / $F_{selected\text{-}clock}$) If any clock, which are divided from XSout(32.768KHz), is selected, the Deviation period can be minimized because the Slow Clock prescaler can be cleared by software. [The second or later Match period] TB-Timer Match signal period = (1 / $F_{selected\text{-}clock}$) X TBDAT (No Deviation period)

20. General Purpose Timer

20.1. Overview

There is 16-bit Genral Purpose Timer. A Genral Purpose Timer (or C-Timer) can be used as an Auto-Reload Timer, or a Genral Purpose Timer. A C-Timer is composed of a input frequency select MUX, a 16-bit up-counter(CT2CH-CT2CL), a Comparator, a 16-bit data register(CT2DH-CT2DL), and a control register(CT2CR).

Genral Purpose Timer in Auto-Reload Mode



20.2. Auto-Reload Mode

If the CT2MD[1:0]) in the CT2CR are 00B, the C-Timer1 (or C-Timer2) will operate in the Auto-Reload Mode.

A C-Timer has the 7 counting clocks that can be selected by CT2FS[2:0]. The period of the Fsys/12 clock is one machine cycle or one fastest instruction cycle. This clock will run during any power-saving mode except the StopAll mode. During the FastAll or FastPeri mode, the Fsys/12 clock is equal to Ffast/12. During the SlowAll or SlowPeri mode, the Fsys/12 clock is equal to Fslow/12. The Ffast/24, Ffast/25, Ffast/27, Ffast/210, Ffast/214, and Ffast/218 can be used during the FastAll or FastPeri mode only. After the CT2EN bit is set to high, the CT2CH & CT2CL will start to count the negative

edge of a selected input clock. When the CT2EN bit is low, the Match signal is never generated even though the contents of the CT2DH & CT2DL and or CT2CH & CT2CL are the same. The CT2CH & CT2CL is the 16-bit up-counter that can be cleared by the CT2CLR bit or the Match signal. The CT2CH & CT2CL is a modulo-N counter (from 0 to N-1), N is the content of the CT2DH & CT2DL. The match signal will always set the CT2INT bit to high. The CT2INT bit can be cleared by a C-Timer Interrupt Acknowledge or by software.

20.3. Genral Purpose Timer Control Registers (CT2CR)

[Table: Definition of /CT2CR]

Address								
Bit Addr.								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**CT2EN**	**CT2FS**	**CT2FS1**	**CT2FS0**	**CT2CLR**	**Reserved**	**Reserved**	**Reserved**
Definition	**C-Timer ENable**	**C-Timer input Frequency Select bit-2**	**C-Timer input Frequency Select bit-1**	**C-Timer input Frequency Select bit-0**	**C-Timer counter CLeaR**			
Reset Value	**0**	**0**	**0**	**0**	**0**			
Read/ Write by Soft-ware	**R/W**	**R/W**	**R/W**	**R/W**	**R/W Always 0 read.**			

[Table: The Description ofCT2CR]

Name	Bit	Description (Note: n = 1 or 2)

CT2EN	7	**C-Timer ENable bit** [Bit Status: 0 (Initial Value)] A selected input clock is halted. The CTnCH & CTnCL keeps counting value. [Bit Status: 1] A selected input clock is active. The CTnCH & CTnCL counts up the negative edge of the selected clock.
CT2FS[2:0]	6 to 4	**C-Timer input clock Frequency Select bits** [Bit Status: 000 (Initial Value)] $F_{sys}/12$ [Bit Status: 001] $F_{fast}/2^4$ [Bit Status: 010] $F_{fast}/2^5$ [Bit Status: 011] $F_{fast}/2^7$ [Bit Status: 100] $F_{fast}/2^{10}$ [Bit Status: 101] $F_{fast}/2^{14}$ [Bit Status: 110] $F_{fast}/2^{18}$ [Bit Status: 111] Reserved
CT2CLR	3	**CTn counter CLeaR bit** If this bit is written with high, the CTnCH & CTnCL (16-bit up-counter) of the C-Timer will be cleared to 0000H. Writing low will not affect anything. When read, a low(0) will always be read.
CT2INT	2	**Reserved bit**
CT2MD[1:0]	1 to 0	Reserved bits

20.4. C-Timer Counter Registers (CT2CH & CT2CL)

[Table: Definition of CTnCH (n = 1 or 2)]

Address								
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**CTnCH[7:0]**							
Definition	**C-Timer-n CouNTer register bit 15 to 8** **(Auto-Reload Mode: High 8-bit of the Modulo N Up-counter: 0000H to N-1, N is the content of CTnDH & CTnDL)**							

Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Software	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Write by Hardware	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**

[Table: Definition of CTnCL (n = 1 or 2)]

Address								
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**CTnCL[7:0]**							
Definition	**C-Timer-n CouNTer register bit 7 to 0 (Auto-Reload Mode: Low 8-bit of the Modulo N Up-counter: 0000H to N-1, N is the content of CTnDH & CTnDL)**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Software	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Write by Hardware	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**	**Written with a new count value 0 or 1. 0 by CTnCLR.**

[Table: The Description of CTnCH & CTnCL]

Name	Bit	Description
CTnCH[7:0] & CTnCL[7:0]	15 to 0	**C-Timer-n CouNTer bits** [Auto-Reload Mode] A Modulo-N (0000H to N-1) up-counter. N is the content of CTnDH & CTnDL. This counter counts up from 0000H to N-1. Then, the counter will go back to 0000H and the comparator will generate a match signal. The Match signal will issue an interrupt request. The counter will not stop after the Match. Thus, any C-Timer will generate continuous Match signals with a fixed period.

20.5. C-Timer Data Register (CT2DH & CT2DL)

[Table: Definition of CTnDH (n = 1 or 2)]

Address								
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**CTnDH[7:0]**							
Definition	**C-Timer-n DATa register bit 15 to 8**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Software	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware	**[A-Reload] none**	**[A-Reload] none**	**[A-Reload] none**	**[A-Reload] none**	**[A-Reload] none**	**[A-Reload] none**	**[A-Reload] none**	**[A-Reload] none**

[Table: Definition of CTnDL (n = 1 or 2)]

Address	

Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	CTnDL[7:0]							
Definition	C-Timer-n DATa register bit 7 to 0							
Reset Value	0	0	0	0	0	0	0	0
Read/ Write by Soft-ware	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hard-ware	[A-Reload] none	[A-Reload] none	[A-Reload] none	[A-Reload] none	[A-Reload] none	[A-Reload] none	[A-Reload] none	[A-Reload] none

[Table: The Description of CTnDH & CTnDL]

Name	Bit	Description
CTnDH[7:0] & CTnDL[7:0]	15 to 0	**C-Timer-n DATa bits** [The first Match period in Auto-Reload Mode] C-Timer Match signal period = $(1 / F_{selected\text{-}clock})$ X ({CTnDH,CTnDL} + 1) - Deviation period 0 <= Deviation period < $(1 / F_{selected\text{-}clock})$ [The second or later Match period in Auto-Reload Mode] C-Timer Match signal period = $(1 / F_{selected\text{-}clock})$ X CTnDH&CTnDL (No Deviation period)

21. SS1103 Reset

21.1. Overview

There are two sorces which reset the SS1103. One external reset - NRESET pin, and one internal - Power-On-Reset (POR). The NRESET always override the POR. Both sorces reset all modules of the chip.

Two modules, SSTM and Voice module have additional sorces of reset. They can be reset by software, aslo.

The SSTM Reset bit of SSTMCR can be set by software. It is cleared by hardware.

For the Voice Module the reset description is provides in Section “Reset and Power Down”.

21.2. Power-On Reset (POR)

21.2.1 General

The power-on reset circuit provides internal SS1103C reset for most power-up situations.

POR consists of power-up detect block, start-up timer, and reset latch. The output of the reset latch is an internal reset (chip_reset) signal. This signal goes low when Vcc rises to the specified level and the signal goes high after some specified interval of time. This interval is determined by the start-up timer.

Ramping up of Vcc generates the Power-up Detect (PUD) signal. This signal does not come until Vcc achieves a level where the logic circuits of the POR start to operate.

The POR is used only at power-up and should not be used to detect drops in power supply voltage.

The PUD is multiplexed with Nreset (external reset signal). The Nreset always overrides the internal reset.

The SS1103C becomes functional after the chip_reset is generated.

Figure 8. and Figure 9. show timing diagrams.

21.2.2 Operation

At power-up, the reset latch and the start-up timer are reset to the appropriate state by the PUD pulse. After some time interval (2^n pulses of the high frequency clock for an n-bit counter) the start-up timer will trigger the reset latch (if there is no Nreset active) and thus issue the chip_reset signal.

The chip_reset signal will be generated by the internal POR circuit when the Nreset signal is held high. The Nreset can be used to override the internal reset.

21.2.3 Crystal Oscillator Start-Up Time

After Vcc achieves the operational level, the crystal oscillator will require time to stabilize. This is the crystal oscillator start-up time.

Low frequency crystals have a typical start-up time of 1-2sec. Higher frequency crystals have shorter start-up times (1-2ms). Start-up times are voltage dependent. The SS1103C uses the high frequency crystal for the start-up timer because it is the default clock at

reset time. The user's software should account for the low frequency crystal's start-up time.

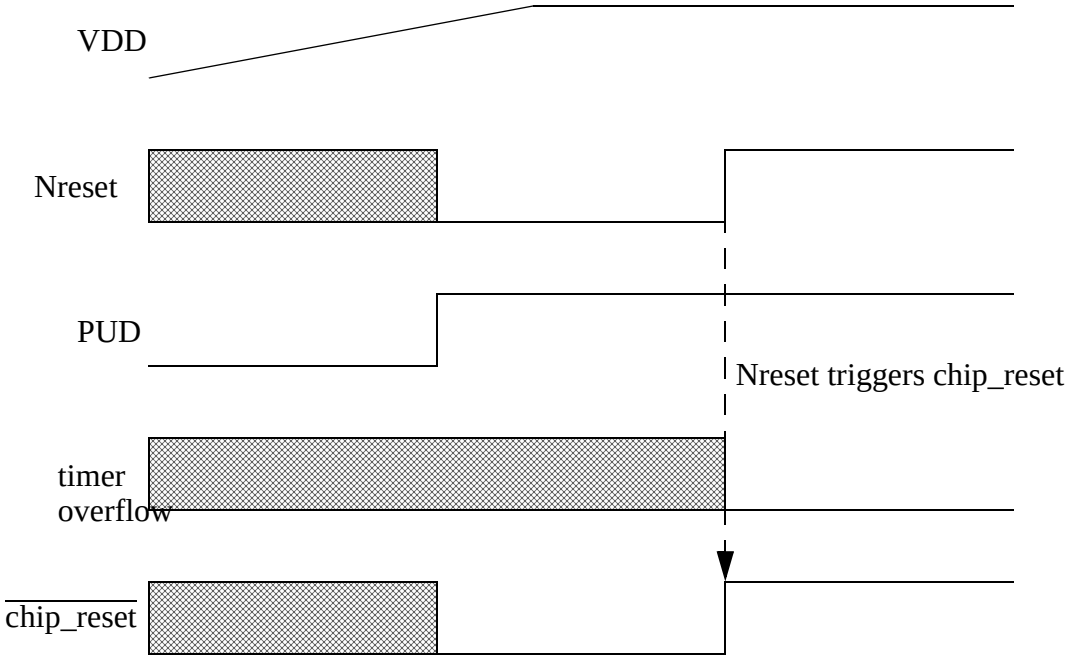


Figure 8. External Reset Asserted

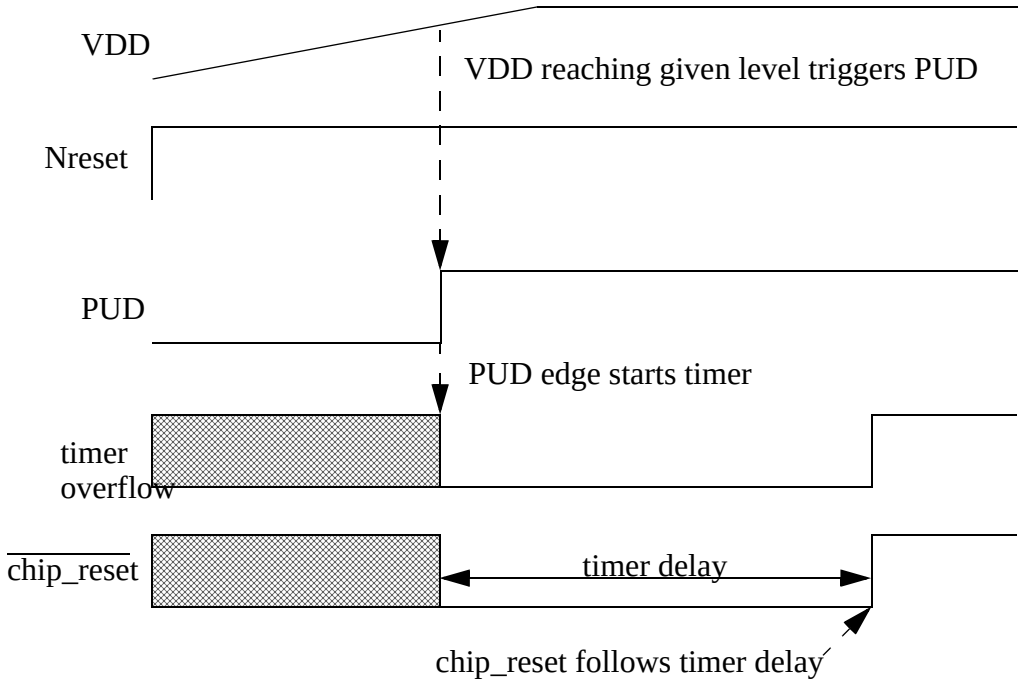


Figure 9. Internal Reset Asserted (Nreset tied to Vcc)

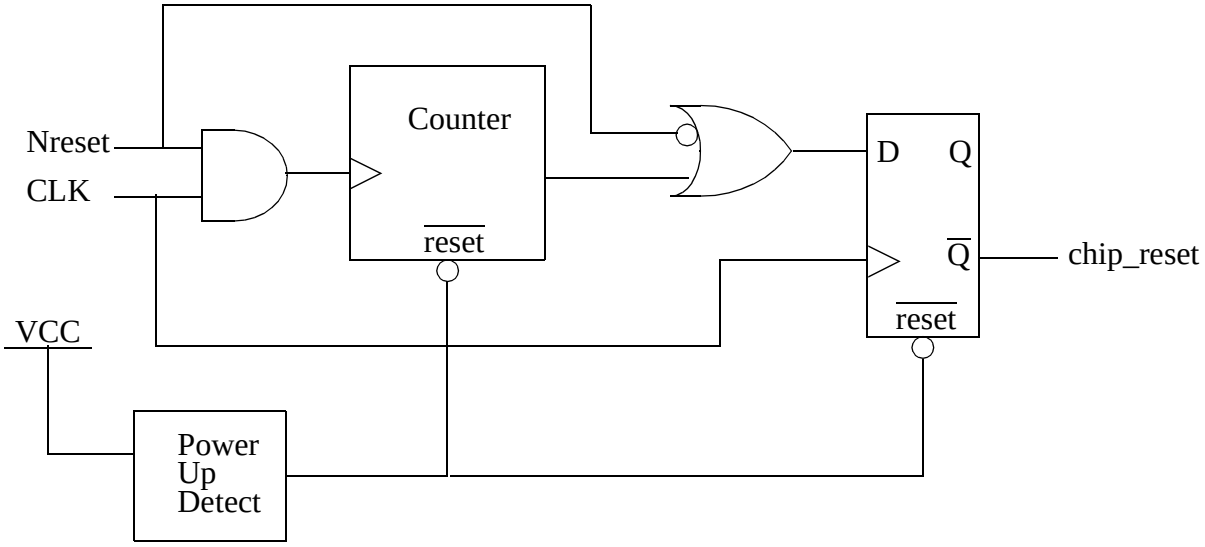


Figure 10. Power On Reset functional diagram

22. Low Battery Detect Module

22.1. Oveview

This module provides the low battery detect function when SS1103 is powered from a battery. This a 8 level programmable voltage detector. It uses resistor string, comparator and bandgap regulator as voltage reference. The block can be enabled by enabling bit 0 of LBDCR control register. The block, when enabled, will generate an interrupt when the battery voltage will fall below the following programmed level.

22.2. Low Battery Detect Module Control Register (LBDCR)

Bit/Name	7	6	5	4	3	2	1	0
LBDCR			TEST	LBDOUT	VSL2	VSL1	VSL0	EN
	R	R	R/W	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Address: 84H

Legend:

Bit7 - Bit6 Reserved. These bits always read "0".

TEST Test mode. When this bit is set to a "1" the output of the Low Battery Detect Comparator can be read at bit LBDOUT. The interrupt output of the LBD is disabled.

LBDOUT Low Battery Detect Out. When the TEST bit is set to a "1" this bit will show the status of the Low Battery Detect Comparator output. When the TEST bit is a "0" this bit reads a "0".

EN Enable. Writing a "1" to this bit enables the Low Battery Detect block. Writing a "0" to this bit disables the block and cuts the power to zero.

VSL2 - VSL0 Voltage Sense Level Select bits. These bits determine the battery voltage detect level which will generate an interrupt.

VSL2	VSL1	VSL0	Battery Voltage Level (V)
0	0	0	2.70
0	0	1	2.79
0	1	0	2.89
0	1	1	3.07
1	0	0	3.15

VSL2	VSL1	VSL0	Battery Voltage Level (V)
1	0	1	3.32
1	1	0	3.46
1	1	1	3.61

APPENDIX A

SS1103 SPECIAL MODES

1. TEST ROM (Using Auxilliary RAM)

The TEST ROM for the SS1103 is initiated by driving the TST and P4.2 pin to a high and the P4.3 pin to a low during reset. This will cause the CPU to fetch opcodes from the onchip auxilliary data ram. The ram is currently 256 bytes. The P4.3 and P4.2 pins will return to the to the general purpose I/O functions after reset has gone inactive.

To load the RAM with opcodes the user should use the “External Memory mode” described below to load the auxilliary data ram using either MOVC or MOVX commands. Then the device can be reset and placed in the test rom mode without losing the ram data.

2. ROM DUMP

To read the internal program memory using the CPU to force the address and read signals the ROM DUMP mode may be used. The mode is entered by forcing the following sequence of signals.

Drive NRESET low for four machine cycles with P4.3 high and P4.2 low.

Internally PSEN, and ALE are driven low and after two full machine cycles the PC will be reset and the device will have entered the ROM DUMP mode.

The P3.7 pin may then be used to read the program memory. Driving P3.7 low will place the data value of program memory address 00H out of P0.7-0. The PC will be incremented 2 XFIN rising edges after P3.7 has been returned high.

The full memory may then be read on P0.7-0 by the toggling of P3.7.

The memory access time should be less than 150ns.

3.0 EMULATION MODE

The SS1103 (in 128 pins package) has 22 extra bond pads on the die which are emulation interface I/O. The pins and their functions are listed below. The emulation mode is entered by driving the ENICE pin low. This causes the SS1103 to redirect program and data memory fetches through the emulation interface.

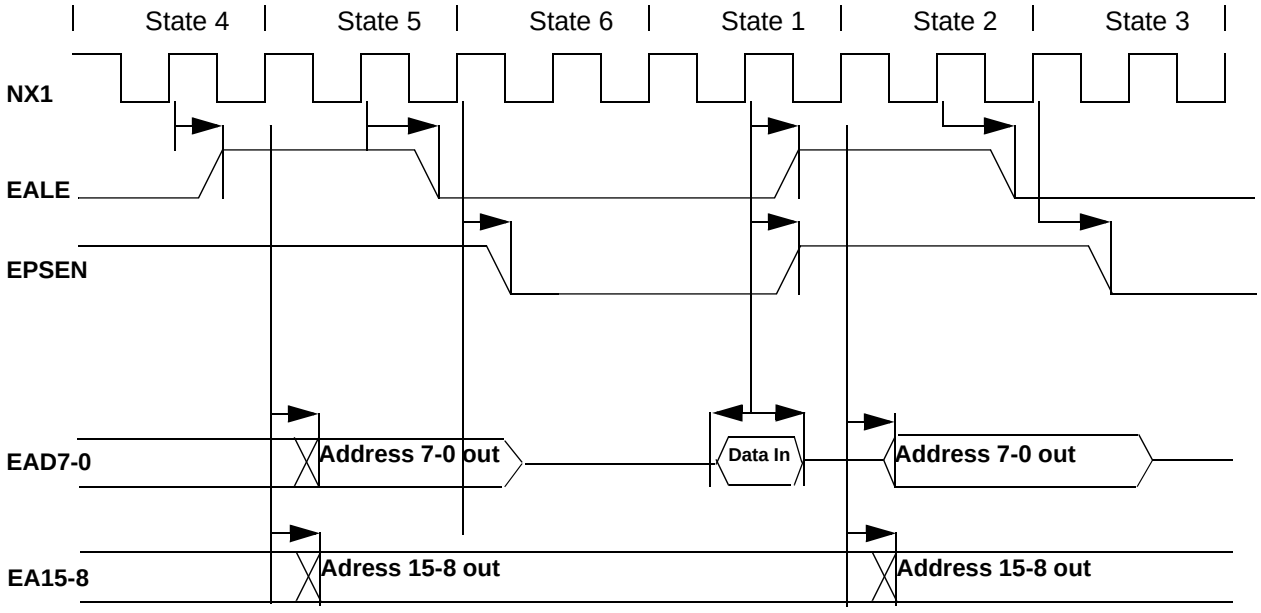
PIN	TYPE	FUNCTION
EAD7-0	I/O	Low byte address and data I/O
EA15-8	OUTPUT	High byte address
EPSEN	OUTPUT	Program store enable for program memory read active low
EALE	OUTPUT	Address latch enable
ENWR	OUTPUT	Data memory write active low
ENRD	OUTPUT	Data memory read active low
ENICE	INPUT	In circuit emulation mode input active low
ENMON	INPUT	Monitor mode active low

In normal operation the SS1103 will fetch opcodes from the internal program memory and data memory is accessed to internal IRAM and, with the MOVX command, to internal XRAM and external data RAM. When emulation mode is entered the internal IRAM continues to be accessed as in normal mode but the program memory fetches and the MOVX data memory fetches are both done through the emulation interface. At the emulation interface the internal

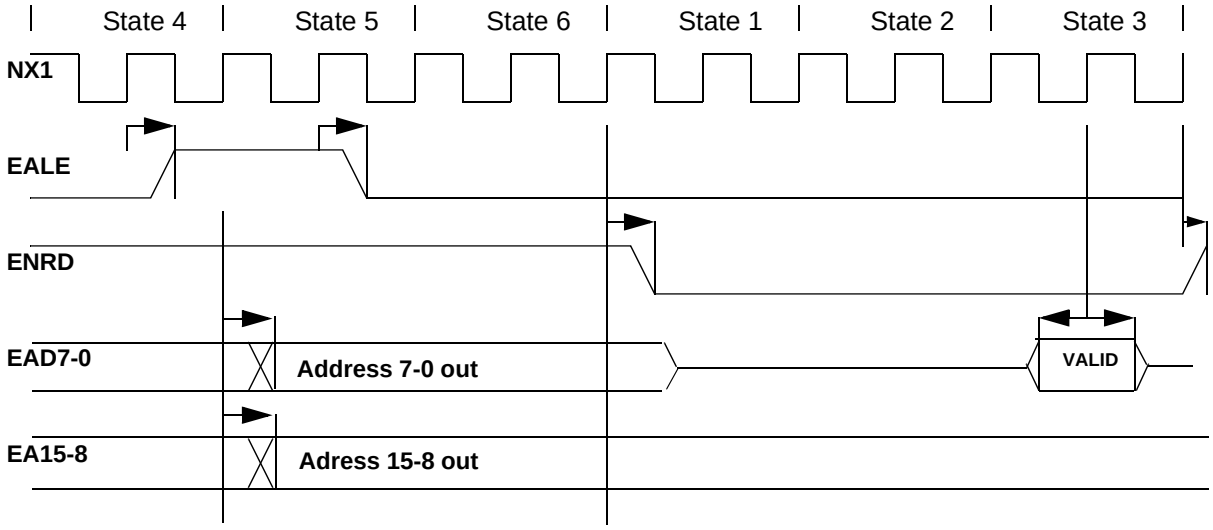
program memory fetch is made to look like an external program memory fetch and all MOVX data memory fetches either internal or external are made to look like external data memory fetches. Both of these fetches are designed to occur through the same emulation interface bus with no disturbances to the port outputs. The emulator can access the internal IRAM by using the appropriate opcodes to read and write this onchip data memory.

The ENMON input is used by the emulator to stop internal activities such as timers, interrupts, and serial I/O for exercising emulation activities such as step mode, or modifying registers etc.

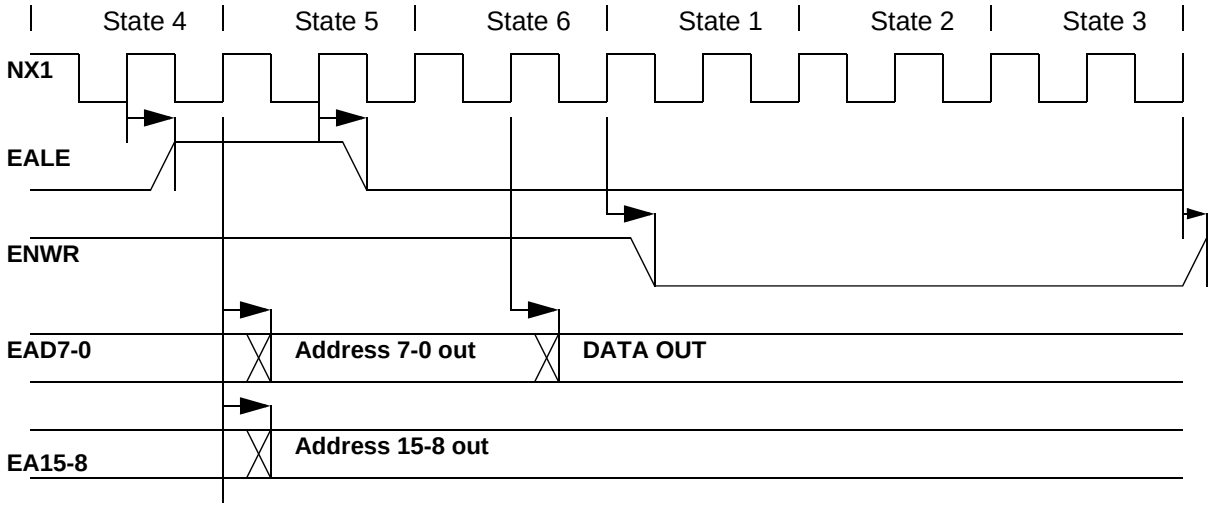
EMULATION INSTRUCTION FETCH FROM PROGRAM MEMORY



EMULATION DATA MEMORY READ



EMULATION DATA MEMORY WRITE



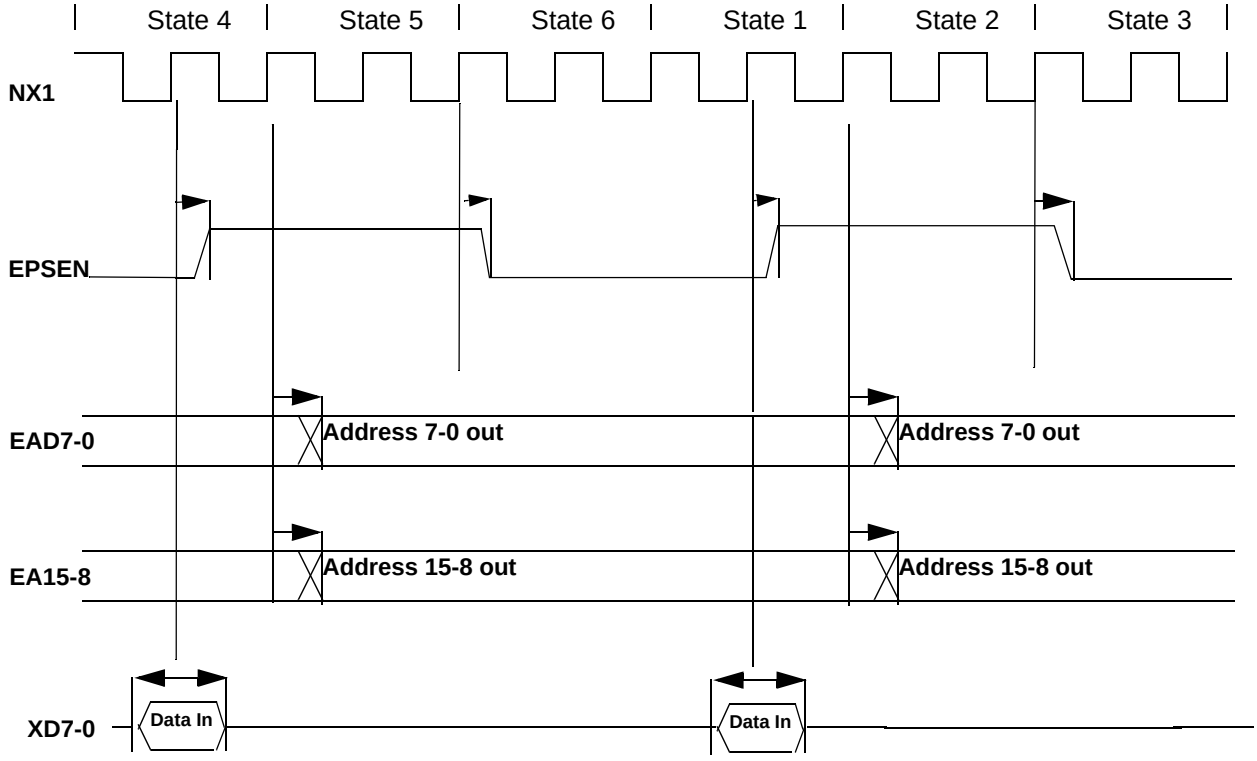
4.0 MULTICHIP PROGRAM MEMORY INTERFACE

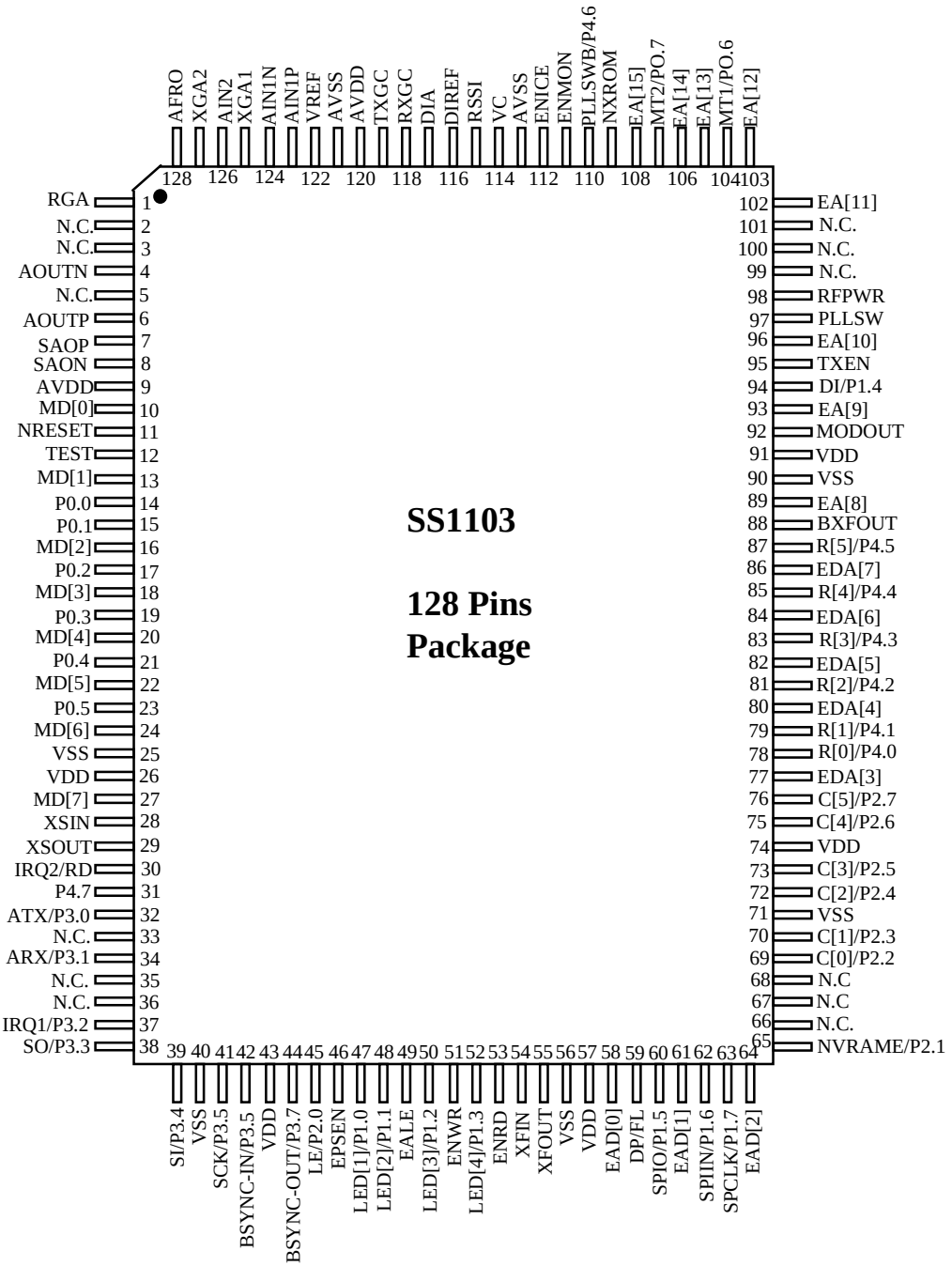
The SS1103 (in 128 pins package) has 26 extra bond pads on the die which are external ROM memory interface. The pins and their functions are listed below. Pins beginning with the letter E are shared with the emulation mode. This external rom memory mode is entered by driving the NXROM pin low. This causes the SS1103 to redirect program memory fetches through this interface. The EPSEN is the NMOE, EAD7-0 is M7-0, and EA15-8 is M15-8 function from the SM8200 core. MD7-0 is the same as the MD7-0 of the SM8200 core being the opcode input to the CPU.

9

PIN	TYPE	FUNCTION
NXROM	INPUT	Mode control
MD7-0	INPUT	Opcode data input
EAD7-0	OUTPUT	Low byte address
EA15-8	OUTPUT	High byte address
EPSEN	OUTPUT	Program store enable for program memory read active low

EXTERNAL INSTRUCTION FETCH FROM PROGRAM MEMORY




SS1103
128 Pins
Package
1 RGA
2 N.C.
3 N.C.
4 AOUTN
5 N.C.
6 AOUTP
7 SAOP
8 SAON
9 AVDD
10 MD[0]
11 NRESET
12 TEST
13 MD[1]
14 P0.0
15 P0.1
16 MD[2]
17 P0.2
18 MD[3]
19 P0.3
20 MD[4]
21 P0.4
22 MD[5]
23 P0.5
24 MD[6]
25 VSS
26 VDD
27 MD[7]
28 XSIN
29 XSOUT
30 IRQ2/RD
31 P4.7
32 ATX/P3.0
33 N.C.
34 ARX/P3.1
35 N.C.
36 N.C.
37 IRQ1/P3.2
38 SO/P3.3
39 SI/P3.4
40 VSS
41 SCK/P3.5
42 BSYNC-IN/P3.5
43 VDD
44 BSYNC-OUT/P3.7
45 LE/P2.0
46 EPSEN
47 LED[1]/P1.0
48 LED[2]/P1.1
49 EALE
50 LED[3]/P1.2
51 ENWR
52 LED[4]/P1.3
53 ENRD
54 XFIN
55 XFOUT
56 VSS
57 VDD
58 EAD[0]
59 DP/FL
60 SPIO/P1.5
61 EAD[1]
62 SPIIN/P1.6
63 SPCLK/P1.7
64 EAD[2]
65 NVRAME/P2.1
66 N.C.
67 N.C
68 N.C
69 C[0]/P2.2
70 C[1]/P2.3
71 VSS
72 C[2]/P2.4
73 C[3]/P2.5
74 VDD
75 C[4]/P2.6
76 C[5]/P2.7
77 EDA[3]
78 R[0]/P4.0
79 R[1]/P4.1
80 EDA[4]
81 R[2]/P4.2
82 EDA[5]
83 R[3]/P4.3
84 EDA[6]
85 R[4]/P4.4
86 EDA[7]
87 R[5]/P4.5
88 BXFOUT
89 EA[8]
90 VSS
91 VDD
92 MODOUT
93 EA[9]
94 DI/P1.4
95 TXEN
96 EA[10]
97 PLLSW
98 RFPWR
99 N.C.
100 N.C.
101 N.C.
102 EA[11]
103 EA[12]
104 MT1/PO.6
105 EA[13]
106 EA[14]
107 MT2/PO.7
108 EA[15]
109 NXROM
110 PLLSWB/P4.6
111 ENMON
112 ENICE
113 AVSS
114 VC
115 RSSI
116 DIREF
117 DIA
118 RXGC
119 TXGC
120 AVDD
121 AVSS
122 VREF
123 AIN1P
124 AIN1N
125 XGA1
126 AIN2
127 XGA2
128 AFRO