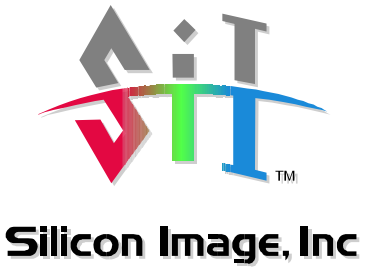

SiI100/SiI101 Datasheet

Silicon Image, Inc.

Version 1.1
June 1998

SiI/DS-0001-B

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Revision History

Revision	Date	Comment
1.0	8/97	Version 1.0 of SiI100/101 Datasheet
1.1	6/98	Version 1.1 of SiI100/101 Datasheet

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1. Feature Review

- **VESA® Standards Compliant***
  - VESA®P&D
  - VESA®PDI-2
- **Full-Color, High-Resolution Display Support**
  - Supports up to true color panels (24-bit/pixel, 16.7M color) in 1 pixel per clock mode.
  - Supports up to 18-bit/pixel panels in 2 pixels per clock mode (36-bit interface).
  - Supports VGA to XGA resolutions for TFT and VGA to SXGA resolutions for DSTN panels.
- **High Integration, Simple Interface**
  - Only 3 data channels needed *(Red, Green, Blue).*
  - One clock channel.
- **Flexible Panel Interface**
  - Single or dual pixel out: supports up to 24-bit interface (one pixel per clock mode) or 36-bit interface (two 18-bit pixels per clock cycle).
  - Up to 3 control signals (in addition to Horizontal Sync, Vertical Sync, and Display Enable signals) for supporting customized features.
  - Parallel data can be latched on the positive or the negative edge.
  - Variety of output clocking options for 24 bit DSTN support.
- **Cable Distance Support and Fiber Optics Ready**
  - Adjustable TMDS™ low-voltage swing signaling for long distance support.
  - DC-balanced signals for direct coupling to fiber-optics ready modules.
- **High Bandwidth and Reduced EMI**
  - Wide operating frequency range: 25MHz to 68MHz.
  - Three TMDS™ data channels capable of transferring up to 680Mbps per channel.
  - TMDS™ reduces high-speed data edges, lowering EMI across the cable.
  - Adjustable internal termination impedance enables optimal impedance matching crucial for high-speed signaling.
- **Skew Tolerant for Reliable Transmission**
  - High-speed data oversampling to minimize effects of signal skew and jitter.
  - Phase, byte, and multi-channel synchronization.
  - Only the frequency information of received clock is used, eliminating effect of clock-to-data skew.
  - Inter-pair skew tolerance up to 1 input clock cycle.
- **High Jitter Tolerant**
  - Jitter tolerant PLL design
  - PLL synchronization of both transmitter and receiver PLL clocks for improved jitter tolerance.
- **Low Power**
  - 3.3V core operation with 5V tolerant I/O.
  - Low-power CMOS technology.
  - Power-down mode.
- **Low Pin-Count Packages**
  - 64-pin TQFP - SiI100.
  - 80-pin TQFP - SiI101.

* As of August 1997, VESA®PDI-2 standard is in the process of completion. VESA®P&D is a standard.

2. Product Summary

Introduction

The SiI100 and SiI101 are high-speed digital video/graphics interconnect devices capable of supporting VGA to XGA resolutions for TFT panels and VGA to SXGA resolutions for DSTN LCD panels. These devices are based on Silicon Image's PanelLink™ Technology that currently enables reliable, scaleable, high-speed data transmission over the same interface, from VGA to SXGA resolutions (and up to HDTV resolution in the future). The PanelLink™ transmitter incorporates an advanced coding scheme to enable TMDS™ signaling for reduced EMI across copper cables and DC-balancing for data transmission over fiber optics. In addition, the advanced coding scheme enables robust clock recovery at the receiver to achieve high-skew tolerance for driving longer cable lengths. To maximize data recovery accuracy, the receiver triple oversamples and makes use of a data recovery algorithm to select the most reliable data sampling points.

Skew Tolerant Reliable Transmission

Valid data is sent over the three data channels during active display time, while synchronization data and embedded control signals are sent over the three data channels during blank time. After each line and frame are sent, the receiver will automatically force phase, byte, and inter-channel synchronization. Because the receiver PLL uses only the frequency information (and not the phase information) from the received clock signal, the receiver is immune to clock-to-data skew and extremely tolerant to data-to-data skew. This provides a robust transmission system for driving long cables.

Design Flexibility

PanelLink™ Technology enables notebook and FPD monitor designers to use one motherboard and one panel interface design to support resolutions from VGA (640x480) all the way up to XGA (1024x768) with true color support (16.7 million colors) for TFT panels, and up to SXGA (1280x1024) for DSTN panels. In addition, panel manufacturers will benefit from PanelLink™ Technology by having the choice of one pixel per clock or two pixels per clock on the output data pins of the SiI101 receiver. Also, three control lines are available for supporting additional differentiating features that may exist on the panel side. *(Future SiI products will maintain the same interface for forward compatibility).*

Reduced EMI

PanelLink™ Technology helps manage EMI from both a *fundamental* and *advanced* perspective.

Fundamental approach (common practice):

The *Fundamental* approach for lowering EMI is to send data using low voltage differential swing (LVDS) signaling.

Advanced approach (unique to PanelLink™):

PanelLink™ Technology builds on LVDS and further codes the data to reduce the number of high frequency signal edges of each transmitted data byte by 22% on average, which is the basis of TMDS™. And, PanelLink™ Technology provides on-chip termination resistors at the receiver to optimize the interconnect system impedance, helping reduce EMI signal reflection on the cable.

Reduced Power

PanelLink™ Technology reduces power consumption by using 3.3V low-power CMOS technology. Because the transmitter and receiver are designed in industry standard CMOS technology, they can be integrated into video/panel controllers, further reducing power and EMI.

Fiber Optics Support

The coding scheme permits DC-balancing for AC coupling, enabling separate power supplies for the transmitter and receiver, with good isolation.

High Jitter Tolerance

PanelLink™ Technology has a leading edge jitter tolerant PLL design. In addition, PanelLink™ employs PLL synchronization, which forces both the transmitter and receiver PLL's to respond similarly to an input jitter, thus improving jitter tolerance.

3. Order Information

	Part Number	Order Information
• Production Version of the Transmitter	SiI100	SiI100CT64V351
• Production Version of the Receiver	SiI101	SiI101CT80V360

For more information, please contact:

• Silicon Image web-site:	www.siimage.com	
• Silicon Image main phone number:	888-PanelLink	(within US and Canada)
	+1-408-873-3111	(outside of US and Canada)

4. PanelLink™ Technology Overview

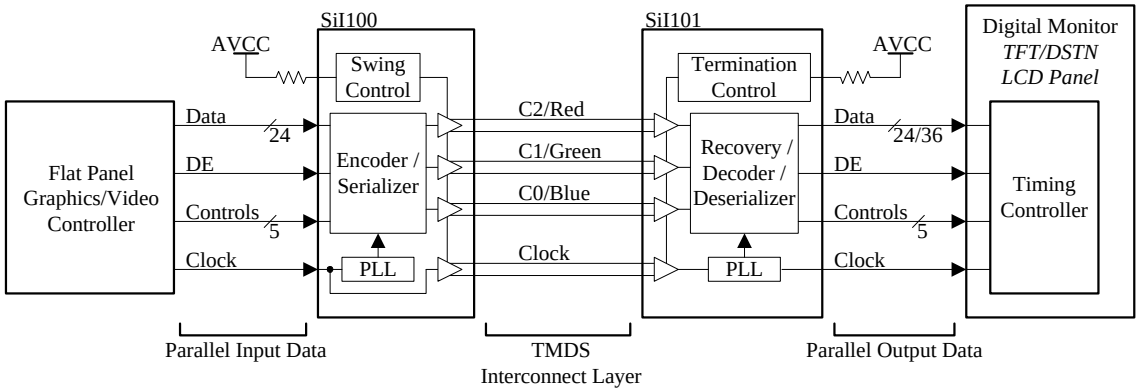

Figure 1. PanelLink™ Block Diagram

The SiI100 and SiI101 are high speed digital video interconnect devices for sending video data to digital displays, such as TFT or DSTN Liquid Crystal Displays (LCD). A block diagram of the transmission system is shown in Figure 1.

The transmitter (SiI100) receives parallel digital video data from a host graphics controller. Through the use of an internal PLL, the SiI100 encodes and serializes the parallel input data. The serialized data is then transmitted to the SiI101 receiver chip over the Transition Minimized Differential Signaling (TMDS™) interconnect layer.

The TMDS™ interconnect layer consists of three high speed data channels, C2, C1 and C0 (red, green and blue, respectively) and one low speed clock channel. These signals are sent over four low voltage differential channels, the amplitude of which is set by the swing control circuit of the SiI100. The high speed data channels have a bandwidth equal to ten times the SiI100 input clock frequency, while the differential clock channel has the same frequency as the input clock. For example, if the input clock is 65 MHz, the output channels are 650 Mbps (megabits per second) and the differential clock channel is 65 MHz. These signals may be sent over a variety of physical medium, such as flex or twisted pair cables. In particular, the encoding of the serial channels is DC balanced, which is required in order for the channels to be capacitive coupled to fiber optic links or systems with independent ground potentials.

The SiI101 receives the serial data and clock from the SiI100. The differential signals are terminated by voltage controlled resistors internal to the SiI101. The value of the resistors is set by the termination control circuit. The differential clock is used only as a frequency reference to an internal PLL in the SiI101. The output of this PLL circuit is used to three times oversample the serial data channels. The oversampling and encoding enable the data recovery circuits to:

1. Determine the correct sampling point of each data channel individually. That is, the correct sampling point of each high speed channel is found independently from those of the other two data channels.
2. Determine the frame boundaries on each serial channel individually. The frame boundaries (also referred to as byte boundaries) are the locations within a serial data stream where the data for one byte ends and the data for then next byte begins.
3. Re-synchronize the three data channels to a single PLL generated clock. This re-synchronization corrects for inter-channel time skews up to one input clock cycle.

The synchronized data is then decoded back to the original parallel data. The SiI101 provides options to output the data at one 24 bit pixel per clock at the normal clock frequency, or in two 18 bit pixels per clock at half the clock frequency.

5. SiI100 Overview

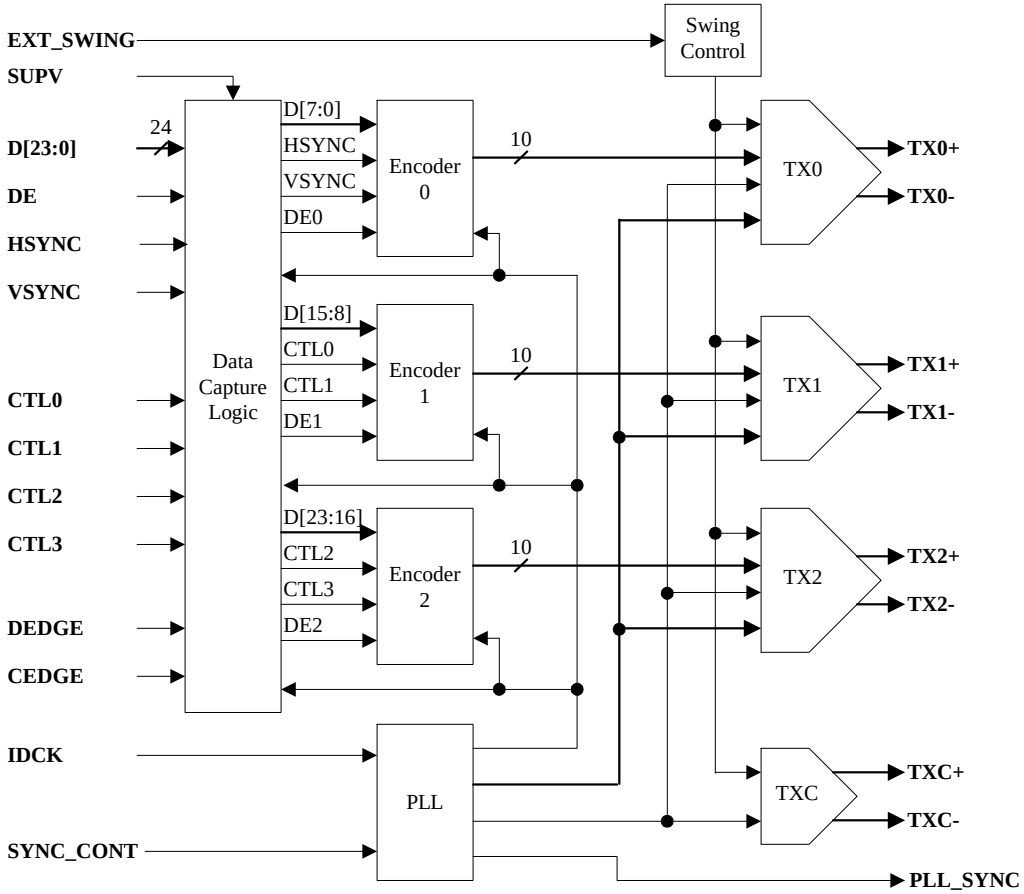

Figure 2. SiI100 Functional Block Diagram

Four major blocks of the SiI100 will be discussed below: Data Capture Logic, Encoders, Data and Clock Transmitters, and Swing Control.

Data Capture Logic

The data capture logic captures 24-bit RGB data (D[23:0]), 6 control signals (HSYNC, VSYNC, and CTL[3:0]), and data enable (DE) from the Graphics controller. Data and control signals can be latched on the rising or falling edge of IDCK depending on the state of the DEDGE and CEDGE configuration inputs respectively.

Encoders

Each encoder receives 8-bit data, 2 control signals, and a DE signal from the Data Capture Logic. When DE is HIGH (active display time), 8-bit data is converted to 10-bit coded data. The encoding guarantees DC-balanced and transition-minimized serial streams over the data channels during the active data period. When DE is LOW (blank time), 2-bit control signals are embedded into 10-bit synchronization control characters. The special characters enable the receiver to synchronize during every blank time (see the description of the SiI101 for a more complete description of what happens during synchronization).

Data and Clock Transmitters (TX[2:0], TXC)

The three data transmitters convert the 10-bit coded data into a serial data stream. The maximum data rate of the data channels is ten times the input clock frequency. For example, for a 65 MHz input clock, the serial data channels transmit 650 Mbps. The input clock is converted directly to a pair of low voltage differential signals and sent to the receiver. Therefore, the transmitted clock has the same frequency as the input clock.

Swing Control

The amplitude of the differential voltage swing is adjustable through the EXT_SWING pin of the SiI100. A series resistor placed between AVCC and EXT_SWING controls the swing amplitude. The larger the voltage swing, the better the signal to noise level, but the higher the power consumption of the cable driving circuit. The following settings are recommended for these common applications:

R_{EXT_SWING} = 680 Ω for short cable lengths, such as for computer laptops.

R_{EXT_SWING} = 400 Ω for long cable lengths, such as for desktop monitors.

5.1 Data Input

The following vertical and horizontal timing diagrams demonstrate the relationship between the data, control and clock signals input to the SiI100's parallel interface.

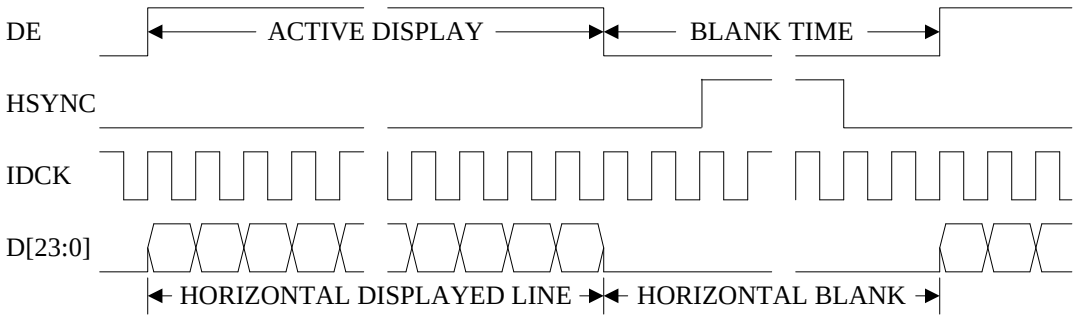

Figure 3. Horizontal Input Timing

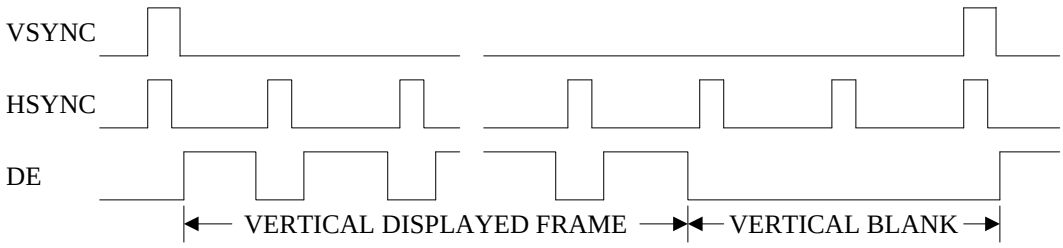

Figure 4. Vertical Input Timing

In the above figures, DE, HSYNC, and VSYNC signals are shown with positive polarity. DE must always have positive polarity, whereas HSYNC, VSYNC and the other control signals (CTL[3:0]) can have either positive or negative polarity. Since the encoding scheme is based on DE, this signal is always required. Because the state of the control signals, other than DE, are coded during the blanking time, the control signals must only transition during the blanking time. Any transitions of these control signals during the active data period will be ignored by the transmission link.

Input data D[23:0] and Data Enable (DE) are normally generated on the rising edge of IDCK by the graphics controller, since most panels latch data on the falling edge of the shift clock. For the SiI100, D[23:0] and DE can be latched on the rising or the falling edge of IDCK depending upon the setting of DEDGE and CEDGE, respectively.

6. SiI101 Overview

The following figure shows the SiI101 functional block diagram:

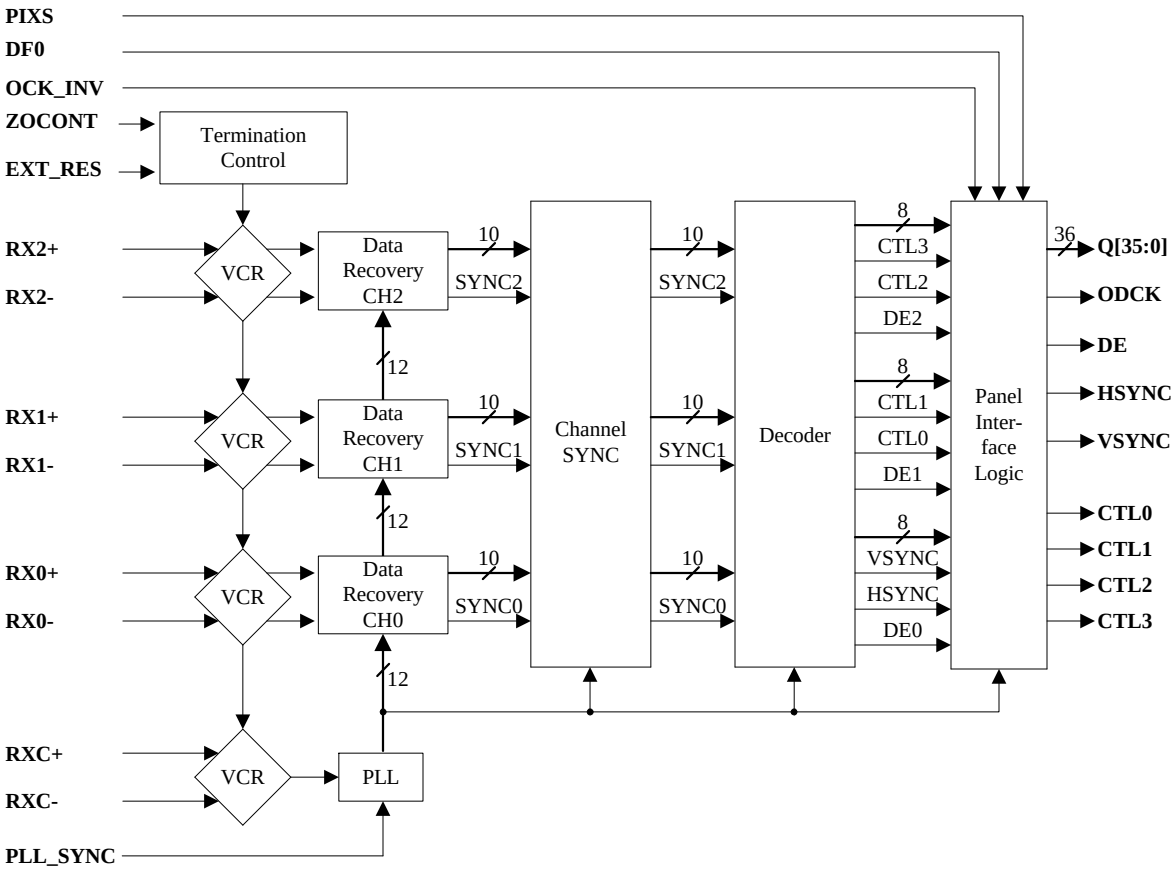

Figure 5. SiI101 Functional Block Diagram

Five major blocks of the SiI101 will be discussed below: Termination Control, Data Recovery, Channel Synchronization, Decoder, and the Panel Interface Logic.

Termination Control

All differential input channels are terminated by a VCR (Voltage Controlled Resistor), which is controlled by an adjustable impedance matching circuit. The VCR removes signal reflection on each line caused by an impedance mismatch between the cable and the inputs to the SiI101 sampling circuitry. The value of the termination is set by the value of a single resistor placed between the EXT_RES pin of the SiI101 and the AVCC supply. The value of this resistor should be set to ten times the single-ended characteristic impedance of the transmission media. In most cases, the characteristic impedance is 50 Ω, so the external resistor should be set to 500 Ω. The ZOCONT configuration pin can be used to account for characteristic impedance of greater than or equal to 50 Ω (ZOCONT set low) and characteristic impedance of less than or equal to than 50 Ω (ZOCONT set high). For most cases, Silicon Image recommends setting ZOCONT high.

Data Recovery

The Data Recovery Block receives the high speed serial data from the transmitter. During horizontal or vertical blank time (when DE is LOW), one of four possible special characters are received. The data recovery block

differentiates the special characters from data characters by the number of transitions it detects. Each channel uses the PLL clock outputs to triple oversample the serial data. The phase tracking circuitry within the data recovery block, dynamically determines the best sampling point among the three sampling points. Also, the special codes enable the frame boundaries to be identified. Each 10 bit frame, during the active data period, is comprised of an encoded data byte (9 bits) and 1 coded bit for DC balancing. The phase and frame information, determined during the blanking time, is locked in and used for data recovery during the active data period. This information remains locked in until the next blanking period at which point it is reevaluated. The data recovery block treats each channel individually, meaning that the phase and byte information are generated for each channel. This enables the data channels to be skewed relative to each other with no adverse effect. The Data Recovery Block further converts the serial data streams to 10-bit parallel output streams from the frame boundary information.

Channel Synchronization

In the Channel Synchronization Block, the three data channels are re-synchronized to a single clock. The synchronization block aligns the channels up to a worse case skew of one input clock cycle (15ns at 65MHz).

Decoder

The Decoder Block receives 10-bit data and Sync signals from the Channel Synchronization Block, and then decodes the data to 8-bit RGB data, 2-bit control signals and a DE (Data Enable) signal.

Panel Interface Logic

The Panel Interface Logic is used to output the parallel data and control signals. The SiI101 data output is configurable for two output modes by the PIXS pin. When PIXS is LOW, the data output is one pixel per clock (24-bits per pixel, synchronized to the ODCK clock output). When PIXS is HIGH, the data output is in two pixels per clock mode (two 18 bits pixels, synchronized to a half frequency ODCK). The next two sections show the timing of these data output modes and the data mapping to use for these modes.

The SiI101 is also configurable for normal ODCK output or inverted ODCK output set by the OCK_INV configuration pin. The configuration pin DF0 selects whether the output clock is blanked (low) during the DE low period or whether the output clock is free running. Many passive DSTN panels make use of the blanked clock output mode. Additional options for dividing the output clock frequency are available in 24-bit DSTN mode (DF0 high), which are described in Section 6.3. The following table summarizes the clock output modes as a function of DF0, PIXS, and OCK_INV.

DF0	PIX	OCK_INV	PANEL	ODCK (frequency/data latch edge/mode)
0	0	0	TFT/16-bit DSTN	divide by 1 / negative / free running
0	0	1	TFT/16-bit DSTN	divide by 1 / positive / free running
0	1	0	TFT	divide by 2 / negative / free running
0	1	1	TFT	divide by 2 /positive / free running
1	0	0	24-bit DSTN	divide by 1 / negative / blanked low
1	0	1	**NONE**	divide by 1 / negative / blanked high
1	1	0	24-bit DSTN	divide by 2 / negative / blanked low
1	1	1	24-bit DSTN	divide by 4 / negative / blanked low

Table 1. Output Clock Configuration by Typical Application

6.1 Output Modes

6.1.1 One Pixel Per Clock Mode

When the PIXS configuration input is low, the output data format is 24-bit per ODCK on the data output pins Q[23:0]. The timing relationship between the ODCK, DE and the output data, when PIXS and OCK_INV pins are low, is shown in the following timing diagram. When OCK_INV is high the output clock is inverted from the clock shown in the figure below.

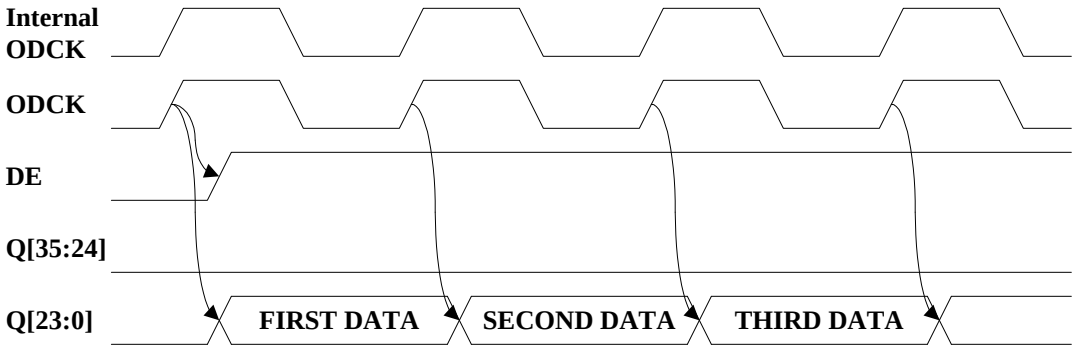

Figure 6. One Pixel/Clock Timing with OCK_INV = Low

6.1.2 Two Pixels Per Clock Mode

When the PIXS pin is high and the OCK_INV pin is low, two pixels per clock are generated and ODCK is run at half frequency. In this mode, the output data format is 36-bit per ODCK and 18-bits per pixel. In this configuration, the two least significant bits for each byte of output data is discarded (not used). The first pixel data is output on Q[17:0] pins and the second pixel data is output on Q[35:18] pins as shown below. When OCK_INV is high the output clock is inverted from the clock shown in the figure below.

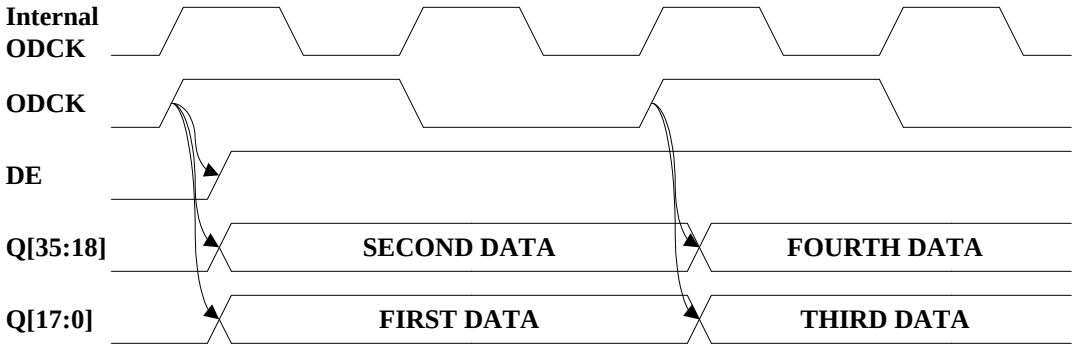

Figure 7. Two Pixels/Clock Timing with OCK_INV = Low

6.2 Data Mapping (TFT) - VESA® Compatible

6.2.1 One Pixel Per Clock Data Mapping

The following table shows the output data mapping in one pixel per clock mode for the connections from the SiI100 to the SiI101. Note that the three data channels (CH0, CH1 and CH2) are mapped to blue, green and red data respectively.

	SiI100			SiI101		
	1 Pixel/Clock			1 Pixel/Clock		
	12bpp	18bpp	24bpp	12bpp	18bpp	24bpp
CH0	D[7:4]	D[7:2]	D[7:0]	Q[7:4]	Q[7:2]	Q[7:0]
(BLUE)	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
CH1	D[15:12]	D[15:10]	D[15:8]	Q[15:12]	Q[15:10]	Q[15:8]
(GREEN)	CTL0	CTL0	CTL0	CTL0	CTL0	CTL0
	CTL1	CTL1	CTL1	CTL1	CTL1	CTL1
CH2	D[23:20]	D[23:18]	D[23:16]	Q[23:20]	Q[23:18]	Q[23:16]
(RED)	CTL2	CTL2	CTL2	CTL2	CTL2	CTL2
	CTL3	CTL3	CTL3	CTL3	CTL3	CTL3

Table 2. One Pixel/Clock Mode Data Mapping from SiI100 to SiI101

Note: For 18/12-bit mode, the LCD Graphics Controller interfaces to the SiI100 exactly the same as in the 24-bit mode; however, 6/4 bits per channel (color) are transmitted instead of 8. It is recommended that unused data bits be tied low.

Note: As can be seen from the above table, the data mapping for less than 24-bit per pixel interfaces are MSB justified.

6.2.2 Two Pixels Per Clock Data Mapping

The following table shows the output data mapping for two pixels per clock from the SiI100 to the SiI101. Pixel N to Pixel N+3, represent four consecutive input pixels to the SiI100. Pixels M and M+1 represent two consecutive parallel outputs of the SiI101, in two pixels per clock mode.

	SiI100		**SiI101**	
	1 Pixel/Clock		**2 Pixel/Clock**	
	12bpp	**18bpp**	**12bpp**	**18bpp**
(Pixel N)	**IDCK[N]**		**ODCK[M]**	
CH0 (blue)	D[7:4]	D[7:2]	Q[5:2]	Q[5:0]
CH1 (green)	D[15:12]	D[15:10]	Q[11:8]	Q[11:6]
CH2 (red)	D[23:20]	D[23:18]	Q[17:14]	Q[17:12]
(Pixel N+1)	**IDCK[N+1]**		**ODCK[M]**	
CH0 (blue)	D[7:4]	D[7:2]	Q[23:20]	Q[23:18]
CH1 (green)	D[15:12]	D[15:10]	Q[29:26]	Q[29:24]
CH2 (red)	D[23:20]	D[23:18]	Q[35:32]	Q[35:30]
(Pixel N+2)	**IDCK[N+2]**		**ODCK[M+1]**	
CH0 (blue)	D[7:4]	D[7:2]	Q[5:2]	Q[5:0]
CH1 (green)	D[15:12]	D[15:10]	Q[11:8]	Q[11:6]
CH2 (red)	D[23:20]	D[23:18]	Q[17:14]	Q[17:12]
(Pixel N+3)	**IDCK[N+3]**		**ODCK[M+1]**	
CH0 (blue)	D[7:4]	D[7:2]	Q[23:20]	Q[23:18]
CH1 (green)	D[15:12]	D[15:10]	Q[29:26]	Q[29:24]
CH2 (red)	D[23:20]	D[23:18]	Q[35:32]	Q[35:30]

Table 3. Two Pixels/Clock Output Data Mapping

Note: In 36-bit mode, the frequency of IDCK of the SiI100 is 2x that of ODCK of the SiI101. The 2 LSBs of 8-bit decoded data will be ignored to generate 18 (3x6) bit pixels. As shown in the mapping diagram, even numbered pixels (Pixel 0, 2, 4, ….) are received via Q[17:0], and odd numbered pixels (Pixel 1, 3, 5, …) are received via Q[35:18].

Note: As can be seen from the above table, the data mapping for less than 18-bit per pixel interfaces are MSB justified.

6.3 Output Clock Modes for 24-bit DSTN

The following timing diagrams show the clock output timing for the DF0 = 1 modes. These modes are most useful for 24-bit Color DSTN panel support. The internal clock depicted in each figure has the same frequency as the input clock IDCK (i.e. one pixel per clock frequency), and is shown for comparison to the output clock timing.

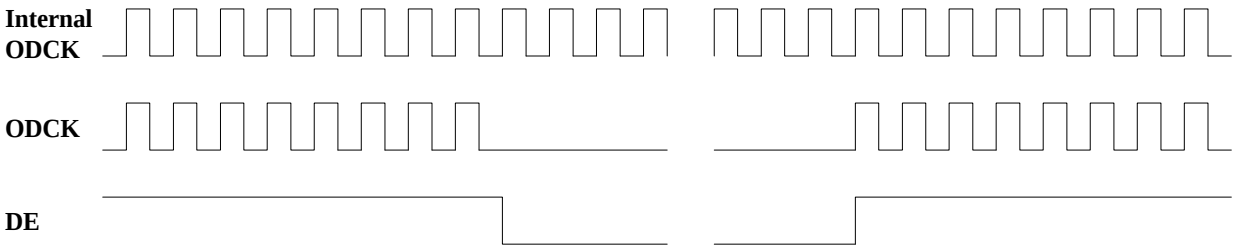

Figure 8. ODCK Timing with DF0 High, PIXS Low, and OCK_INV Low

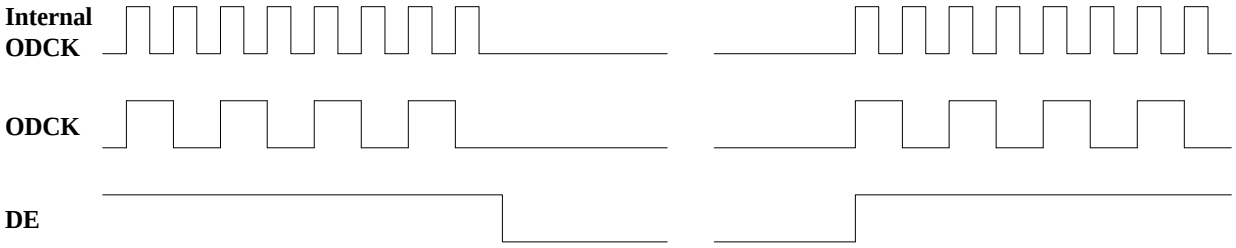

Figure 9. ODCK Timing with DF0 High, PIXS High, and OCK_INV Low

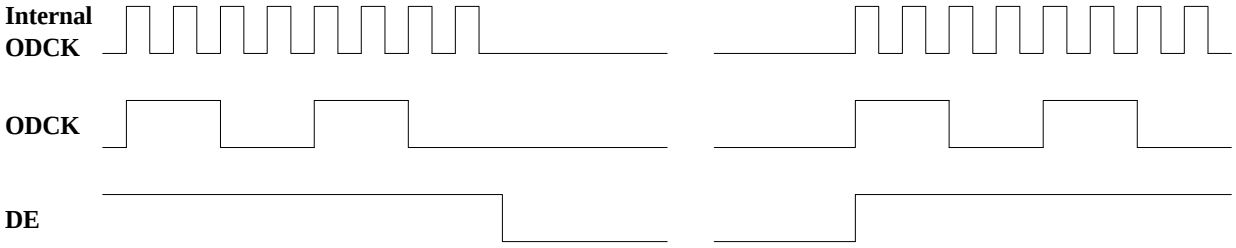

Figure 10. ODCK Timing with DF0 High, PIXS High, and OCK_INV High

6.4 Data Mapping (DSTN) - VESA® Compatible

Input Data Pin	24-bit	16-bit	Output Data Pin	24-bit	16-bit
D0	UR0	UR0	Q0	UR0	UR0
D1	UG0	UG0	Q1	UG0	UG0
D2	UB0	UB0	Q2	UB0	UB0
D3	LR0	UR1	Q3	LR0	UR1
D4	LG0	LR0	Q4	LG0	LR0
D5	LB0	LG0	Q5	LB0	LG0
D6	UR1	LB0	Q6	UR1	LB0
D7	UG1	LR1	Q7	UG1	LR1
D8	UB1	UG1	Q8	UB1	UG1
D9	LR1	UB1	Q9	LR1	UB1
D10	LG1	UR2	Q10	LG1	UR2
D11	LB1	UG2	Q11	LB1	UG2
D12	UR2	LG1	Q12	UR2	LG1
D13	UG2	LB1	Q13	UG2	LB1
D14	UB2	LR2	Q14	UB2	LR2
D15	LR2	LG2	Q15	LR2	LG2
D16	LG2	Shift CLK	Q16	LG2	Shift CLK
D17	LB2		Q17	LB2	
D18	UR3		Q18	UR3	
D19	UG3		Q19	UG3	
D20	UB3		Q20	UB3	
D21	LR3		Q21	LR3	
D22	LG3		Q22	LG3	
D23	LB3		Q23	LB3	
IDCK	Pixel CLK or Pixel CLK/2	Pixel CLK	ODCK	Pixel CLK/4 or Pixel CLK/2 (Shift CLK)	Pixel CLK
VSYNC	FLM	FLM	VSYNC	FLM	FLM
HSYNC	LP	LP	HSYNC	LP	LP
DE	DE	DE	DE	DE	DE

	24-bit	16-bit
CHANNEL 0	D[7:0]/Q[7:0]	D[7:0]/Q[7:0]
	HSYNC, VSYNC	HSYNC, VSYNC
CHANNEL 1	D[15:8]/Q[15:8]	D[15:8]/Q[15:80]
	PLL_SYNC, CTL1	PLL_SYNC, CTL1
CHANNEL 2	D[23:16]/Q[23:16]	D[23:16]/Q[23:16]
	CTL2, CTL3	CTL2, CTL3

Table 4. DSTN Data Mapping

Note:
The clock input to IDCK must be free running. For 16-bit DSTN support, the SiI101 must be in 1 pixel/clock mode (PIXS=0) and DF0 must be set low. This enables the panel shift clock to be sent over the unused data pin Q16, as shown above. For 24-bit DSTN support, the SiI101 must be in 24-bit DSTN mode (DF0=1). In this mode the panel shift clock is recreated on the ODCK output by programming PIXS and OCK_INV (see Table 1). The panel shift clock (ODCK) can be divided by either 2 or 4 depending on IDCK frequency.

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7. TMDS™ Interconnect Layer

The TMDS™ Interconnect Layer refers to the electrical and physical connection between the transmitter and receiver. Typically, the physical media for this layer is a twisted pair or flex cable. PanelLink™ technology uses current mode to electrically drive the cable of the TMDS™ Interconnect Layer. In the following figure, the cable driving circuit between the transmitter and receiver is shown. The signal voltage is developed by pulling down the cable potential through the pull down devices at the transmitter side. The receiver contains the pull-up device which is a voltage controlled resistor that provides termination to AVCC. The actual signal voltage will therefore pull-down from AVCC (nominally 3.3V) as shown in Figure 12.

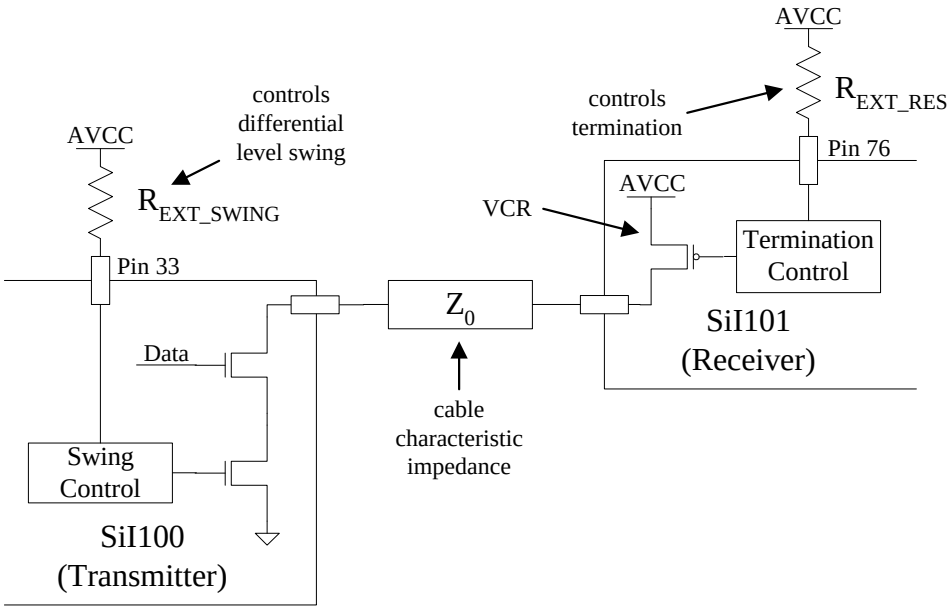

Figure 11. Differential Signaling Circuit

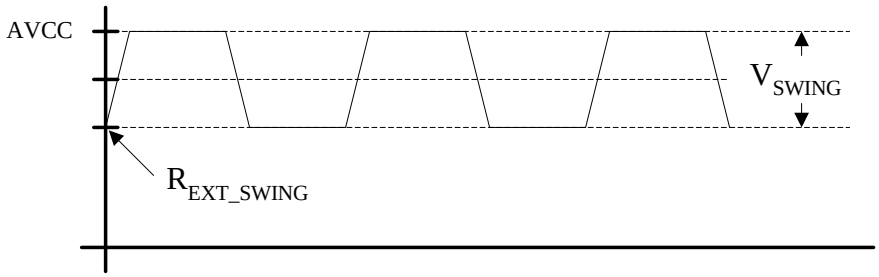

Figure 12. Single-Ended Low Voltage Differential Signal Adjustment

7.1 Voltage Swing Control (EXT_SWING)

The amplitude of the differential voltage swing is adjustable through the EXT_SWING pin of the SiI100. A series resistor placed between AVCC and EXT_SWING controls the swing amplitude. The functional relationship between the resistor value and the voltage swing is approximately given by:

$$\mathbf{V_{SWING} = 0.5V \times (500\Omega / R_{EXT\_SWING})}$$ where V_{SWING} = Single-ended differential voltage swing.

R_{EXT_SWING} = External resistor on EXT_SWING pin.

The larger the voltage swing, the better the signal to noise ratio, but the higher the power consumption of the cable driving circuit. The following settings are recommended for these common applications:

R_{EXT_SWING} = 680 Ω for short cable lengths, such as for computer laptops.

R_{EXT_SWING} = 400 Ω for long cable lengths, such as for desktop monitors.

7.2 Termination Control (EXT_RES)

The value of the termination is set by the value of a single resistor placed between the EXT_RES pin of the SiI101 and the AVCC supply. The value of this resistor should be set to ten times the single-ended characteristic impedance of the transmission media. In most cases, the characteristic impedance is 50 Ω, so the external resistor should be set to 500 Ω. The ZOCONT configuration pin can be used to account for characteristic impedance of greater than or equal to 50 Ω (ZOCONT set low) and characteristic impedance of less than or equal to than 50 Ω (ZOCONT set high). In most cases, ZOCONT high is recommended.

8. PLL Synchronization

PanelLink™ technology uses a PLL synchronization feature to make the link more robust to IDCK clock jitter and supply noise. PLL synchronization ensures that the transmitter and receiver PLLs respond to clock jitter and system noise with the same phase. This synchronization is accomplished by generating a sync signal (PLL_SYNC) based on the VSYNC control input to the SiI100, PLL_SYNC is independent of the polarity or the VSYNC input. The PLL_SYNC signal needs to be sent from the SiI100 to the SiI101 for the synchronization to be enabled. While this signal can be routed directly from the transmitter to the receiver, Silicon Image strongly recommends that the PLL_SYNC signal be sent over the auxiliary control line CTL0. In this way, no extra interconnect lines are required and delays due to the transmission distance will be automatically compensated. Silicon Image has reserved CTL0 for this purpose. To be compatible with future PanelLink™ products and VESA® P&D, PLL_SYNC must be sent over CTL0. The following figure shows how to send PLL_SYNC over the CTL0 control line.

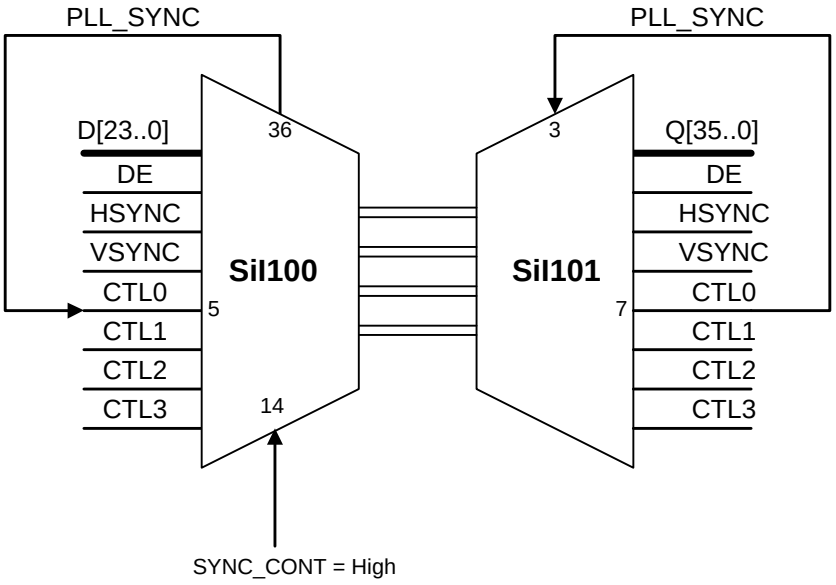

Figure 13. How to send PLL_SYNC over CTL0

9. SiI100 Pin Description

9.1 SiI100 Pin Diagram

The SiI100 is available in a 64-pin 10mm x 10mm TQFP package.

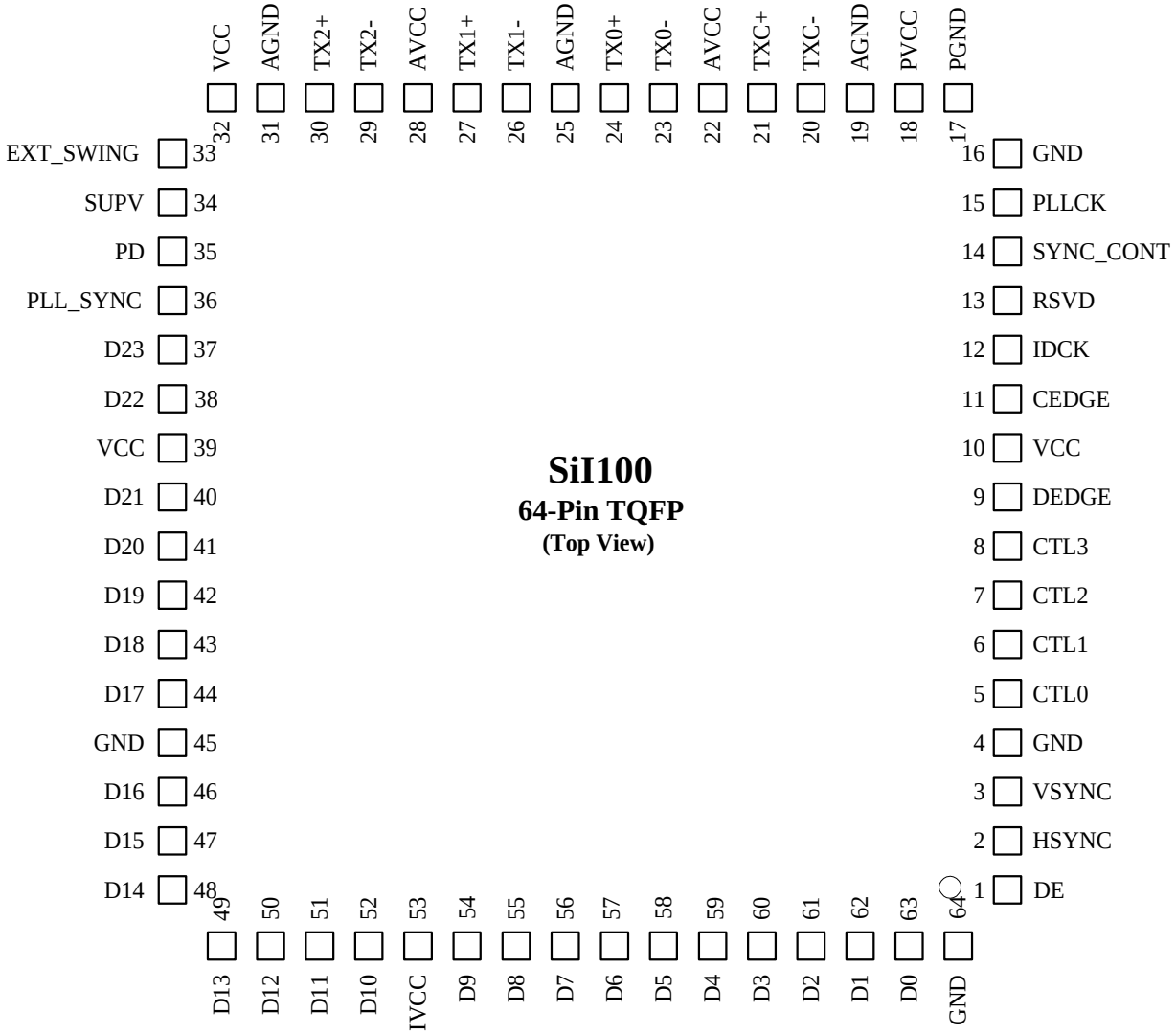

Figure 14. SiI100 Pin Diagram

9.2 SiI100 Pins Grouped by Functionality

9.2.1 SiI100 Input Pin Description

Pin Name	Pin #	Type	Description
D23	37	In	Input Data[23:0].
D22	38	In	Input data is synchronized with input data clock (IDCK).
D21	40	In	
D20	41	In	Refer to Signal Mapping Section 6.2 for description of data coordination between
D19	42	In	data in for SiI100 and data out for SiI101.
D18	43	In	
D17	44	In	
D16	46	In	
D15	47	In	
D14	48	In	
D13	49	In	
D12	50	In	
D11	51	In	
D10	52	In	
D9	54	In	
D8	55	In	
D7	56	In	
D6	57	In	
D5	58	In	
D4	59	In	
D3	60	In	
D2	61	In	
D1	62	In	
D0	63	In	
IDCK	12	In	Input Data Clock. Input data can be valid either on the falling or on the rising edge of IDCK as selected by DEDGE pin.
DE	1	In	Input Data Enable. This signal qualifies the active data period. DE is always required by the SiI100 and must be high during active display time and low during blank time.
HSYNC	2	In	Horizontal Sync input control signal.
VSYNC	3	In	Vertical Sync input control signal.
CTL0	5	In	Reserved control signal, which should be connected to PLL_SYNC (pin 36).
CTL1	6	In	General input control signal 1.
CTL2	7	In	General input control signal 2.
CTL3	8	In	General input control signal 3.

9.2.2 SiI100 Test Output Pin Description

Pin Name	Pin #	Type	Description
PLLCK	15	Out	Internal PLL Clock Output. The operating frequency is 2.5 times that of IDCK. This signal is for test purposes only, and should be left unconnected. To probe this signal output, a 500 Ω pull down resistor must be connected between this pin and ground.

9.2.3 SiI100 Synchronization Pin Description

Pin Name	Pin #	Type	Description
PLL_SYNC	36	Out	PLL Synchronization. Generated every VSYNC to force synchronization of both transmitter and receiver PLL clocks. This pin must be connected to pin 5 (CTL0) to enable the PLL synchronization feature.

9.2.4 SiI100 Configuration Pin Description

Pin Name	Pin #	Type	Description
DEDGE	9	In	Data Latching Edge. A low level indicates that input data (D[23:0]) will be latched on the falling edge of IDCK while a high level (3.3V) indicates that input data will be latched on the rising edge of IDCK.
CEDGE	11	In	Control Latching Edge. Controls latching edge of control signals DE, HSYNC, VSYNC, and CTL[3:0]. A low level indicates that input data enable and control signals will be latched on the falling edge of IDCK, while a high level (3.3V) indicates that input data enable and control signals will be latched on rising edge of IDCK.
RSVD	13	In	This signal must be tied high (3.3V) for normal operation.
SYNC_CONT	14	In	PLL Synchronization Control. This signal should be tied high (3.3V) when PLL_SYNC is sent over CTL0, see Figure 13.
SUPV	34	In	Input Threshold Voltage Control. A high level (3.3V) indicates that input signal voltage level is 5V and a low level indicates that input signal voltage level is 3.3V. Should match IVCC voltage.
PD	35	In	Power Down (active low). A high level (3.3V) indicates normal operation and a low level indicates power down mode. During power down mode, all data and control inputs are disabled and most internal logic is powered down.

9.2.5 SiI100 Analog Data Pin Description

Pin Name	Pin #	Type	Description
TX0+	24	Analog	Low Voltage Differential Signal output data pairs.
TX0-	23	Analog	
TX1+	27	Analog	
TX1-	26	Analog	
TX2+	30	Analog	
TX2-	29	Analog	
TXC+	21	Analog	Low Voltage Differential Signal output clock pair.
TXC-	20	Analog	
EXT_ SWING	33	Analog	Voltage Swing Adjust. A resistor should tie this pin to AVCC. The amplitude of the voltage swing is determined by this resistance. For remote display applications, 400 Ω is recommended. For laptop computers, 680 Ω is recommended.

9.2.6 SiI100 Power and Ground Pin Description

Pin Name	Pin #	Type	Description
VCC	10	Power	Core VCC. These VCC pins supply power to the core digital logic and must be set to 3.3V.
VCC	32	Power	
VCC	39	Power	
IVCC	53	Power	Input VCC. This VCC pin supplies power for the input pin protection devices. This pin must be set to 5V if input signals are at 5V and can be set to 3.3V if input signals are at 3.3V. SUPV should be set accordingly.
GND	4	Ground	Digital GND.
GND	16	Ground	
GND	45	Ground	
GND	64	Ground	
AVCC	22	Power	Analog VCC, must be set to 3.3V.
AVCC	28	Power	
AGND	19	Ground	Analog GND.
AGND	25	Ground	
AGND	31	Ground	
PVCC	18	Power	PLL Analog VCC, must be set to 3.3V.
PGND	17	Ground	PLL Analog GND.

9.3 SiI100 Pins Listed Numerically

Pin #	Pin Name	Type	Description
1	DE	In	Input Data Enable. This signal qualifies the active data period. DE is always required by the SiI100 and must be high during active display time and low during blank time.
2	HSYNC	In	Horizontal Sync input control signal.
3	VSYNC	In	Vertical Sync input control signal.
4	GND	Ground	Digital GND.
5	CTL0	In	Reserved control signal, which should be connected to PLL_SYNC (pin 36).
6	CTL1	In	General input control signal 1.
7	CTL2	In	General input control signal 2.
8	CTL3	In	General input control signal 3.
9	DEDGE	In	Data Latching Edge. A low level indicates that input data (D[23:0]) will be latched on the falling edge of IDCK while a high level (3.3V) indicates that input data will be latched on the rising edge of IDCK.
10	VCC	Power	Core VCC. This VCC pin supplies power to the core digital logic and must be set to 3.3V.
11	CEDGE	In	Control Latching Edge. Controls latching edge of control signals DE, HSYNC, VSYNC, and CTL[3:0]. A low level indicates that input data enable and control signals will be latched on the falling edge of IDCK, while a high level (3.3V) indicates that input data enable and control signals will be latched on rising edge of IDCK.
12	IDCK	In	Input Data Clock. Input data can be valid either on falling or on rising edge of IDCK as selected by DEDGE pin.
13	RSVD	In	This signal must be tied high (3.3V) for normal operation.
14	SYNC_ CONT	In	PLL Synchronization Control. This signal should be tied high (3.3V) when PLL_SYNC is sent over CTL0, see Figure 13.
15	PLLCK	Out	Internal PLL Clock Output. The operating frequency is 2.5 times that of IDCK. This signal is for test purposes only, and should be left unconnected. To probe this signal output, a 500 Ω pull down resistor must be connected between this pin and ground.
16	GND	Ground	Digital GND.
17	PGND	Ground	PLL Analog GND.
18	PVCC	Power	PLL Analog VCC, must be set to 3.3V.
19	AGND	Ground	Analog GND.
20	TXC-	Analog	Low voltage Differential Signal output clock pair.
21	TXC+	Analog	
22	AVCC	Power	Analog VCC must be set to 3.3V.
23	TX0-	Analog	Low Voltage Differential Signal output data pairs.
24	TX0+	Analog	
25	AGND	Ground	Analog GND.
26	TX1-	Analog	Low Voltage Differential Signal output data pairs.
27	TX1+	Analog	

SiI100 Numerical Pin Description (cont'd)

Pin #	Pin Name	Type	Description
28	AVCC	Power	Analog VCC must be set to 3.3V.
29	TX2-	Analog	Low Voltage Differential Signal output data pairs.
30	TX2+	Analog	
31	AGND	Ground	Analog GND.
32	VCC	Power	Core VCC. This VCC pin supplies power to the core digital logic and must be set to 3.3V.
33	EXT_ SWING	Analog	Voltage Swing Adjust. A resistor should tie this pin to AVCC. The amplitude of the voltage swing is determined by this resistance. For remote display applications, 400 Ω is recommended. For laptop computers, 680 Ω is recommended.
34	SUPV	In	Input Threshold Voltage Control. A high level (3.3V) indicates that input signal voltage level is 5V and a low level indicates that input signal voltage level is 3.3V. Should match IVCC voltage.
35	PD	In	Power Down (active low). A high level (3.3V) indicates normal operation and a low level indicates power down mode. During power down mode, all data and control inputs are disabled and most internal logic is powered down.
36	PLL_ SYNC	Out	PLL Synchronization. Generated every VSYNC to force synchronization of both transmitter and receiver PLL clocks. This pin must be connected to pin 5 (CTL0) to enable the PLL synchronization feature.
37	D23	In	Input Data.
38	D22	In	
39	VCC	Power	Core VCC. This VCC pin supplies power to the core digital logic and must be set to 3.3V.
40	D21	In	Input Data.
41	D20	In	
42	D19	In	
43	D18	In	
44	D17	In	
45	GND	Ground	Digital GND.
46	D16	In	Input Data.
47	D15	In	
48	D14	In	
49	D13	In	
50	D12	In	
51	D11	In	
52	D10	In	
53	IVCC	Power	Input VCC. This VCC pin supplies power for the input pin protection devices. This pin must be set to 5V if input signals are at 5V and can be set to 3.3V if input signals are at 3.3V. SUPV should be set accordingly.
54	D9	In	Input Data.
55	D8	In	
56	D7	In	
57	D6	In	
58	D5	In	
59	D4	In	
60	D3	In	
61	D2	In	
62	D1	In	
63	D0	In	
64	64	Ground	Digital GND.

10. SiI101 Pin Description

10.1 SiI101 Pin Diagram

The SiI101 is available in an 80-pin 12mm x 12mm TQFP package.

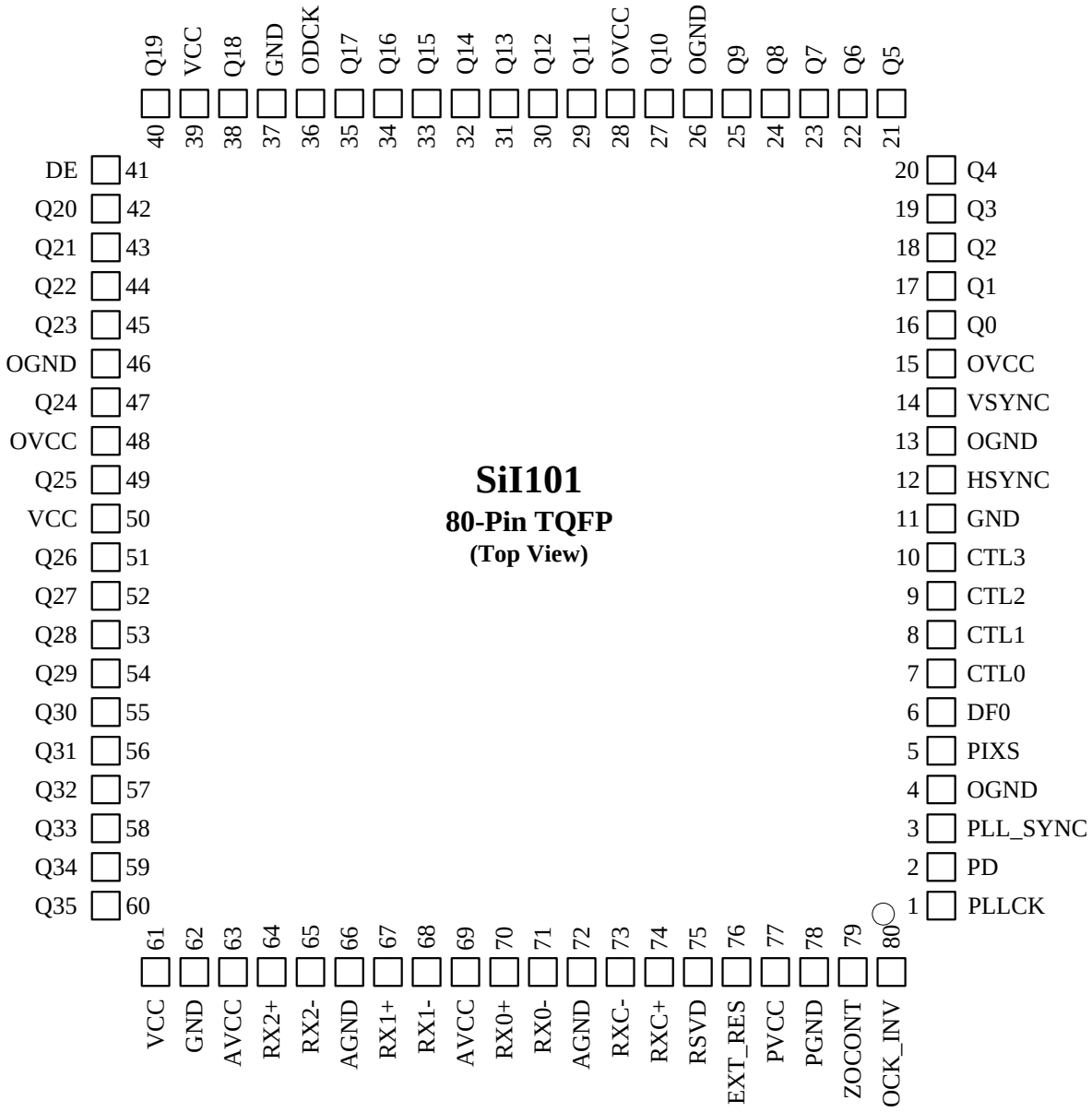

Figure 15. SiI101 Pin Diagram

10.2 SiI101 Pins Grouped by Functionality

10.2.1 SiI101 Data Output Pin Description

Pin Name	Pin #	Type	Description
Q35	60	Out	Output Data [35:0].
Q34	59	Out	Output data is synchronized with output data clock (ODCK).
Q33	58	Out	When PIXS is low Q35-Q24 are low and Q23-Q0 output 24-bit/pixel data.
Q32	57	Out	When PIXS is high Q17-Q0 output the even numbered pixels (pixel 0, 2, 4, ... , etc.)
Q31	56	Out	and Q35-Q18 output the odd numbered pixels (pixel 1, 3, 5, ... , etc.).
Q30	55	Out	
Q29	54	Out	Refer to Signal Mapping Section 6.2 for description of data coordination between
Q28	53	Out	data in for SiI100 and data out for SiI101.
Q27	52	Out	
Q26	51	Out	
Q25	49	Out	
Q24	47	Out	
Q23	45	Out	
Q22	44	Out	
Q21	43	Out	
Q20	42	Out	
Q19	40	Out	
Q18	38	Out	
Q17	35	Out	
Q16	34	Out	
Q15	33	Out	
Q14	32	Out	
Q13	31	Out	
Q12	30	Out	
Q11	29	Out	
Q10	27	Out	
Q9	25	Out	
Q8	24	Out	
Q7	23	Out	
Q6	22	Out	
Q5	21	Out	
Q4	20	Out	
Q3	19	Out	
Q2	18	Out	
Q1	17	Out	
Q0	16	Out	
ODCK	36	Out	Output Data Clock.
DE	41	Out	Output Data Enable.
HSYNC	12	Out	Horizontal Sync output control signal.
VSYNC	14	Out	Vertical Sync output control signal.
CTL0	7	Out	Reserved control signal, which should be connected to PLL_SYNC (pin 3).
CTL1	8	Out	General output control signal 1.
CTL2	9	Out	General output control signal 2.
CTL3	10	Out	General output control signal 3.

10.2.2 SiI101 Test Output Pin Description

Pin Name	Pin #	Type	Description
PLLCK	1	Out	Internal PLL Clock Output. The operating frequency is 2.5 times that of IDCK. This signal is for test purposes only, and should be left unconnected.

10.2.3 SiI101 Synchronization Pin Description

Pin Name	Pin #	Type	Description
PLL_SYNC	3	In	PLL Synchronization. Generated every VSYNC to force synchronization of both transmitter and receiver PLL clocks. This pin must be connected to pin 7 (CTL0) to enable the PLL synchronization feature.

10.2.4 SiI101 Analog Data Pin Description

Pin Name	Pin #	Type	Description
RX0+	70	Analog	Low Voltage Differential Signal input data pairs.
RX0-	71	Analog	
RX1+	67	Analog	
RX1-	68	Analog	
RX2+	64	Analog	
RX2-	65	Analog	
RXC+	74	Analog	Low Voltage Differential Signal input clock pair.
RXC-	73	Analog	
EXT_RES	76	Analog	Impedance Matching Control. Resistor value should be ten times the characteristic impedance of the cable. In the common case of 50Ω transmission line, an external 500 Ω resistor must be connected between AVCC and this pin.

10.2.5 SiI101 Configuration Pin Description

Pin Name	Pin #	Type	Description
PD	2	In	Power Down (active low). A high level (3.3V) indicates normal operation and a low level indicates power down mode. During power down mode, all data and control outputs are brought low and internal circuitry is powered down.
PIXS	5	In	Pixel Select. A low level indicates that output data is one pixel (up to 24-bit) per clock and a high level (3.3V) indicates that output data is two pixels (up to 36-bit) per clock.
DF0	6	In	Output Data Format. This pin controls clock and data output format. A low level indicates that ODCK runs continuously for color TFT panel support and a high level (3.3V) indicates that ODCK is stopped (LOW) for color 24-bit DSTN panel support when DE is low. For more information, see Table 1.
RSVD	75	In	This signal must be tied high (3.3V) for normal operation.
ZOCONT	79	In	Termination Resistor Range Selection. A low level selects the termination resistor range of approximately 50 Ω to 70 Ω. A high level (3.3V) selects the termination resistor range of approximately 40 Ω to 50 Ω. For most applications ZOCONT should be set high (low termination range).
OCK_INV	80	In	ODCK Polarity. A low level selects normal ODCK output. A high level (3.3V) selects inverted ODCK output for color TFT panel support. For color 24-bit DSTN panel support, please refer to Table 1.

10.2.6 SiI101 Power and Ground Pin Description

Pin Name	Pin #	Type	Description
VCC	39	Power	Core VCC. These VCC pins supply power to the core digital logic and must be set to 3.3V.
VCC	50	Power	
VCC	61	Power	
GND	11	Ground	Digital GND.
GND	37	Ground	
GND	62	Ground	
OVCC	15	Power	Output VCC. This OVCC pin supplies power for output buffers and for output pin protection devices. This pin must be set to 5V for 5V digital outputs and set to 3.3V for 3.3V digital outputs.
OVCC	28	Power	
OVCC	48	Power	
OGND	4	Ground	Output GND.
OGND	13	Ground	
OGND	26	Ground	
OGND	46	Ground	
AVCC	63	Power	Analog VCC, must be set to 3.3V.
AVCC	69	Power	
AGND	66	Ground	Analog GND.
AGND	72	Ground	
PVCC	77	Power	PLL Analog VCC, must be set to 3.3V.
PGND	78	Ground	PLL Analog GND.

10.3 SiI101 Pins Listed Numerically

Pin #	Pin Name	Type	Description
1	PLLCK	Out	Internal PLL Clock Output. The operating frequency is 2.5 times that of IDCK. This signal is for test purposes only, and should be left unconnected.
2	PD	In	Power Down (active low). A high level (3.3V) indicates normal operation and a low level indicates power down mode. During power down mode, all data and control outputs are brought low and internal circuitry is powered down.
3	PLL_SYNC	In	PLL Synchronization. Generated every VSYNC to force synchronization of both transmitter and receiver PLL clocks. This pin must be connected to pin 7 (CTL0) to enable the PLL synchronization feature.
4	OGND	Ground	Output GND.
5	PIXS	In	Pixel Select. A low level indicates that output data is one pixel (up to 24-bit) per clock and a high level (3.3V) indicates that output data is two pixels (up to 36-bit) per clock.
6	DF0	In	Output Data Format. This pin controls clock and data output format. A low level indicates that ODCK runs continuously for color TFT panel support and a high level (3.3V) indicates that ODCK is stopped (LOW) for color 24-bit DSTN panel support when DE is low. For more information, see Table 1.
7	CTL0	Out	Reserved control signal, which should be connected to PLL_SYNC (pin 3).
8	CTL1	Out	General output control signal 1.
9	CTL2	Out	General output control signal 2.
10	CTL3	Out	General output control signal 3.
11	GND	Ground	Digital GND.
12	HSYNC	Out	Horizontal Sync output control signal.
13	OGND	Ground	Output GND.
14	VSYNC	Out	Vertical Sync output control signal.
15	OVCC	Power	Output VCC. This OVCC pin supplies power for output buffers and for output pin protection devices. This pin must be set to 5V for 5V digital outputs and set to 3.3V for 3.3V digital outputs.
16	Q0	Out	Output Data.
17	Q1	Out	
18	Q2	Out	
19	Q3	Out	
20	Q4	Out	
21	Q5	Out	
22	Q6	Out	
23	Q7	Out	
24	Q8	Out	
25	Q9	Out	
26	OGND	Ground	Output GND.
27	Q10	Out	Output Data.

SiI101 Numerical Pin Description (cont'd)

Pin #	Pin Name	Type	Description
28	OVCC	Power	Output VCC. This OVCC pin supplies power for output buffers and for output pin protection devices. This pin must be set to 5V for 5V digital outputs and set to 3.3V for 3.3V digital outputs.
29	Q11	Out	Output Data.
30	Q12	Out	
31	Q13	Out	
32	Q14	Out	
33	Q15	Out	
34	Q16	Out	
35	Q17	Out	
36	ODCK	Out	Output Data Clock.
37	GND	Ground	Digital GND.
38	Q18	Out	Output Data.
39	VCC	Power	Core VCC. This VCC pin supplies power to the core digital logic and must be set to 3.3V.
40	Q19	Out	Output Data.
41	DE	Out	Output Data Enable.
42	Q20	Out	Output Data.
43	Q21	Out	
44	Q22	Out	
45	Q23	Out	
46	OGND	Ground	Output GND.
47	Q24	Out	Output Data.
48	OVCC	Power	Output VCC. This OVCC pin supplies power for output buffers and for output pin protection devices. This pin must be set to 5V for 5V digital outputs and set to 3.3V for 3.3V digital outputs.
49	Q25	Out	Output Data.
50	VCC	Power	Core VCC. This VCC pin supplies power to the core digital logic and must be set to 3.3V.

SiI101 Numerical Pin Description (cont'd)

Pin #	Pin Name	Type	Description
51	Q26	Out	Output Data.
52	Q27	Out	
53	Q28	Out	
54	Q29	Out	
55	Q30	Out	
56	Q31	Out	
57	Q32	Out	
58	Q33	Out	
59	Q34	Out	
60	Q35	Out	
61	VCC	Power	Core VCC. This VCC pin supplies power to the core digital logic and must be set to 3.3V.
62	GND	Ground	Digital GND.
63	AVCC	Power	Analog VCC, must be set to 3.3V..
64	RX2+	Analog	Low Voltage Differential Signal input data pairs.
65	RX2-	Analog	
66	AGND	Ground	Analog GND.
67	RX1+	Analog	Low Voltage Differential Signal input data pairs.
68	RX1-	Analog	
69	AVCC	Power	Analog VCC, must be set at 3.3V.
70	RX0+	Analog	Low Voltage Differential Signal input data pairs.
71	RX0-	Analog	
72	AGND	Ground	Analog GND.
73	RXC-	Analog	Low Voltage Differential Signal input clock pair.
74	RXC+	Analog	
75	RSVD	In	This signal must be tied high (3.3V) for normal operation
76	EXT_RES	Analog	Impedance Matching Control. Resistor value should be ten times the characteristic impedance of the cable. In the common case of 50Ω transmission line, an external 500Ω resistor must be connected between AVCC and this pin.
77	PVCC	Power	PLL Analog VCC, must be set to 3.3V.
78	PGND	Ground	PLL Analog GND.
79	ZOCONT	In	Termination Resistor Range Selection. A low level selects the termination resistor range of approximately 50 Ω to 70 Ω. A high level (3.3V) selects the termination resistor range of approximately 40 Ω to 50 Ω. For most applications ZOCONT should be set high (low termination range).
80	OCK_INV	In	ODCK Polarity. A low level selects normal ODCK output. A high level (3.3V) selects inverted ODCK output for color TFT panel support. For color 24-bit DSTN panel support, please refer to Table 1.

11. Electrical Specifications

11.1 Absolute Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage 5V	-0.3		6.0	V
V_{CC}	Supply Voltage 3.3V	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{CC}+ 0.3	V
V_O	Output Voltage	-0.3		V_{CC}+ 0.3	V
T_A	Ambient Temperature (with power applied)	-25		105	°C
T_{STG}	Storage Temperature	-40		125	°C
P_{PD}	Package Power Dissipation			1	W

Table 5. Absolute Conditions

Notes: Permanent device damage may occur if Absolute Maximum Conditions are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Core Supply Voltage applies to VCC, AVCC, PVCC	3.00	3.3	3.6	V
V_{CCIO}	I/O Supply Voltage applies to IVCC, OVCC	3.00	3.3	5.5	V
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

Table 6. Normal Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND - 0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			IVCC + 0.8	V
V_{CONL}	Output Clamp Voltage[1]	I_{CL} = -18mA			GND - 0.8	V
V_{COPL}	Output Clamp Voltage[1]	I_{CL} = 18mA			OVCC + 0.8	V
I_{IL}	Input Leakage Current		-10		10	µA
I_{OZ}	Output Leakage Current	High Impedance	-100		100	µA

Under normal operating conditions unless otherwise specified.

Table 7. DC Digital I/O Specifications (SiI100 and SiI101)

Note:
[1] Guaranteed by design.

11.2 DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak to peak amplitude	R_{LOAD} = 50 Ω R_{EXT_SWING} = 850 Ω R_{EXT_SWING} = 680 Ω R_{EXT_SWING} = 400 Ω	 250 310 580	 300 370 650	 350 430 720	 mV mV mV
V_{DOH}	Differential High-level Output Voltage			AVCC		V
I_{DOS}	Differential Output Short Circuit Current	V_{OUT} = 0 V			5	µA
I_{PD}	Power-down Current				4	mA
I_{CCT}	Transmitter Supply Current	DCLK = 65 MHz R_{EXT_SWING} = 680 Ω IVCC = VCC Typical Pattern[3]		38	50	mA
		DCLK = 65 MHz R_{EXT_SWING} = 680 Ω IVCC = VCC Worse Case Pattern[4]		40	55	mA

Under normal operating conditions unless otherwise specified.

Table 8. SiI100 Transmitter DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OHD}	Output High Drive	V_{OUT} = V_{OH} , Data and Controls, OVCC=3.3V		10		mA
I_{OLD}	Output Low Drive	V_{OUT} = V_{OL} , Data and Controls, OVCC=3.3V		-14		mA
I_{OHC}	Output High Drive	V_{OUT} = V_{OH} , ODCK, OVCC=3.3V		22		mA
I_{OLC}	Output Low Drive	V_{OUT} = V_{OL} , ODCK, OVCC=3.3V		-30		mA
V_{ID}	Differential Input Voltage Single Ended Amplitude		250		1000	mV
I_{PD}	Power-down Current[1]				25	µA
I_{CCR}	Receiver Supply Current Output is one pixel per clock mode.[2]	DCLK = 65 MHz C_{LOAD} = 10pF R_{EXT_SWING} = 680 Ω OVCC = VCC Typical Pattern[3]		110	130	mA
		DCLK = 65 MHz C_{LOAD} = 10pF R_{EXT_SWING} = 680 Ω OVCC = VCC Worse Case Pattern[4]		124	150	mA

Under normal operating conditions unless otherwise specified.

Table 9. SiI101 Receiver DC Specifications

Notes:
1. The transmitter must be in power-down mode, powered off, or disconnected for the current to be under this maximum.
2. For worst case I/O power consumption.
3. The Typical Pattern contains a gray scale area, checkerboard area, and text.
4. Black and white checkerboard pattern, each checker is one pixel wide.

11.3 AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{CIP} /F_{CIP}	IDCK Period/Frequency		40/25		14.7/68	ns/MHz
T_{CIH}	IDCK High Time		4			ns
T_{CIL}	IDCK Low Time		4			ns
T_{IJIT}	Worst Case IDCK Clock Jitter[2,3]				2	ns
T_{SIDF}	Data, DE, VSYNC, HSYNC, and CTL[3:0] Setup Time from IDCK falling edge	CEDGE = 0 DEDGE = 0	1			ns
T_{HIDF}	Data, DE, VSYNC, HSYNC, and CTL[3:0] Hold Time from IDCK falling edge	CEDGE = 0 DEDGE = 0	3			ns
T_{SIDR}	Data, DE, VSYNC, HSYNC, and CTL[3:0] [1] Setup Time from IDCK rising edge	CEDGE = 1 DEDGE = 1	2			ns
T_{HIDR}	Data, DE, VSYNC, HSYNC, and CTL[3:0] [1] Hold Time from IDCK rising edge	CEDGE = 1 DEDGE = 1	3			ns
T_{DDF}	VSYNC, HSYNC, and CTL[3:0] Delay from DE falling edge		T_{CIP}			ns
T_{DDR}	VSYNC, HSYNC, and CTL[3:0] Delay from DE rising edge		T_{CIP}			ns
T_{HDE}	DE high time[1]				$8000T_{CIP}$	ns
T_{LDE}	DE low time		$10T_{CIP}$			ns
S_{LHT}	Small Swing Low-to-High Transition Time	C_{LOAD} = 5pF R_{LOAD} = 50Ω R_{EXT_SWING} = 680Ω	0.25	0.3	0.5	ns
S_{HLT}	Small Swing High-to-Low Transition Time	C_{LOAD} = 5pF R_{LOAD} = 50Ω R_{EXT_SWING} = 680Ω	0.25	0.3	0.5	ns

Under normal operating conditions unless otherwise specified.

Table 10. SiI100 AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew	1 Bit Time			10	%
T_{CCS}	Channel to Channel Differential Input Skew				T_{CIP}	ns
T_{IJIT}	Worst Case Differential Input Clock Jitter tolerance[2,3]				2	ns
D_{LHT}	Low-to-High Transition Time					
	Data and Controls	C_L = 10pF			5.5	ns
	ODCK	C_L = 10pF			2.75	ns
D_{HLT}	High-to-Low Transition Time					
	Data and Controls	C_L = 10pF			3	ns
	ODCK	C_L = 10pF			2	ns
T_{SODF}	Data, DE Setup Time to ODCK falling edge	OCK_INV = 0	3			ns
T_{HODF}	Data, DE Hold Time to ODCK falling edge	OCK_INV = 0	6			ns
T_{SOCR}	VSYNC, HSYNC, and CTL[3:0] Setup Time to ODCK rising edge	OCK_INV = 0	3			ns
T_{HOCR}	VSYNC, HSYNC, and CTL[3:0] Hold Time to ODCK rising edge	OCK_INV = 0	6			ns
T_{SODR}	Data, DE Setup Time to ODCK rising edge[1]	OCK_INV = 1	3			ns
T_{HODR}	Data, DE Hold Time to ODCK rising edge[1]	OCK_INV = 1	6			ns
T_{SOCF}	VSYNC, HSYNC, and CTL[3:0] [1] Setup Time from ODCK falling edge	OCK_INV = 1	3			ns
T_{HOCF}	VSYNC, HSYNC, and CTL[3:0] [1] Hold Time from ODCK falling edge	OCK_INV = 1	6			ns
R_{CIP}	ODCK Cycle Time		14.7		40	ns
R_{CIH}	ODCK High Time[4]		5			ns
R_{CIL}	ODCK Low Time[4]		6			ns
T_{PDL}	Delay from PD Low to high impedance outputs				10	ns

Under normal operating conditions unless otherwise specified.

Table 11. SiI101 AC Specifications

Notes:
1. Guaranteed by design.
2. Jitter is measured by 1) triggering a digital scope at the rising of input clock and 2) measuring the peak to peak time spread of the rising edge of the input clock 1µs after the trigger.
3. Actual jitter tolerance may be higher depending on the frequency of the jitter.
4. Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.

11.4 Timing Diagrams

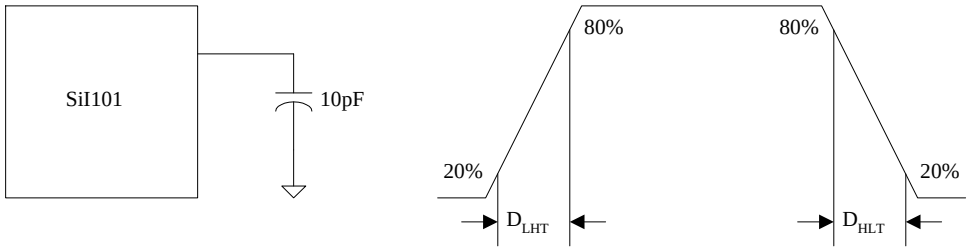

Figure 16. Receiver Digital Output Transition Times

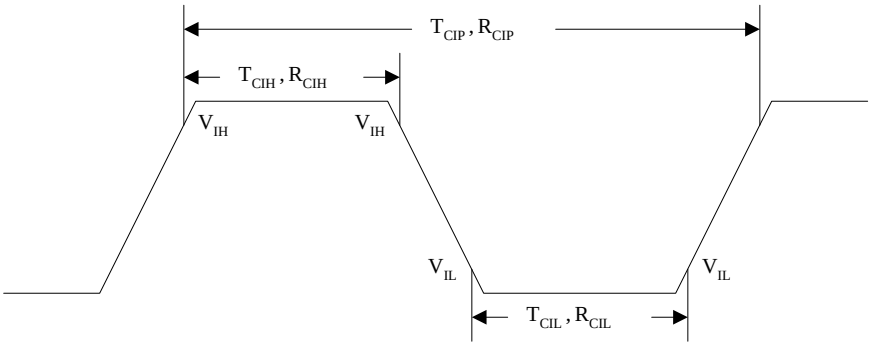

Figure 17. Transmitter/Receiver Clock Cycle/High/Low Times

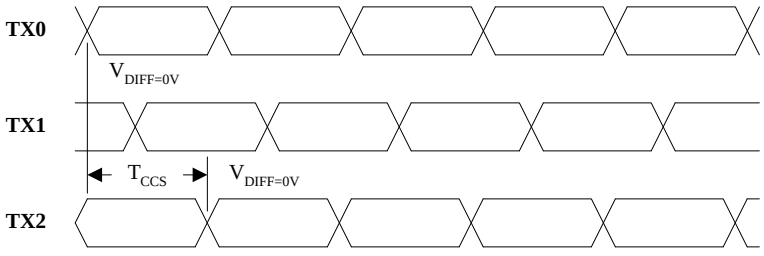

Figure 18. Channel-to-Channel Skew Timing

11.4.1 SiI100 Input Timing

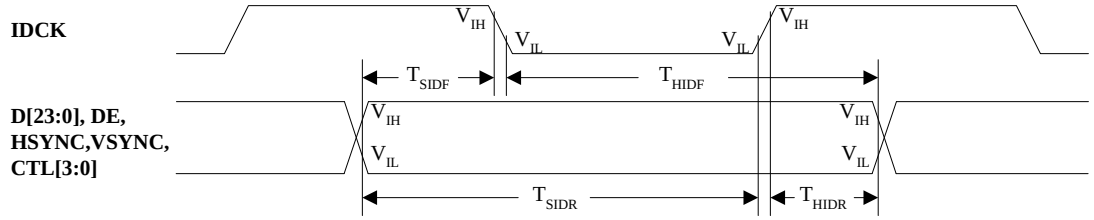

Figure 19. Input Data Setup/Hold Times to IDCK of SiI100

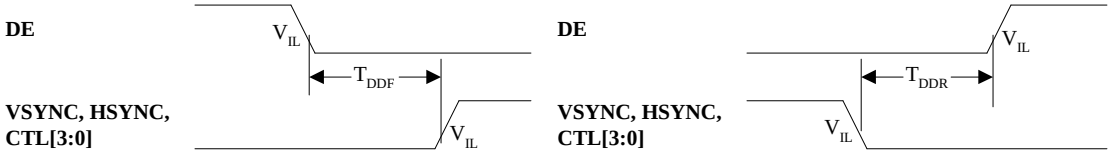

Figure 20. VSYNC, HSYNC, and CTL[3:0] Delay Times from DE of SiI100

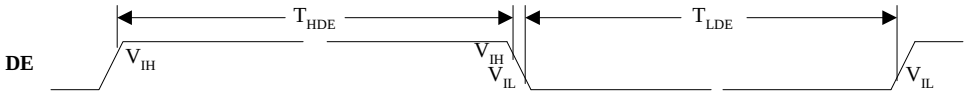

Figure 21. DE High/Low Times of SiI100

11.4.2 SiI101 Output Timing

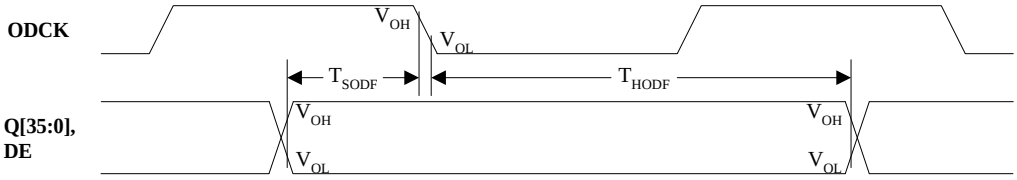

Figure 22. Output Data Setup/Hold Times to ODCK of SiI101

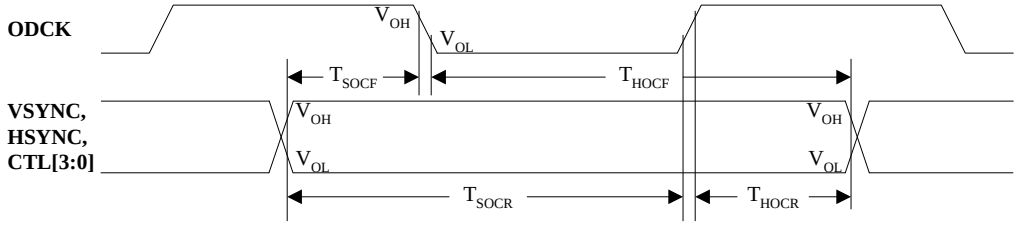

Figure 23. Output Control Setup/Hold Times to ODCK of SiI101

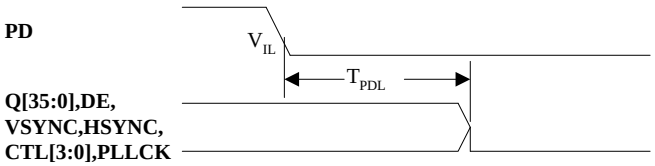

Figure 24. Output Signals Disabled Timing from PD Active of SiI101

12. Package Dimensions

12.1 SiI100 Package Dimensions

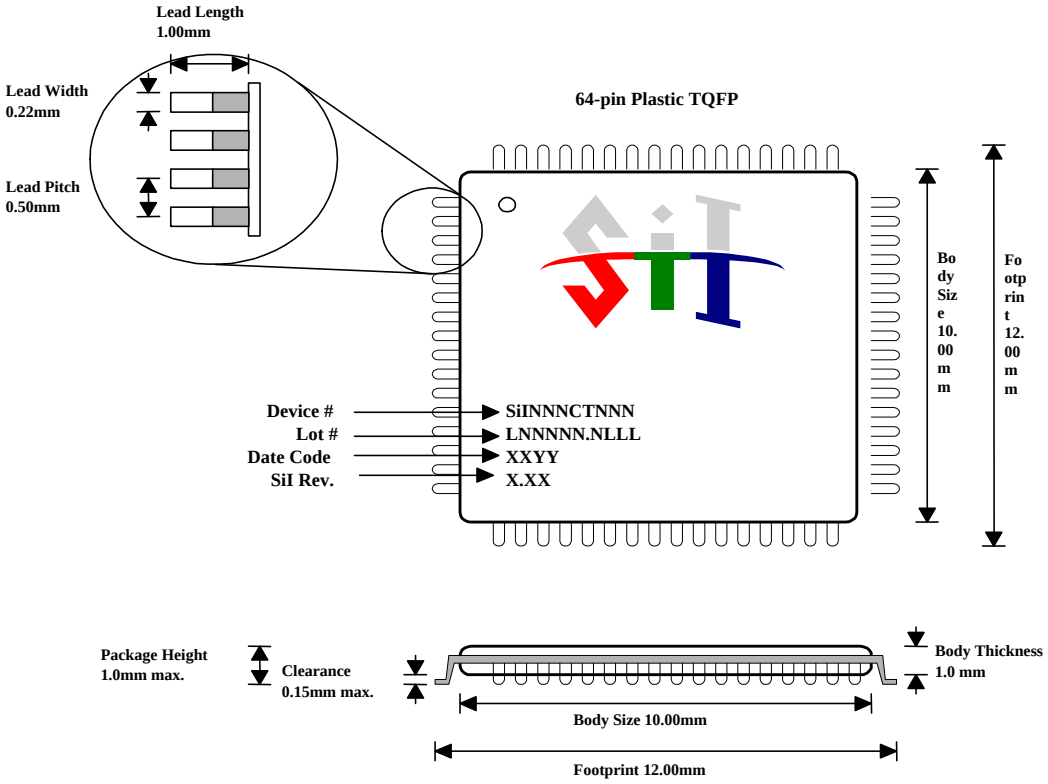

Figure 25. 64 Pin TQFP Package Dimensions

12.2 SiI101 Package Dimensions

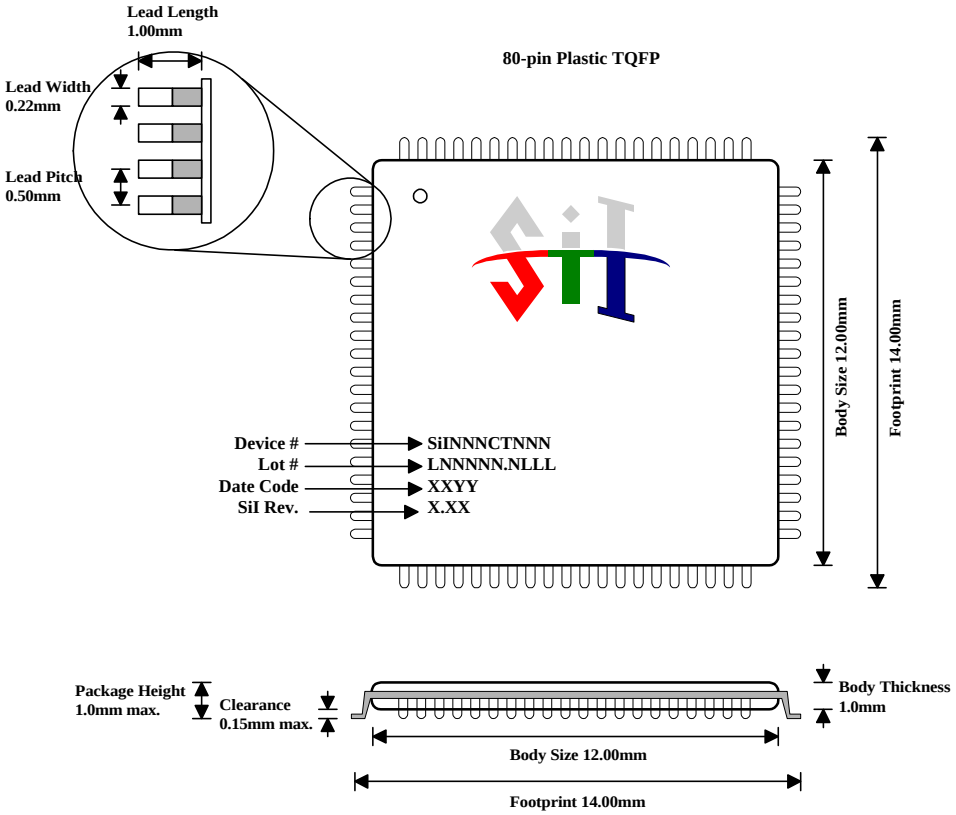

Figure 26. 80 Pin TQFP Package Dimensions

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