# ULTRA COMPACT CMOS VOLTAGE REGULATOR S-817 Series

The S-817 is an ultra compact 3-pin positive voltage regulator developed using CMOS technology. Due to housing into an even more miniaturized SC-82AB package of 2.0 x 2.1 mm, the S-817 offers key advantages for small, portable applications.
The S-817 allows many type of output capacitors including a ceramic type and ensures highly-stable operations at low load of 1μA.

## ■ Features

- Low current consumption
  During operation: Typ. 1.2 μA, Max. 2.5 μA
- Output voltage: 0.1 V steps between 1.1 and 6.0 V
- High accuracy output voltage: ±2.0%
- Output current;
  50 mA capable (3.0 V output product, $V_{IN}$=5 V) Note1
  75 mA capable (5.0 V output product, $V_{IN}$=7 V) Note1
- Dropout voltage
  Typ. 160 mV ($V_{OUT}$ = 5.0 V, $I_{OUT}$ = 10 mA)
- Low ESR capacitor (e.g., a ceramic capacitor of 0.1 μF or more) can be used as the output capacitor.
- Built-in short current limit circuit: Series A only
- Excellent Line Regulation: Stable operation at low load of 1μA
- Ultra compact package: SC-82AB, SOT-23-5

## ■ Applications

- Power source for battery-powered devices
- Power source for personal communication devices
- Power source for home electric/electronic appliances

Note1

Check power dissipation of the package when you use large output current.

## ■ Block Diagram

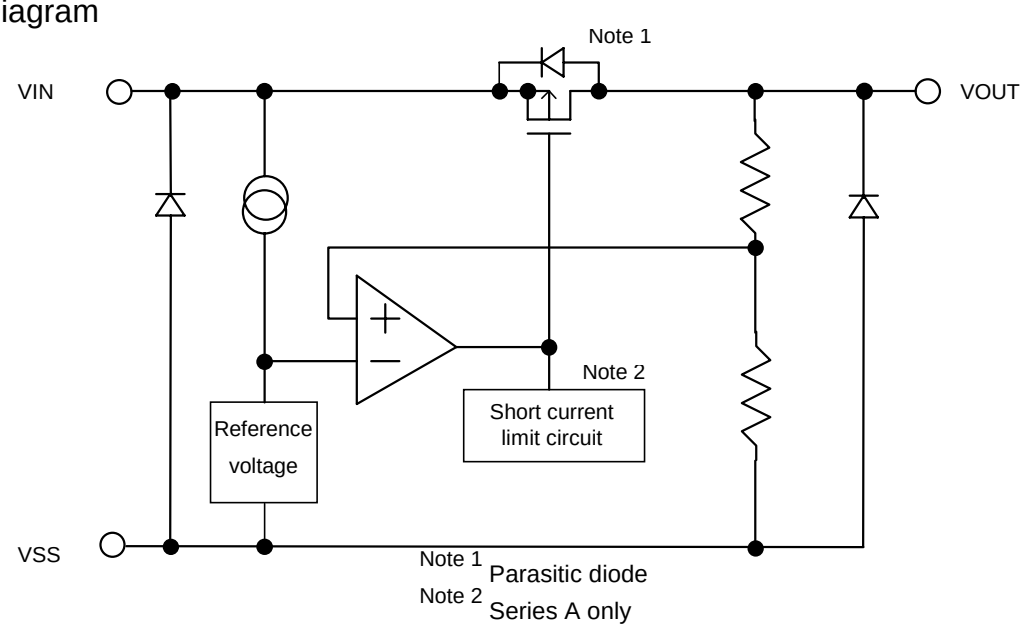



Figure 1 Block Diagram

## ■ Selection Guide

Product Name

S-817x xx Axx - xxx - T2

- IC orientation for taped specifications
- Product symbol
- Package code
  - NB: SC-82AB
  - MC: SOT-23-5
- Output voltage x 10
- Short current limit function: Yes = A, No = B

Table 1 Selection Guide

| Output Voltage | SC-82AB | SOT-23-5 |
|---|---|---|
| 1.5 V ± 2.0% | S-817A15ANB-CUE-T2 | S-817B15AMC-CWE-T2 |
| 2.0 V ± 2.0% | S-817A20ANB-CUJ-T2 | S-817B20AMC-CWJ-T2 |
| 2.5 V ± 2.0% | S-817A25ANB-CUO-T2 | S-817B25AMC-CWO-T2 |
| 3.0 V ± 2.0% | S-817A30ANB-CUT-T2 | S-817B30AMC-CWT-T2 |
| 3.3 V ± 2.0% | S-817A33ANB-CUW-T2 | S-817B33AMC-CWW-T2 |
| 3.5 V ± 2.0% | S-817A35ANB-CUY-T2 | S-817B35AMC-CWY-T2 |
| 4.0 V ± 2.0% | S-817A40ANB-CVD-T2 | S-817B40AMC-CXD-T2 |
| 4.2 V ± 2.0% | S-817A42ANB-CVF-T2 | S-817B42AMC-CXF-T2 |
| 5.0 V ± 2.0% | S-817A50ANB-CVN-T2 | S-817B50AMC-CXN-T2 |

Note:
Contact our sales personnel for products with an output voltage other than those specified above.

## ■ Pin Configuration

For details of package, refer to the attached drawing.

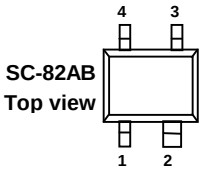



Figure 2 SC-82AB

Table 2 Pin Assignment

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VSS | GND pin |
| 2 | VIN | Input voltage pin |
| 3 | VOUT | Output voltage pin |
| 4 | NC | No connection Note1 |

Note1 Electrically open. So, there is no problem even when connecting pin NC to VIN or VSS.

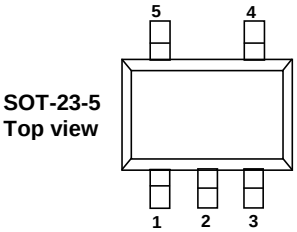



Figure 3 SOT-23-5

Table 3 Pin Assignment

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VSS | GND pin |
| 2 | VIN | Input voltage pin |
| 3 | VOUT | Output voltage pin |
| 4 | NC | No connection Note1 |
| 5 | NC | No connection Note1 |

Note1 Electrically open. So, there is no problem even when connecting pin NC to VIN or VSS.

## ■ Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings (Ta=25°C unless otherwise specified)

| Item | Symbol | Absolute Maximum Rating | Units |
|---|---|---|---|
| Input voltage | $V_{IN}$ | 12 | V |
| Output voltage | $V_{OUT}$ | $V_{SS}$-0.3 to $V_{IN}$+0.3 | V |
| Power dissipation | $P_D$ | 150 (SC-82AB)<br>250(SOT-23-5) | mW |
| Operating temperature range | Topr | -40 to +85 | °C |
| Storage temperature range | Tstg | -40 to +125 | °C |

Note:
This IC has a protection circuit against static electricity. DO NOT apply high static electricity or high voltage that exceeds the performance of the protection circuit to the IC.

## ■ Electrical Characteristics

1. S-817AXXANB

Table 5 Electrical Characteristics (Ta=25°C unless otherwise specified)

| Item | Symbol | Conditions | | Min. | Typ. | Max. | Units | Test circuits |
|---|---|---|---|---|---|---|---|---|
| Output voltage *1) | $V_{OUT}(E)$ | $V_{IN}=V_{OUT}(S)+2V$, $I_{OUT}$=10mA | | $V_{OUT}(S)$ × 0.98 | $V_{OUT}(S)$ | $V_{OUT}(S)$ × 1.02 | V | 1 |
| Output current *2) | $I_{OUT}$ | $V_{OUT}(S)+2V \le V_{IN} \le 10V$ | 1.1V ≤ $V_{OUT}(S)$ ≤ 1.9V | 20 | – | – | mA | 3 |
| | | | 2.0V ≤ $V_{OUT}(S)$ ≤ 2.9V | 35 | – | – | mA | 3 |
| | | | 3.0V ≤ $V_{OUT}(S)$ ≤ 3.9V | 50 | – | – | mA | 3 |
| | | | 4.0V ≤ $V_{OUT}(S)$ ≤ 4.9V | 65 | – | – | mA | 3 |
| | | | 5.0V ≤ $V_{OUT}(S)$ ≤ 6.0V | 75 | – | – | mA | 3 |
| Dropout voltage *3) | Vdrop | $I_{OUT}$ = 10mA | 1.1V ≤ $V_{OUT}(S)$ ≤ 1.4V | – | 0.92 | 1.58 | V | 1 |
| | | | 1.5V ≤ $V_{OUT}(S)$ ≤ 1.9V | – | 0.58 | 0.99 | V | 1 |
| | | | 2.0V ≤ $V_{OUT}(S)$ ≤ 2.4V | – | 0.40 | 0.67 | V | 1 |
| | | | 2.5V ≤ $V_{OUT}(S)$ ≤ 2.9V | – | 0.31 | 0.51 | V | 1 |
| | | | 3.0V ≤ $V_{OUT}(S)$ ≤ 3.4V | – | 0.25 | 0.41 | V | 1 |
| | | | 3.5V ≤ $V_{OUT}(S)$ ≤ 3.9V | – | 0.22 | 0.35 | V | 1 |
| | | | 4.0V ≤ $V_{OUT}(S)$ ≤ 4.4V | – | 0.19 | 0.30 | V | 1 |
| | | | 4.5V ≤ $V_{OUT}(S)$ ≤ 4.9V | – | 0.18 | 0.27 | V | 1 |
| | | | 5.0V ≤ $V_{OUT}(S)$ ≤ 5.4V | – | 0.16 | 0.25 | V | 1 |
| | | | 5.5V ≤ $V_{OUT}(S)$ ≤ 6.0V | – | 0.15 | 0.23 | V | 1 |
| Line regulation 1 | $\Delta V_{OUT}1$ | $V_{OUT}(S)$ + 1 V ≤ $V_{IN}$ ≤ 10 V, $I_{OUT}$ = 1mA | | – | 5 | 20 | mV | 1 |
| Line regulation 2 | $\Delta V_{OUT}2$ | $V_{OUT}(S)$ + 1 V ≤ $V_{IN}$ ≤ 10 V, $I_{OUT}$ = 1µA | | – | 5 | 20 | mV | 1 |
| Load regulation | $\Delta V_{OUT}3$ | $V_{IN}$= $V_{OUT}(S)$+ 2 V | 1.1V ≤ $V_{OUT}(S)$ ≤ 1.9V, 1µA ≤ $I_{OUT}$ ≤ 10mA | – | 5 | 20 | mV | 1 |
| | | | 2.0V ≤ $V_{OUT}(S)$ ≤ 2.9V, 1µA ≤ $I_{OUT}$ ≤ 20mA | – | 10 | 30 | mV | 1 |
| | | | 3.0V ≤ $V_{OUT}(S)$ ≤ 3.9V, 1µA ≤ $I_{OUT}$ ≤ 30mA | – | 20 | 45 | mV | 1 |
| | | | 4.0V ≤ $V_{OUT}(S)$ ≤ 4.9V, 1µA ≤ $I_{OUT}$ ≤ 40mA | – | 25 | 65 | mV | 1 |
| | | | 5.0V ≤ $V_{OUT}(S)$ ≤ 6.0V, 1µA ≤ $I_{OUT}$ ≤ 50mA | – | 35 | 80 | mV | 1 |
| Output voltage temperature coefficient *4) | $\frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}$ | $V_{IN}$ = $V_{OUT}(S)$ + 1 V, $I_{OUT}$ = 10mA -40°C ≤ Ta ≤ 85°C | | | ±100 | – | ppm /°C | 1 |
| Current consumption | $I_{SS}$ | $V_{IN}$ = $V_{OUT}(S)$ + 2 V, no load | | – | 1.2 | 2.5 | µA | 2 |
| Input voltage | $V_{IN}$ | | | – | – | 10 | V | 1 |
| Short current limit | $I_{OS}$ | $V_{IN}$ = $V_{OUT}(S)$ + 2 V, $V_{OUT}$ pin = 0 V | | – | 40 | – | mA | 3 |

*1) $V_{OUT}(S)$=Specified output voltage
$V_{OUT}(E)$=Effective output voltage, i.e., the output voltage when fixing $I_{OUT}$(=10 mA) and inputting $V_{OUT}(S)$+2.0 V.

*2) Output amperage when output voltage goes below 95% of $V_{OUT}(E)$ after gradually increasing output current.

*3) Vdrop = $V_{IN}1$-($V_{OUT}(E)$ × 0.98)
$V_{IN}1$ = Input voltage when output voltage falls 98% of $V_{OUT}(E)$ after gradually decreasing input voltage.

*4) A change in temperatures [mV/°C] is calculated using the following equation.

$$\frac{\Delta V_{OUT}}{\Delta Ta}[mV/°C] = V_{OUT}(S)[V] \times \frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}[ppm/°C] \div 1000$$

Change in temperature of output voltage
Specified output voltage
Output voltage temperature coefficient

2. S-817BXXAMC

Table 6 Electrical Characteristics (Ta=25°C unless otherwise specified)

| Item | Symbol | Conditions | | Min. | Typ. | Max. | Units | Test circuits |
|---|---|---|---|---|---|---|---|---|
| Output voltage *1) | $V_{OUT}(E)$ | $V_{IN}=V_{OUT}(S)+2V$, $I_{OUT}=10mA$ | | $V_{OUT}(S)\times 0.98$ | $V_{OUT}(S)$ | $V_{OUT}(S)\times 1.02$ | V | 1 |
| Output current *2) | $I_{OUT}$ | $V_{OUT}(S)+2V \le V_{IN} \le 10V$ | $1.1V \le V_{OUT}(S) \le 1.9V$ | 20 | – | – | mA | 3 |
| | | | $2.0V \le V_{OUT}(S) \le 2.9V$ | 35 | – | – | mA | 3 |
| | | | $3.0V \le V_{OUT}(S) \le 3.9V$ | 50 | – | – | mA | 3 |
| | | | $4.0V \le V_{OUT}(S) \le 4.9V$ | 65 | – | – | mA | 3 |
| | | | $5.0V \le V_{OUT}(S) \le 6.0V$ | 75 | – | – | mA | 3 |
| Dropout voltage *3) | Vdrop | $I_{OUT}$ = 10mA | $1.1V \le V_{OUT}(S) \le 1.4V$ | – | 0.92 | 1.58 | V | 1 |
| | | | $1.5V \le V_{OUT}(S) \le 1.9V$ | – | 0.58 | 0.99 | V | 1 |
| | | | $2.0V \le V_{OUT}(S) \le 2.4V$ | – | 0.40 | 0.67 | V | 1 |
| | | | $2.5V \le V_{OUT}(S) \le 2.9V$ | – | 0.31 | 0.51 | V | 1 |
| | | | $3.0V \le V_{OUT}(S) \le 3.4V$ | – | 0.25 | 0.41 | V | 1 |
| | | | $3.5V \le V_{OUT}(S) \le 3.9V$ | – | 0.22 | 0.35 | V | 1 |
| | | | $4.0V \le V_{OUT}(S) \le 4.4V$ | – | 0.19 | 0.30 | V | 1 |
| | | | $4.5V \le V_{OUT}(S) \le 4.9V$ | – | 0.18 | 0.27 | V | 1 |
| | | | $5.0V \le V_{OUT}(S) \le 5.4V$ | – | 0.16 | 0.25 | V | 1 |
| | | | $5.5V \le V_{OUT}(S) \le 6.0V$ | – | 0.15 | 0.23 | V | 1 |
| Line regulation 1 | $\Delta V_{OUT}1$ | $V_{OUT}(S)+1V \le V_{IN} \le 10V$, $I_{OUT}=1mA$ | | – | 5 | 20 | mV | 1 |
| Line regulation 2 | $\Delta V_{OUT}2$ | $V_{OUT}(S)+1V \le V_{IN} \le 10V$, $I_{OUT}=1\mu A$ | | – | 5 | 20 | mV | 1 |
| Load regulation | $\Delta V_{OUT}3$ | $V_{IN}=V_{OUT}(S)+2V$ | $1.1V \le V_{OUT}(S) \le 1.9V$, $1\mu A \le I_{OUT} \le 10mA$ | – | 5 | 20 | mV | 1 |
| | | | $2.0V \le V_{OUT}(S) \le 2.9V$, $1\mu A \le I_{OUT} \le 20mA$ | – | 10 | 30 | mV | 1 |
| | | | $3.0V \le V_{OUT}(S) \le 3.9V$, $1\mu A \le I_{OUT} \le 30mA$ | – | 20 | 45 | mV | 1 |
| | | | $4.0V \le V_{OUT}(S) \le 4.9V$, $1\mu A \le I_{OUT} \le 40mA$ | – | 25 | 65 | mV | 1 |
| | | | $5.0V \le V_{OUT}(S) \le 6.0V$, $1\mu A \le I_{OUT} \le 50mA$ | – | 35 | 80 | mV | 1 |
| Output voltage temperature coefficient *4) | $\frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}$ | $V_{IN}=V_{OUT}(S)+1V$, $I_{OUT}=10mA$, $-40°C \le Ta \le 85°C$ | | | ±100 | – | ppm /°C | 1 |
| Current consumption | $I_{SS}$ | $V_{IN}=V_{OUT}(S)+2V$, no load | | – | 1.2 | 2.5 | μA | 2 |
| Input voltage | $V_{IN}$ | | | – | – | 10 | V | 1 |

*1) $V_{OUT}(S)$=Specified output voltage
$V_{OUT}(E)$=Effective output voltage, i.e., the output voltage when fixing $I_{OUT}$(=10 mA) and inputting $V_{OUT}(S)$+2.0 V.

*2) Output amperage when output voltage goes below 95% of $V_{OUT}(E)$ after gradually increasing output current.

*3) Vdrop = $V_{IN}1-(V_{OUT}(E)\times 0.98)$
$V_{IN}1$ = Input voltage when output voltage falls 98% of $V_{OUT}(E)$ after gradually decreasing input voltage.

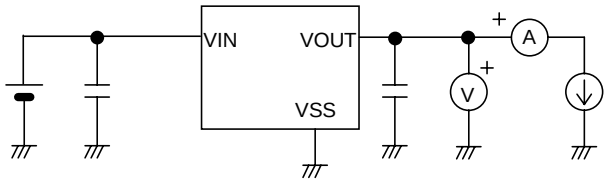
*4) A change in temperatures [mV/°C] is calculated using the following equation.

$$\frac{\Delta V_{OUT}}{\Delta Ta}[mV/°C] = V_{OUT}(S)[V] \times \frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}[ppm/°C] \div 1000$$

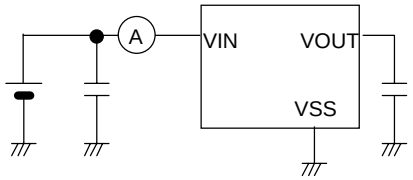
Change in temperature of output voltage
Specified output voltage
Output voltage temperature coefficient

## ■ Test Circuits

1.




2.




3.

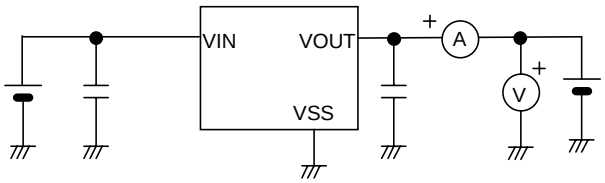
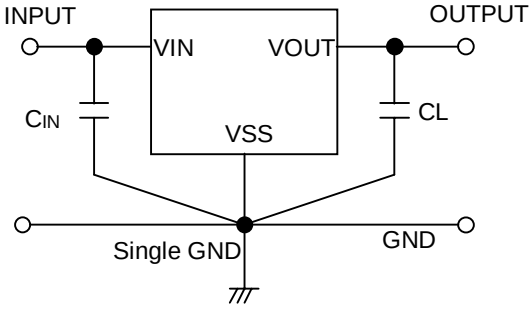



Figure 4 Test Circuits

## ■ Standard Circuit




In addition to a tantalum capacitor, a ceramic capacitor of 0.1 μF or more can be used in CL.
$C_{IN}$ is a capacitor used to stabilize input.

Figure 5 Standard Circuit

## ■ Technical Terms

1. Low ESR
   ESR is the abbreviation for Equivalent Series Resistance.
   Low ESR output capacitors (CL) can be used in the S-817 Series.

2. Output voltage ($V_{OUT}$)
   The accuracy of the output voltage is ensured at ± 2.0% under the specified conditions of input voltage, output current, and temperature, which differ depending upon the product items.

   Note:
   If you change the above conditions, the output voltage value may vary out of the accuracy range of the output voltage. See the electrical characteristics and characteristics data for details.

3. Line regulations 1 and 2 ($\Delta V_{OUT}1$, $\Delta V_{OUT}2$)
   Indicate the input voltage dependencies of output voltage. That is, the values show how much the output voltage changes due to a change in the input voltage with the output current remained unchanged.

4. Load regulation ($\Delta V_{OUT}3$)
   Indicates the output current dependencies of output voltage. That is, the values show how much the output voltage changes due to a change in the output current with the input voltage remained unchanged.

5. Dropout voltage (Vdrop)
   Indicates a difference between input voltage ($V_{IN}1$) and output voltage when output voltage falls by 98 % of $V_{OUT}$ (E) by gradually decreasing the input voltage ($V_{IN}$).
   Vdrop = $V_{IN}1$-[$V_{OUT}$(E) × 0.98]

6. Temperature coefficient of output voltage [$\Delta V_{OUT}/(\Delta Ta \bullet V_{OUT})$]
   The shadowed area in Figure 6 is the range where $V_{OUT}$ varies in the operating temperature range when the temperature coefficient of the output voltage is ±100 ppm/°C.

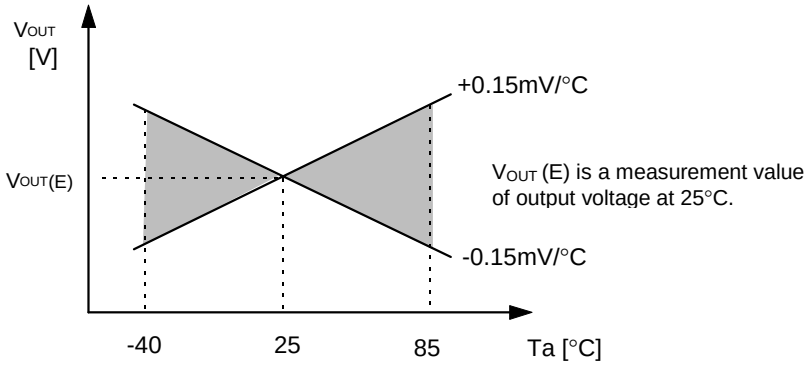



Figure 6 Typical Example of the S-817A15A

A change in temperatures of output voltage [mV/°C] is calculated using the following equation.

$$\frac{\Delta V_{OUT}}{\Delta Ta}\text{[mV/°C]} = V_{OUT}(S)\text{[V]} \times \frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}\text{[ppm/°C]} \div 1000$$

Change in temperatures of output voltage

Specified output voltage

Output voltage temperature coefficient

## ■ Operation

1. Basic Operation

   Figure 7 shows the block diagram of the S-817 Series.

   The error amplifier compares a reference voltage $V_{ref}$ with part of the output voltage divided by the feedback resistors Rs and Rf. It supplies the output transistor with the gate voltage, necessary to ensure certain output voltage free of any fluctuations of input voltage and temperature.

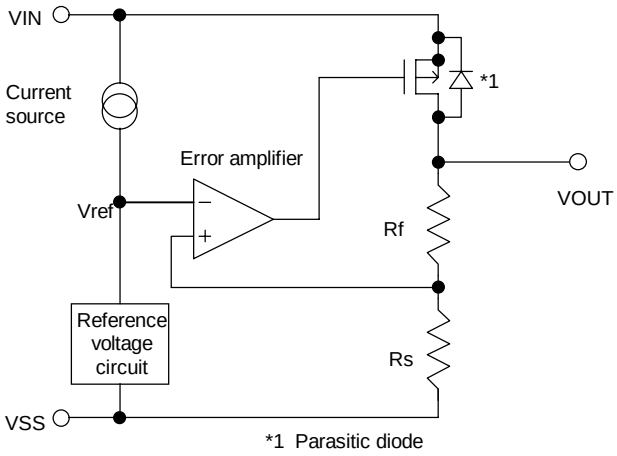



Figure 7 Typical Circuit Block Diagram

2. Output Transistor

   The S-817 Series uses a Pch MOS transistor as the output transistor.

   Be sure that $V_{OUT}$ does not exceed $V_{IN}$+0.3 V to prevent the voltage regulator from being broken due to inverse current flowing when the voltage at $V_{OUT}$ pin goes higher than that at $V_{IN}$ pin because the parasitic diode is connected between pins $V_{IN}$ and $V_{OUT}$.

3. Short Current Limit Circuit

   The S-817A Series incorporates a short current limit circuit to protect the output transistor against shortcircuiting between pins VOUT and VSS. The short current limit circuit controls output current as shown in (1) OUTPUT VOLTAGE versus OUTPUT CURRENT curve, and prevents output current of approx. 40 mA or more from flowing even if VOUT and VSS pins are shorted.

   However, the short current limit circuit does not protect thermal shutdown.

   Be sure that input voltage and load current do not exceed the specified power dissipation level.

   When output current is large and a difference between input and output voltages is large even if not shorted, the short current limit circuit may start functioning and the output current may be controlled to the specified amperage.

   For details, refer to (3) MAXIMUM OUTPUT CURRENT versus INPUT VOLTAGE curve (page 14).

   S-817B Series are removed a short current limit circuit from S-817A Series to flow big current.

## ■ Selection of Output Capacitor (CL)

To stabilize operation against any fluctuation in output load, a capacitor (CL) must be mounted between pins VOUT and VSS in the S-817 Series because the phase is compensated with the help of the internal phase compensating circuit and ESR of the output capacitor.

When selecting a ceramic or an OS capacitor:

Capacitance of 0.1 μF or more

When selecting a tantalum or an aluminum electrolytic capacitor.

Capacitance of 0.1 μF or more and ESR of 30 Ω or less

Pay special attention not to cause an oscillation due to an increase in ESR at low temperatures, when you select an aluminum electrolytic capacitor. Check the capacitor for its performance including temperature characteristics before use.

Overshoot and undershoot characteristics differ depending upon the type of the output capacitor you select. Refer to CL dependencies in “TRANSIENT RESPONSE CHARACTERISTICS” (pages 17 through 22).

## ■Applied Circuits

1. Output Current Boosting Circuit

As shown in Figure 8, the output current can be boosted by externally attaching a PNP transistor. The base current of the PNP transistor is controlled so that output voltage VOUT goes the voltage specified in the S-817 when base-emitter voltage VBE necessary to turn on the PNP transistor is obtained between input voltage VIN and S-817 power source pin VIN.

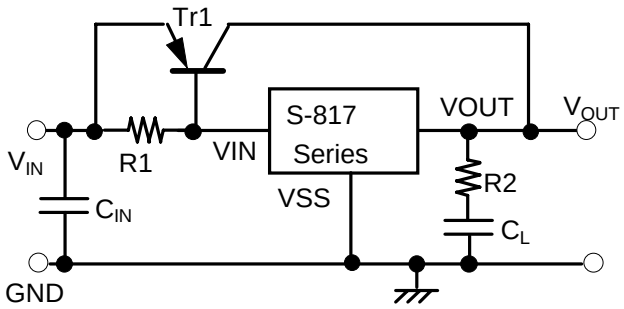



Figure 8 Output Current Boosting Circuit

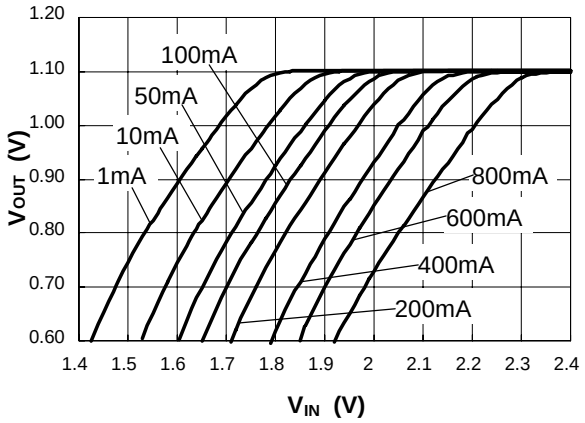
The following are tips and hints for selecting and ensuring optimum use of external parts:

- PNP transistor Tr1:
  1. Set $h_{FE}$ to approx. 100 to 400.
  2. Confirm that no problem occurs due to power dissipation under normal operation conditions.
- Resistor R1:
  Generally set R1 to 1 kΩ ÷ VOUT (S) (the voltage specified in the S-817 Series) or more.
  Output capacitor CL:
  Output capacitor CL is effective in minimizing output fluctuation at powering on or due to power or load fluctuation, but oscillation might occur. Always connect resistor R2 in series to output capacitor CL.
- Resistor R2: Set R2 to 2 Ω x VOUT(S) or more.
- DO NOT attach a capacitor between the S-817 power source VIN and GND pins or between base and emitter of the PNP transistor to avoid oscillation.
- To improve transient response characteristics of the output current boosting circuit shown in Figure 8, check that no problem occurs due to output fluctuation at powering on or due to power or load fluctuation under normal operating conditions.
- Pay attention to the short current limit circuit incorporated into the S-817 Series because it does not function as a shortcircuiting protection circuit for this boosting circuit.

The following graphs show the examples of input-output voltage characteristics (Ta = 25°C, typ.) in the output current boosting circuit:

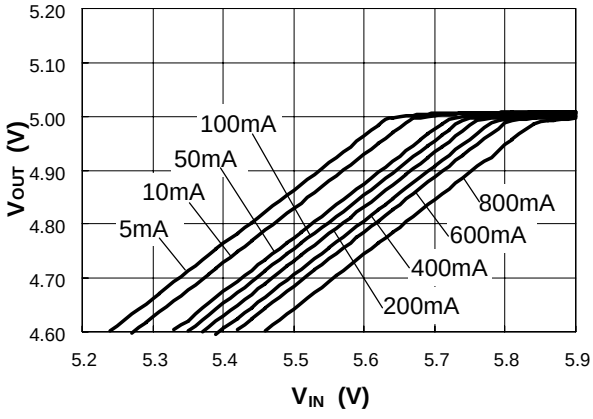
(1) S-817A11ANB/S-817B11AMC

Tr1: 2SA1213Y, R1: 1kΩ, CL: 10µF, R2: 2Ω




(2) S-817A50ANB/S-817B50AMC

Tr1: 2SA1213Y, R1: 200Ω, CL: 10µF, R2: 10Ω



2. Constant Current Circuit

The S-817 Series can be configured as a constant current circuit. See Figure 9. Constant amperage IO is calculated using the following equation

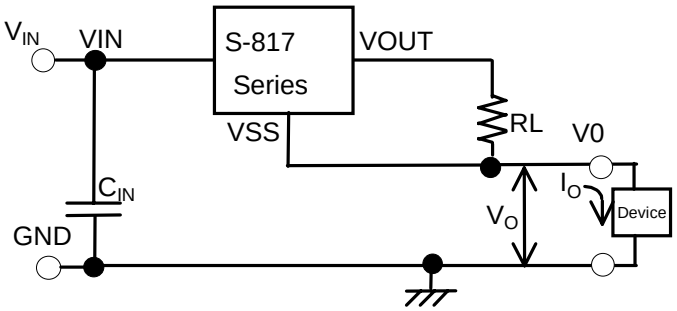
(VOUT (E): Effective output voltage):

IO = (VOUT (E) ÷ RL) +ISS.

Please note that it is impossible to set constant amperage IO in case of circuit (1) of Figure 9 to the value exceeding the drive ability of the S-817.

However, circuit (2) of Figure 9 is an example to set constant amperage to the value exceeding the drive ability of the S-817. Circuit (2) incorporates a current boosting circuit. The maximum input voltage of the constant current circuit is the value obtained by adding 10 V to voltage VO of the device. It is not recommended to attach a capacitor between the S-817 power source VIN and VSS pins or between output VOUT and VSS pins because rush current flows at powering on. An example of input voltage between VIN and VO in circuit (2) vs. IO current characteristics (Ta = 25 °C, typ.) is illustrated in Figure 10.

(1) Constant Current Circuit




(2) Constant Current Boosting Circuit

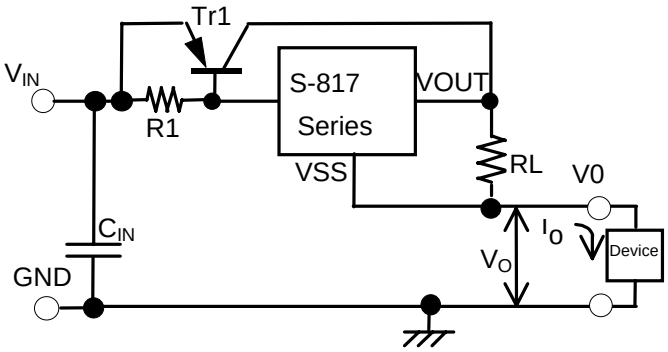



Figure 9 Constant Current Circuit

S-817A11ANB, S-817B11AMC;
VIN-VO pins, Input voltage-IO current

Tr: 2SK1213Y, R1: 1kΩ,VO=2V

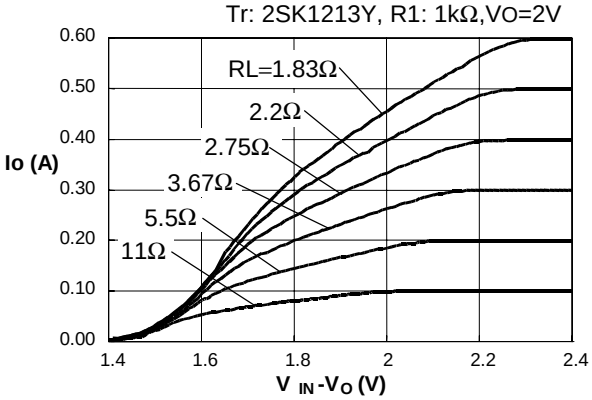



Figure 10 Input Voltage vs Current Characteristics

3. Output Voltage Adjustment Circuit

The output voltage can be boosted by using the configuration shown in Figure 11. The output Voltage VO can be calculated using the following equation (VOUT (E):Effective output voltage):

VO = VOUT (E) x (R1 + R2) ÷ R1 + R2 x ISS

Set R1 and R2 to high values of resistance so as not to be affected by current consumption ISS.

Capacitor C1 is effective in minimizing output fluctuation at powering on or due to power or load fluctuation. Determine the optimum value on your actual device.

It is not also recommended to attach a capacitor between the S-817 power source VIN and VSS pins or between output VOUT and VSS pins because output fluctuation or oscillation at powering on might occur.

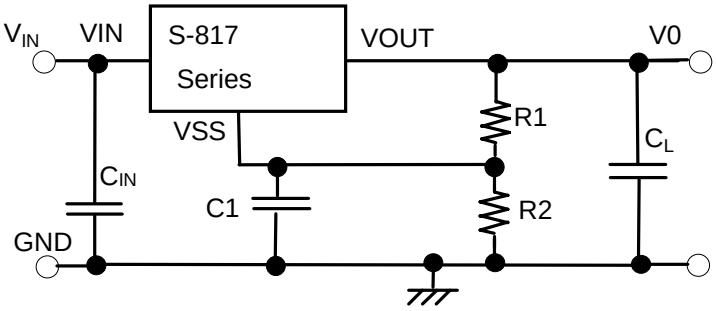



Figure 11 Voltage Adjustment Circuit

## ■ Design Considerations

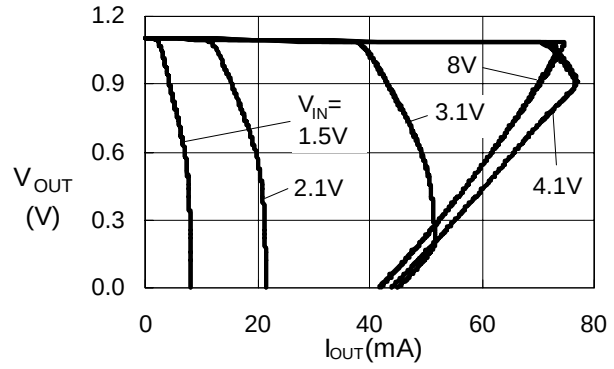
- Design wiring patterns for VIN, VOUT and GND pins to decrease impedance.
  When mounting the output capacitor, connect pins VOUT and VSS as close as possible.
- Note that output voltage may be increased at low load current of less than 1 μA.
- To prevent oscillation, it is recommended to use the external parts under the following conditions.
  * Output capacitor (CL): 0.1 μF or more
  * Equivalent Series Resistance (ESR): 30 Ω or less
  * Input series resistance ($R_{IN}$): 10 Ω or less
- The voltage regulator may oscillate when power source impedance is high and input capacitor is low or not connected.
- Be sure that input voltage and load current do not exceed the power dissipation level of the package.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

Be sure that input voltage and load current do not exceed the power dissipation level of the package.

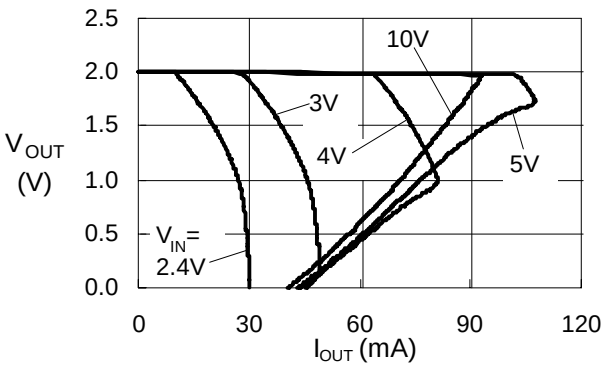
## ■ Typical Operating Chracteristics

(1) OUTPUT VOLTAGE versus OUTPUT CURRENT (When load current increases)

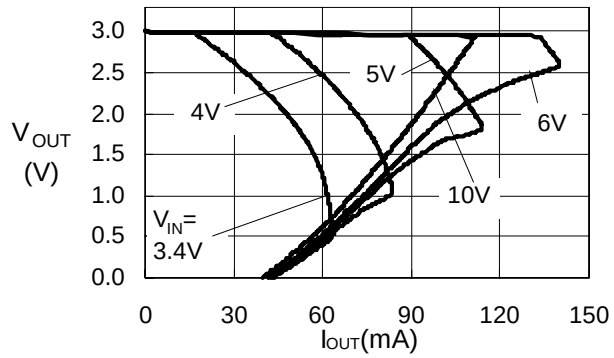
S-817A11A(Ta=25°C)



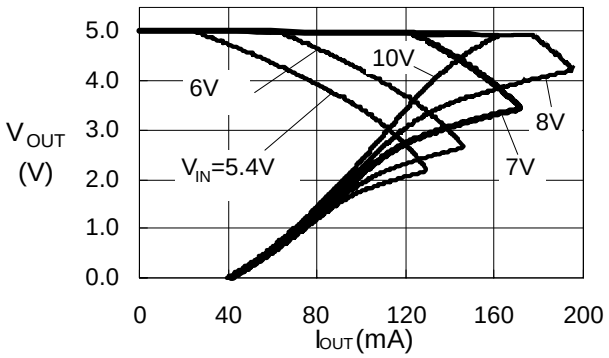

S-817A20A(Ta=25°C)



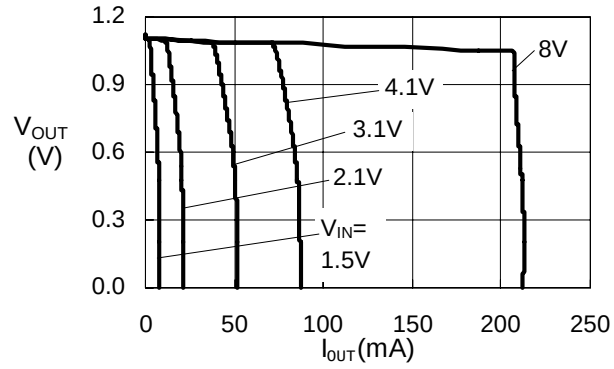

S-817A30A(Ta=25°C)



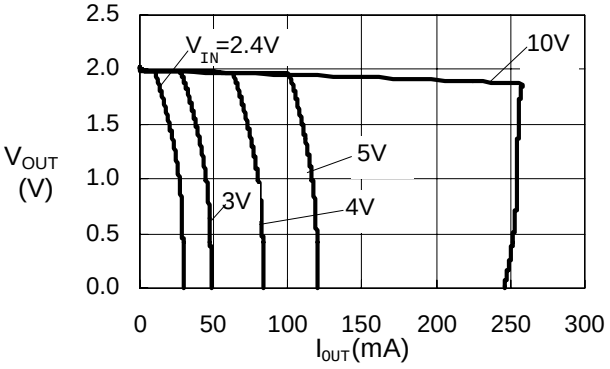

S-817A50A(Ta=25°C)



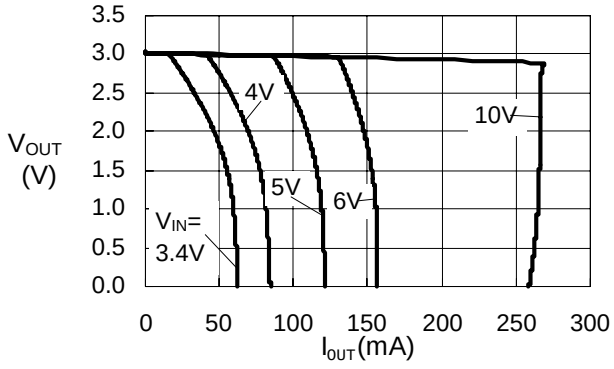

S-817B11A(Ta=25°C)



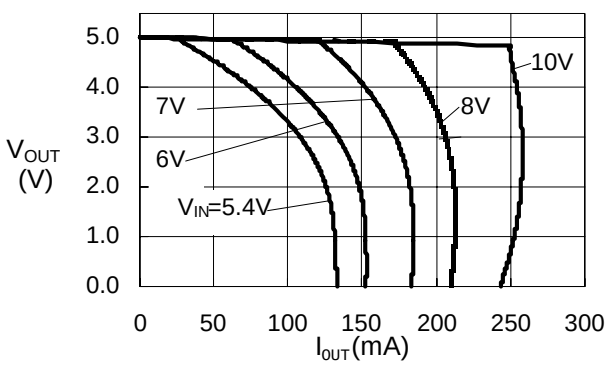

S-817B20A(Ta=25°C)




S-817B30A(Ta=25°C)

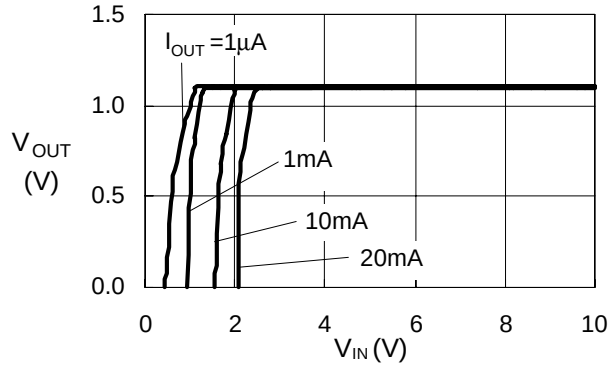



S-817B50A(Ta=25°C)

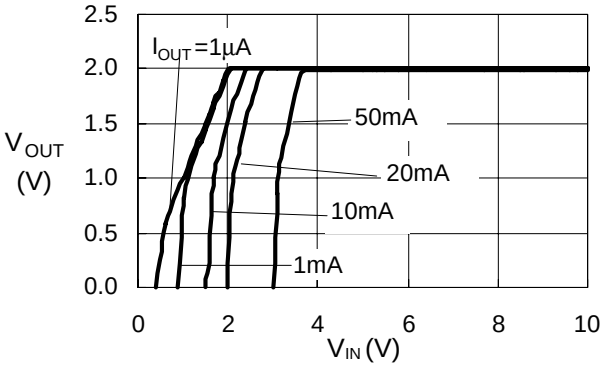


(2) OUTPUT VOLTAGE versus INPUT VOLTAGE

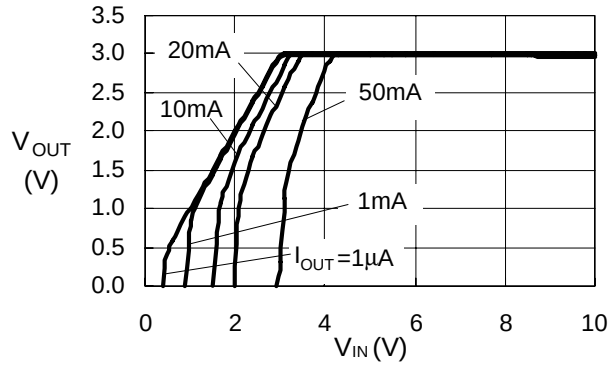
S-817A11A/S-817B11A(Ta=25°C)



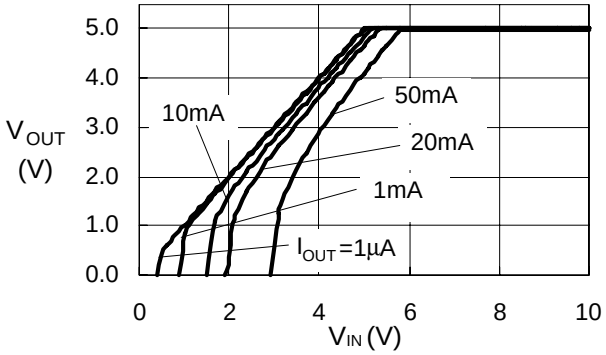

S-817A20A/S-817B20A(Ta=25°C)




S-817A30A/S-817B30A(Ta=25°C)



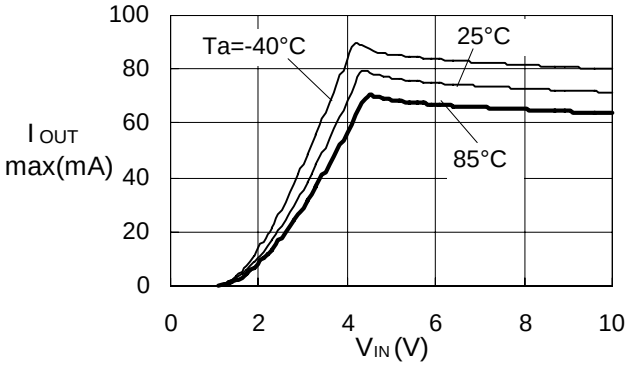

S-817A50A/S-817B50A(Ta=25°C)



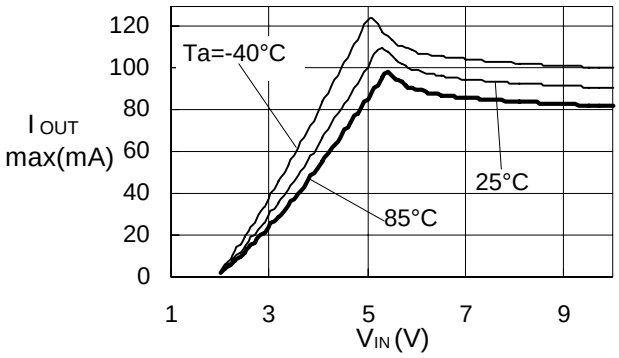
Be sure that input voltage and load current do not exceed the power dissipation level of the package.

(3) MAXIMUM OUTPUT CURRENT versus INPUT VOLTAGE

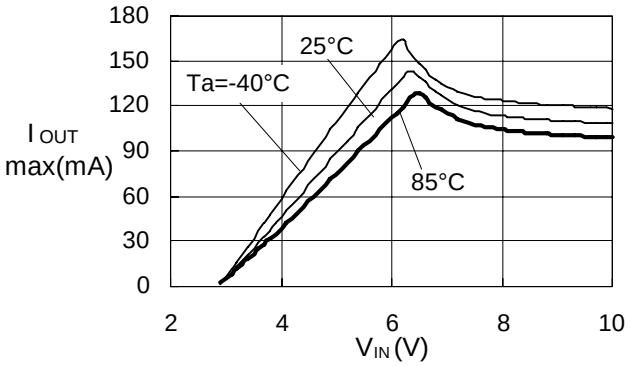
S-817A11A



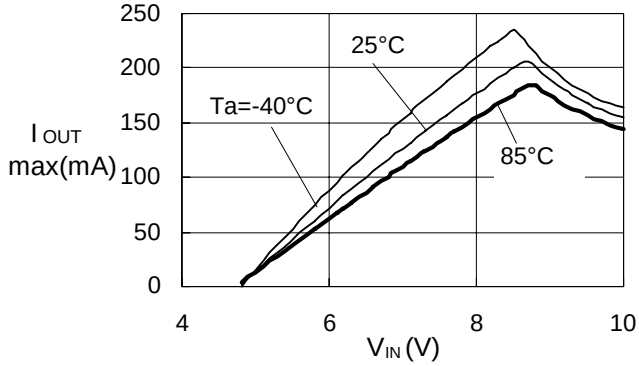

S-817A20A



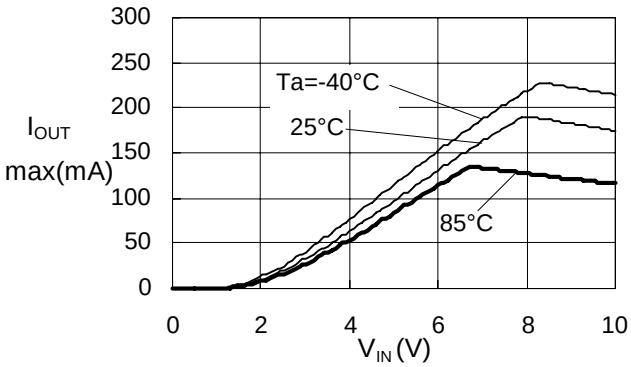

S-817A30A



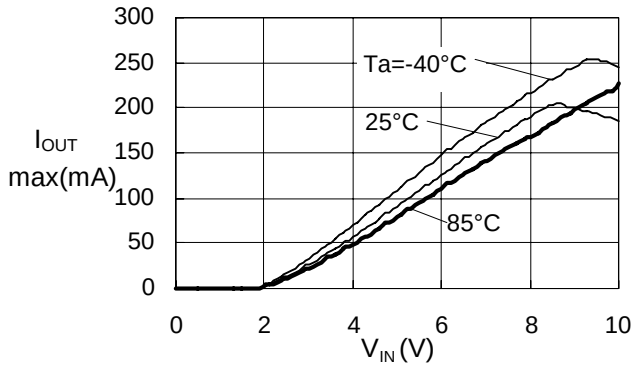

S-817A50A



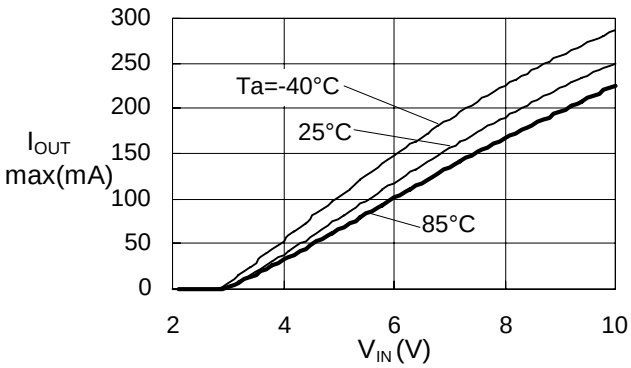

S-817B11A



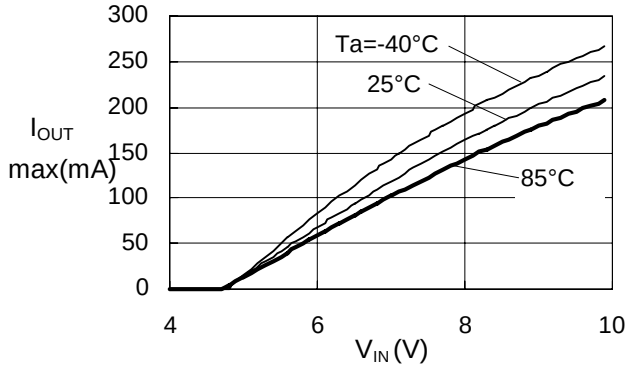

S-817B20A




S-817B30A

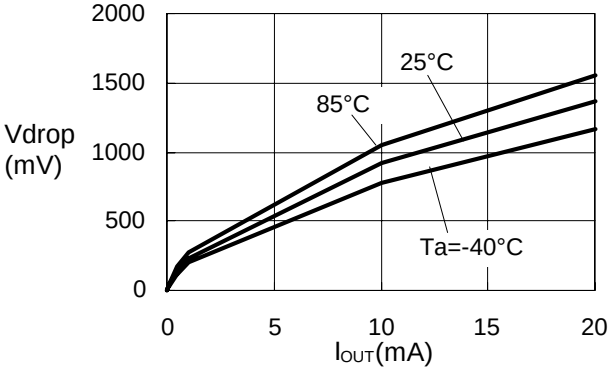



S-817B50A

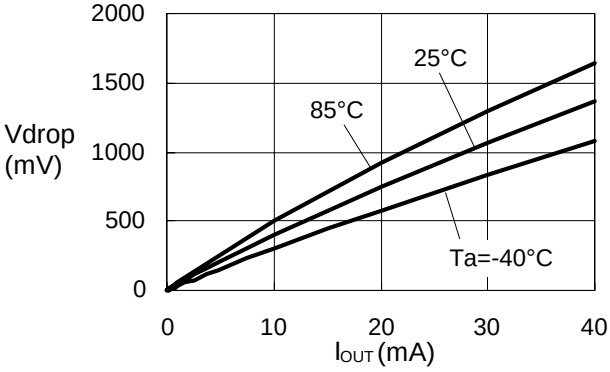


(4) DROPOUT VOLTAGE versus OUTPUT CURRENT

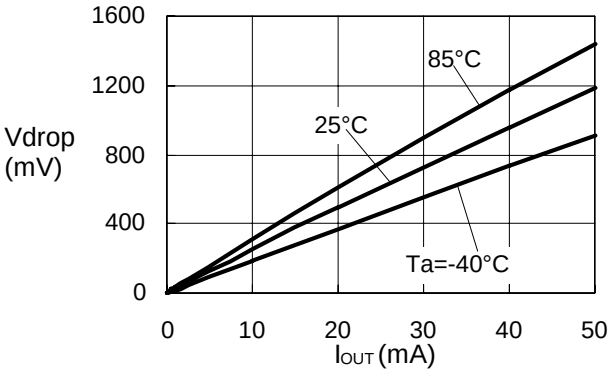
S-817A11A/S-817B11A



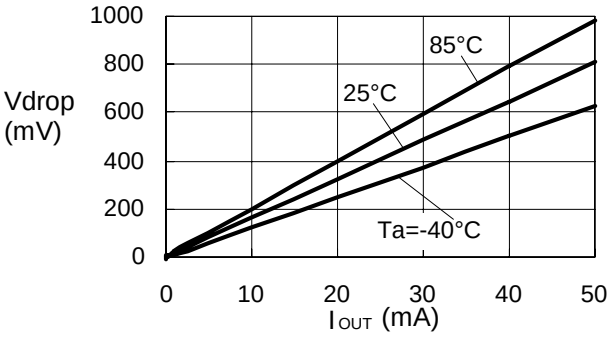

S-817A20A/S-817B20A




S-817A30A/S-817B30A

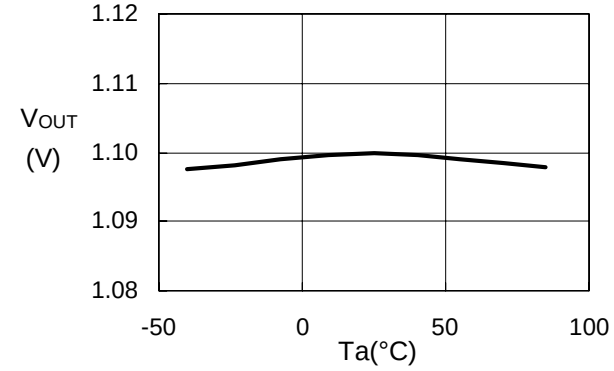



S-817A50A/S-817B50A

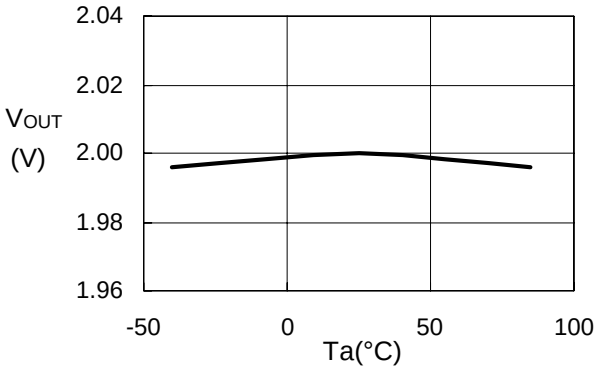



(5) OUTPUT VOLTAGE versus AMBIENT TEMPERATURE

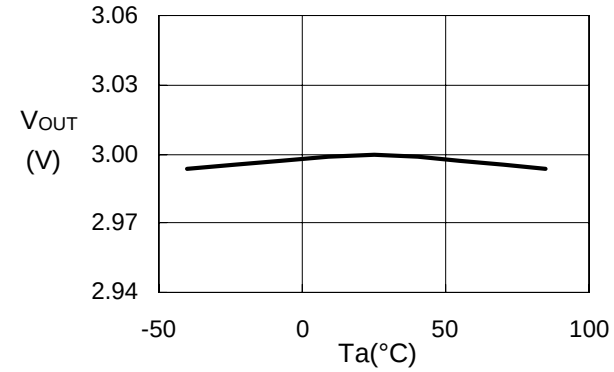
S-817A11A/S-817B11A $V_{IN}$=3.1V,$I_{OUT}$=10mA



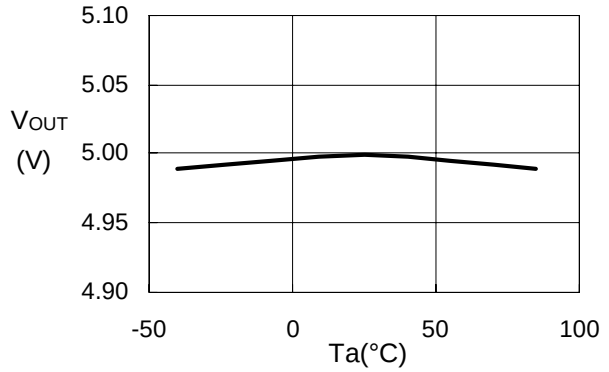

S-817A20A/S-817B20A $V_{IN}$=4V,$I_{OUT}$=10mA




S-817A30A/S-817B30A $V_{IN}$=5V,$I_{OUT}$=10mA

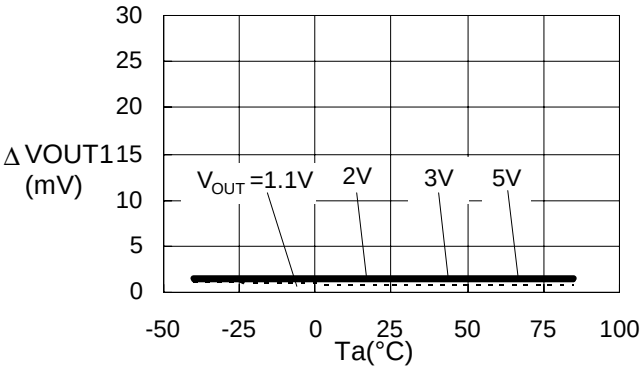



S-817A50A/S-817B50A $V_{IN}$=7V,$I_{OUT}$=10mA



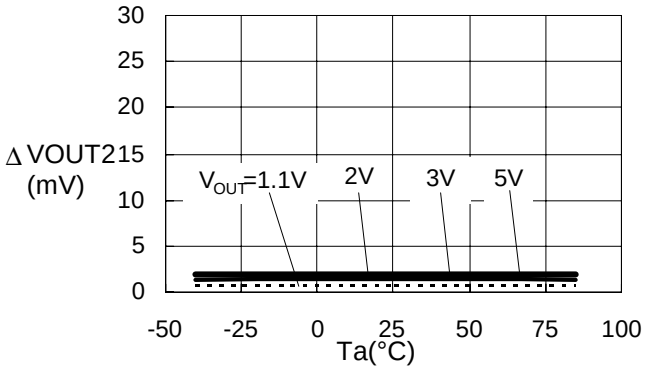
(6) LINE REGULATION 1 versus AMBIENT TEMPERATURE

S-817A11/20/30/50A
S-817B11/20/30/50A $V_{IN}=V_{OUT}(S)+1V\leftrightarrow10V, I_{OUT}=1mA$



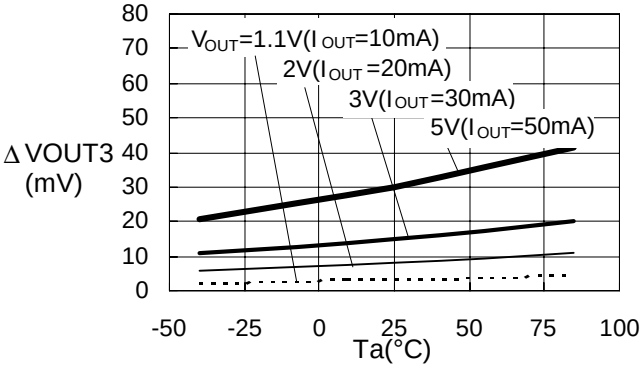

(7) LINE REGULATION 2 versus AMBIENT TEMPERATURE

S-817A11/20/30/50A
S-817B11/20/30/50A $V_{IN}=V_{OUT}(S)+1V\leftrightarrow10V, I_{OUT}=1\mu A$



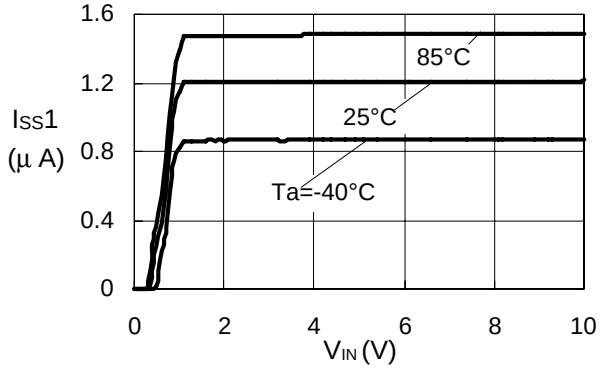

(8) LOAD REGULATION versus AMBIENT TEMPERATURE

S-817A11/20/30/50A
S-817B11/20/30/50A $V_{IN}=V_{OUT}(S)+2V, I_{OUT}=1\mu A\leftrightarrow I_{OUT}$

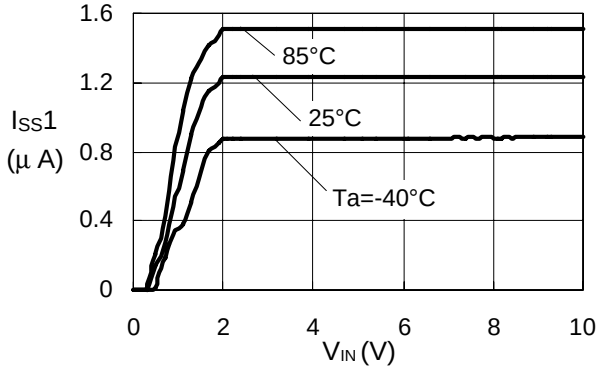



(9) CURRENT CONSUMPTION versus INPUT VOLTAGE

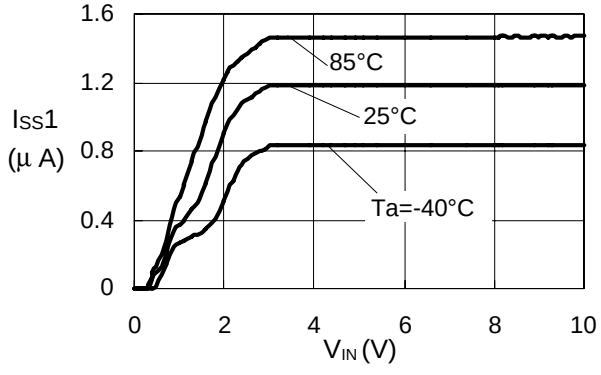
S-817A11A/S-817B11A



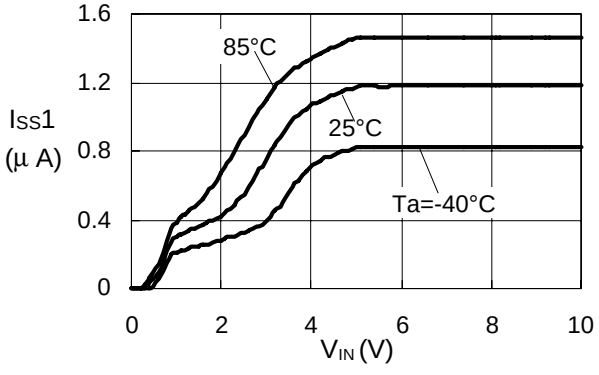

S-817A20A/S-817B20A




S-817A30A/S-817B30A

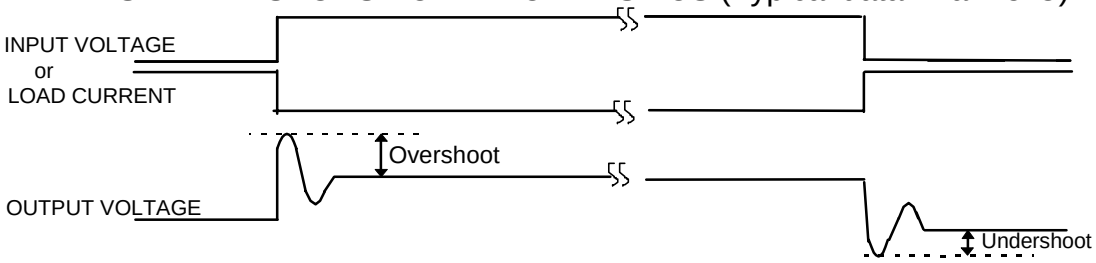



S-817A50A/S-817B50A



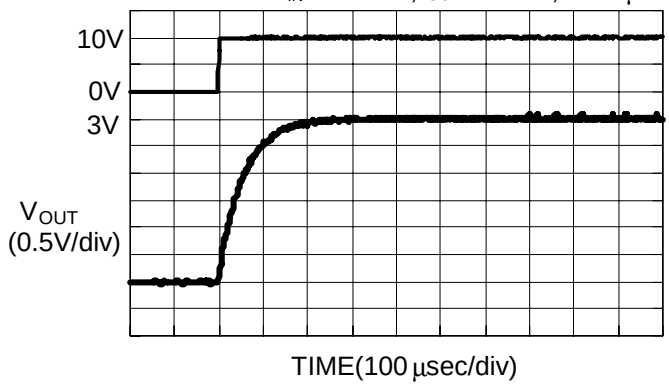
## REFERENCE DATA

### ■ TRANSIENT RESPONSE CHARACTERISTICS (Typical data: Ta=25°C)



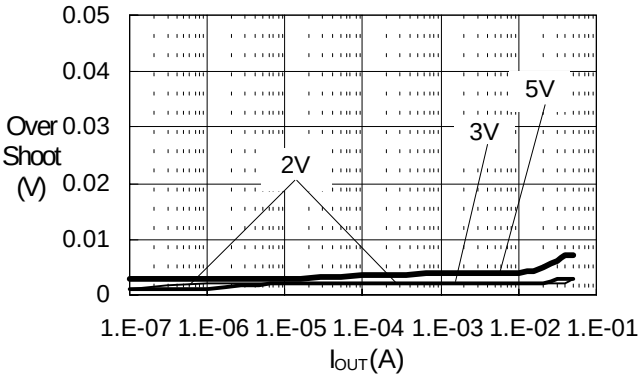

(1) At powering on S-817A30A (when using a ceramic capacitor, CL=1μF)

$V_{IN}$=0→10V,$I_{OUT}$=10mA, CL=1μF



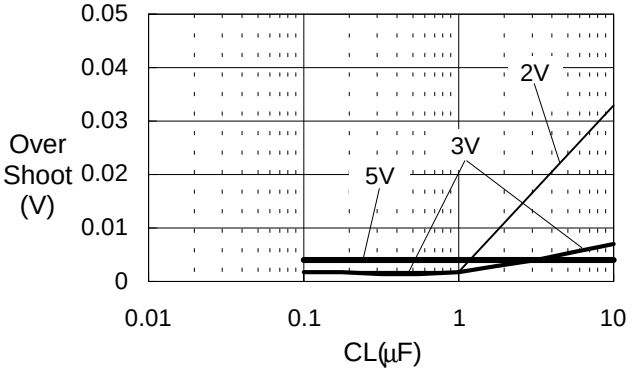

Load dependencies of overshoot at powering on

$V_{IN}$=0→$V_{OUT}$(S)+2V,CL=1μF



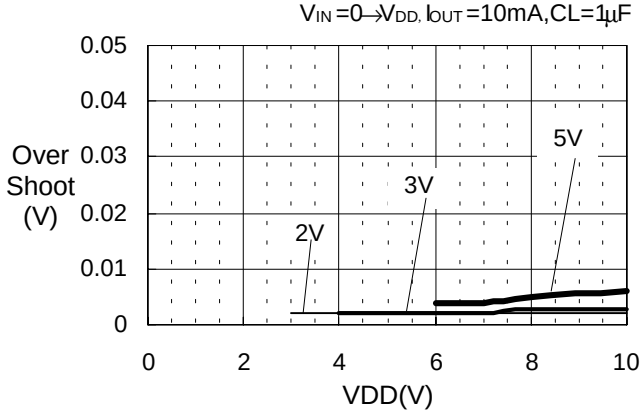

CL dependencies of overshoot at powering on

$V_{IN}$=0→$V_{OUT}$(S)+2V,$I_{OUT}$=10mA



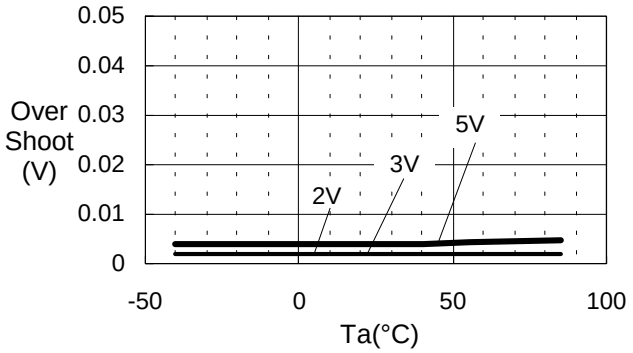

VDD dependencies of overshoot at powering on

$V_{IN}$=0→$V_{DD}$, $I_{OUT}$=10mA,CL=1μF

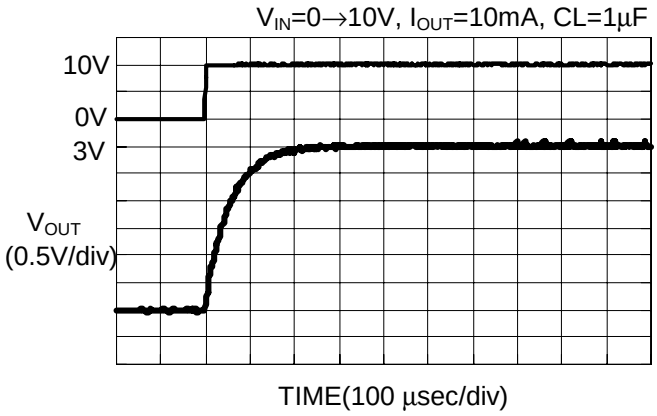



"Ta" dependencies of overshoot at powering on

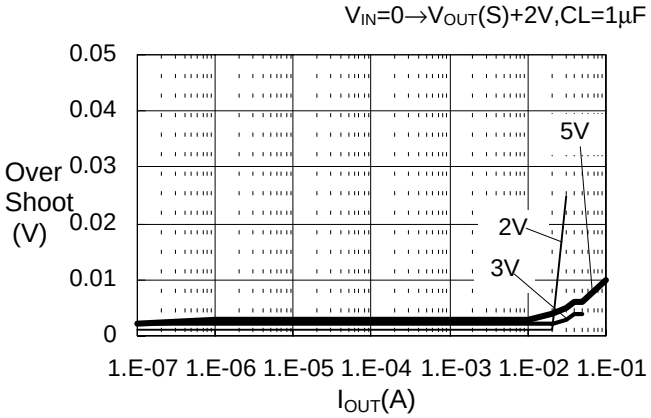
$V_{IN}$=0→$V_{OUT}$(S)+2V
$I_{OUT}$=10mA,CL=1μF



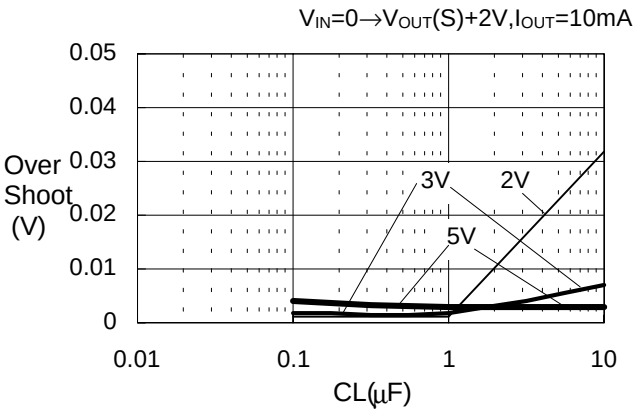
(2) At powering on S-817B30A (when using a ceramic capacitor, CL=1µF)



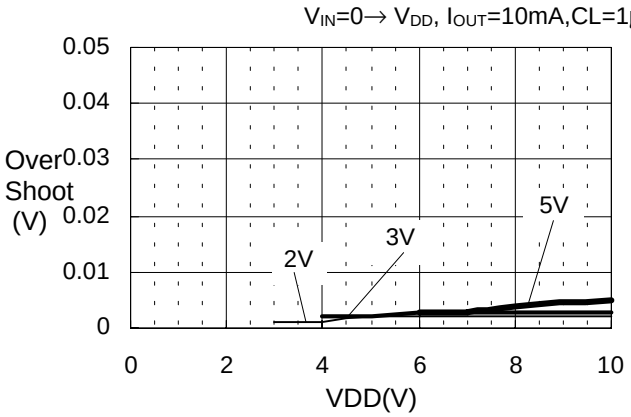

Load dependencies of overshoot at powering on



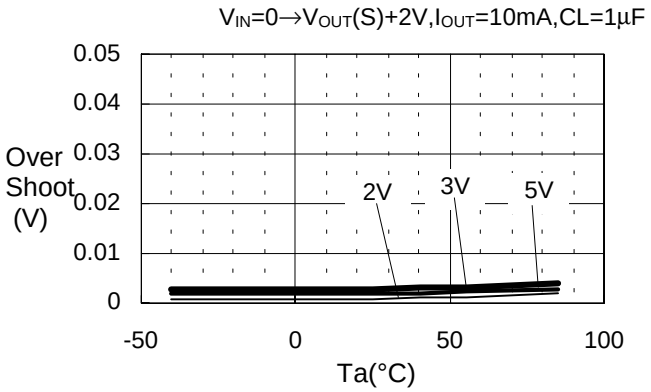

CL dependencies of overshoot at powering on



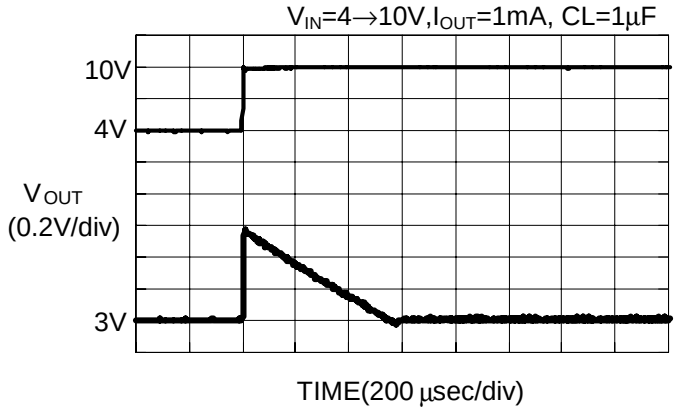

VDD dependencies of overshoot at powering on



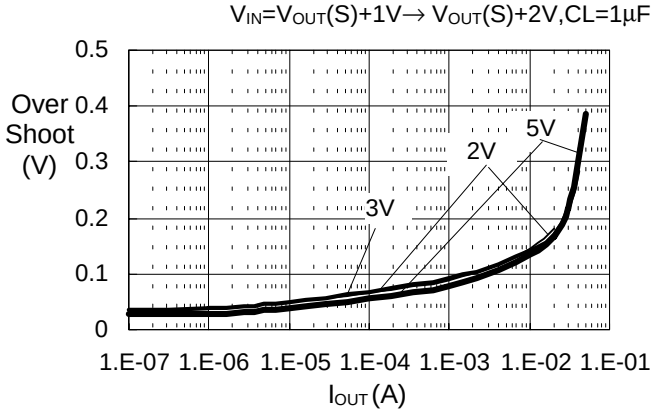

"Ta" dependencies of overshoot at powering on



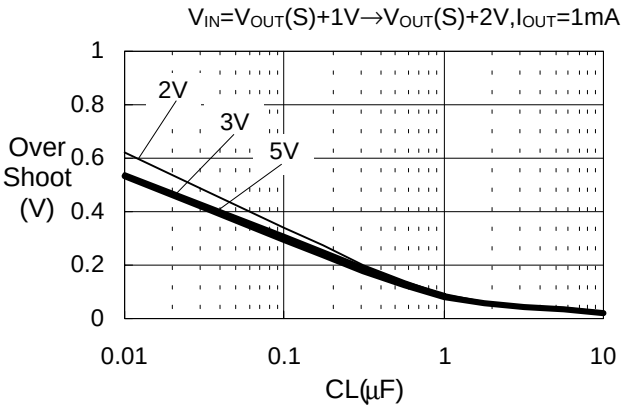
(3) Power fluctuation S-817A30A/S-817B30A (when using a ceramic capacitor, CL=1μF)



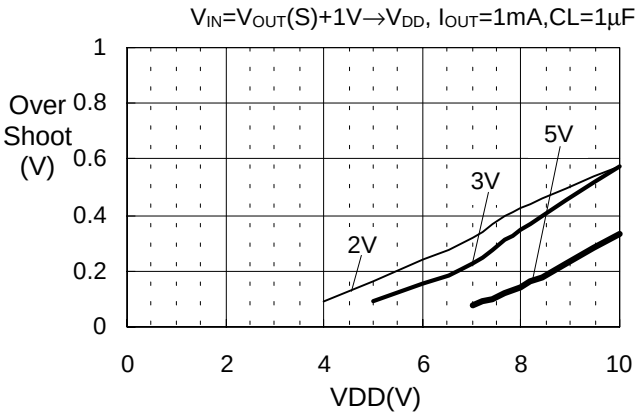

Load dependencies of overshoot at power fluctuation



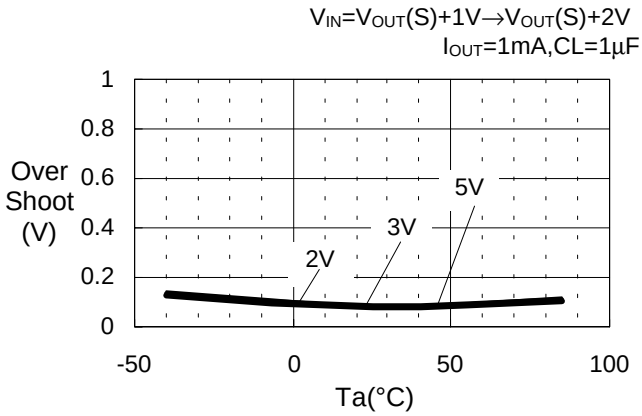

CL dependencies of overshoot at power fluctuation

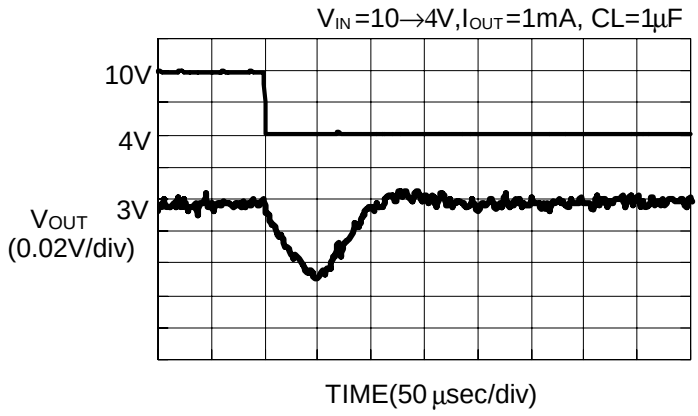



VDD dependencies of overshoot at power fluctuation

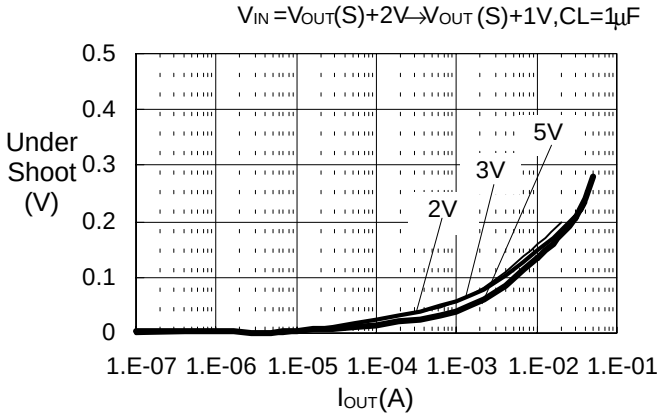



"Ta" dependencies of overshoot at power fluctuation

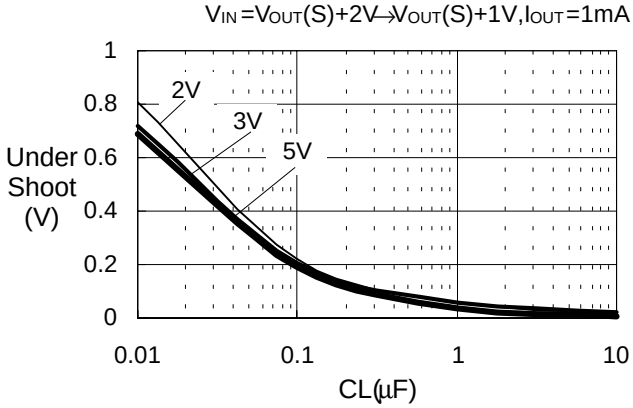




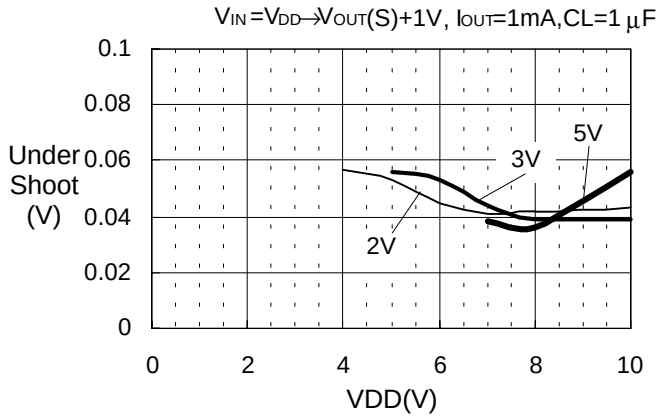

Load dependencies of undershoot at power fluctuation



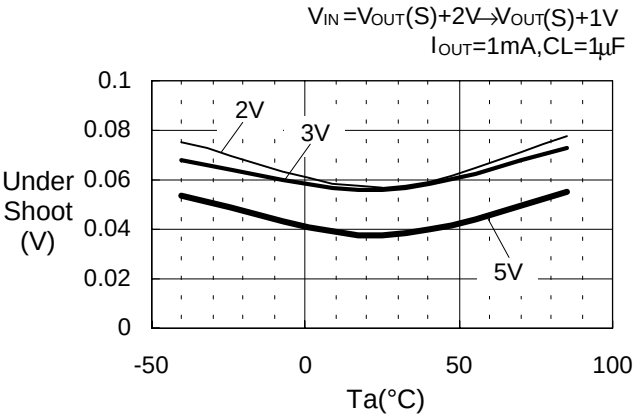

CL dependencies of undershoot at power fluctuation



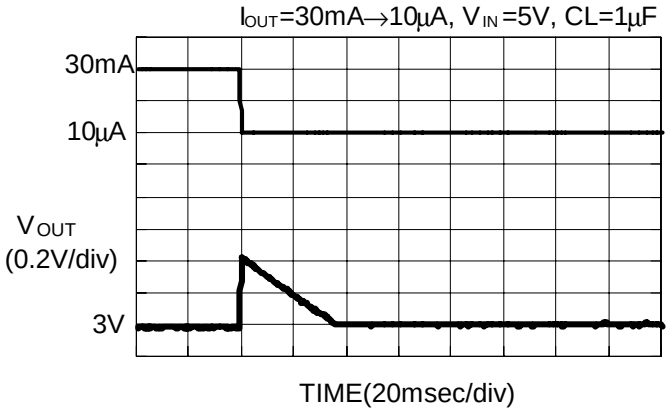

VDD dependencies of undershoot at power fluctuation



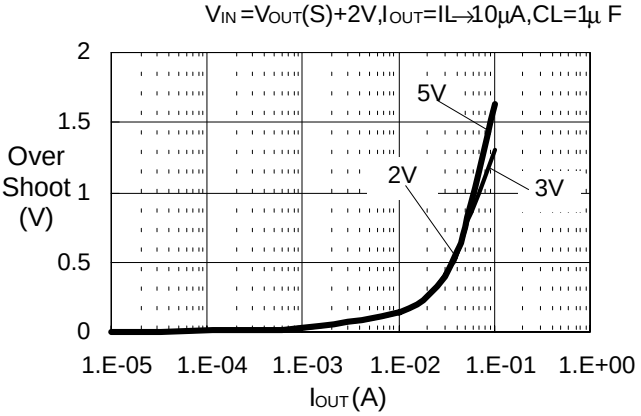

"Ta" dependencies of undershoot at power fluctuation



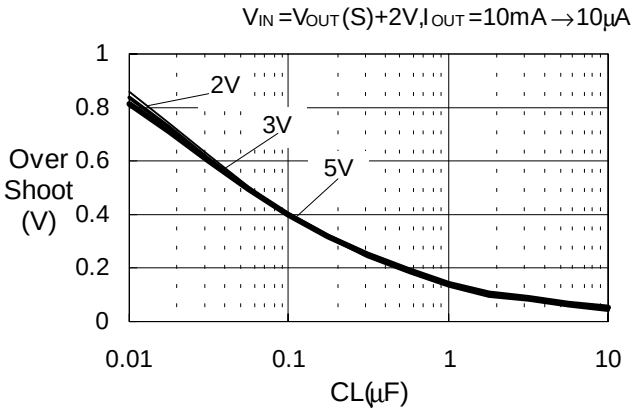
(4) Load fluctuation S-817A30A/S-817B30A (when using a ceramic capacitor, CL=1μF)



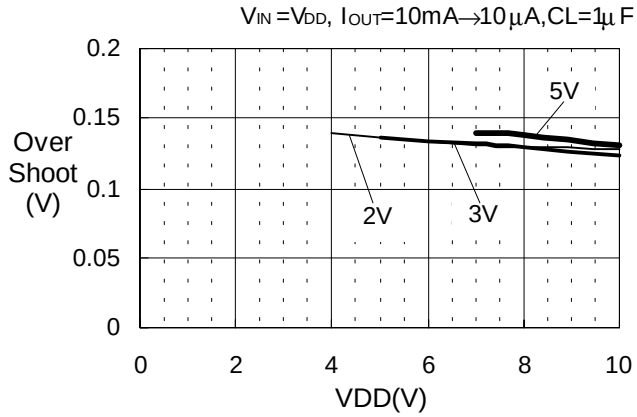

Load current dependencies of overshoot at load fluctuation



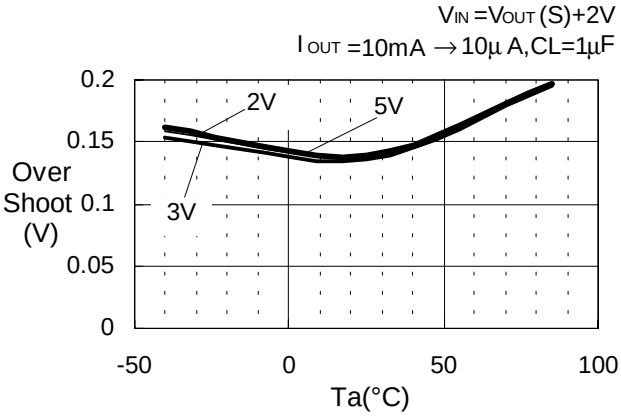

CL dependencies of overshoot at load fluctuation

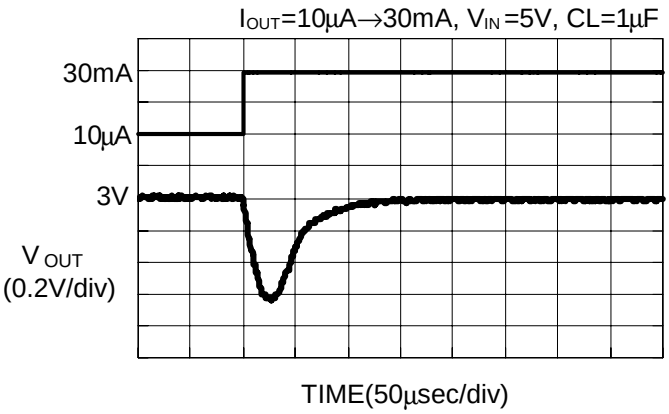



VDD dependencies of overshoot at load fluctuation

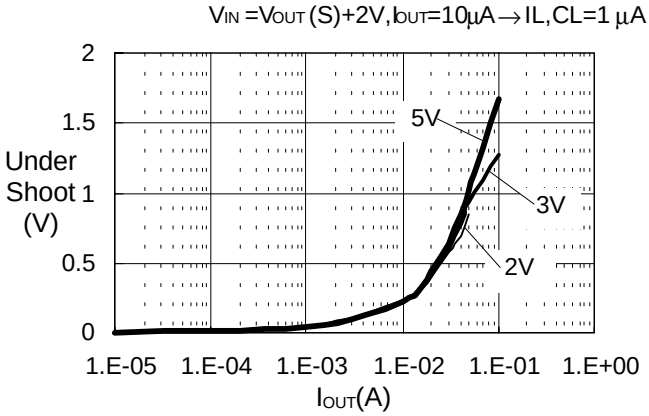



"Ta" dependencies of overshoot at load fluctuation

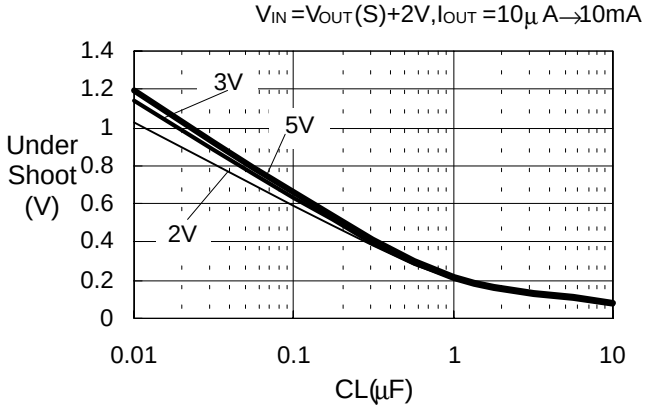




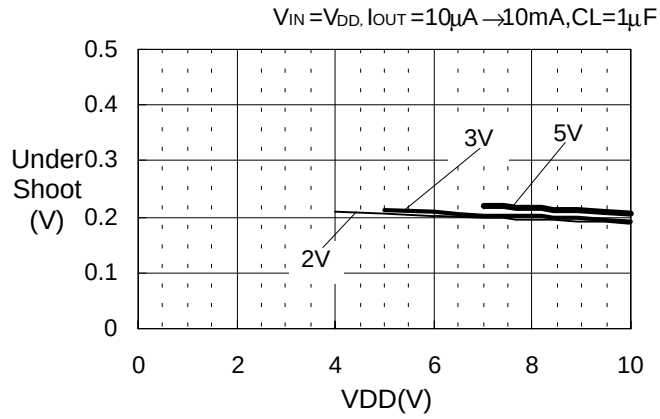

Load current dependencies of undershoot at load fluctuation



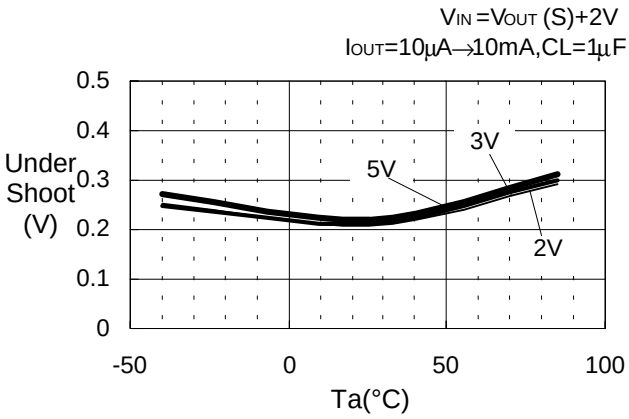

CL dependencies of undershoot at load fluctuation




VDD dependencies of undershoot at load fluctuation



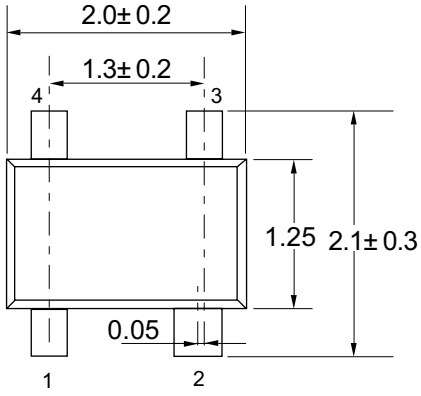

"Ta" dependencies of undershoot at load fluctuation

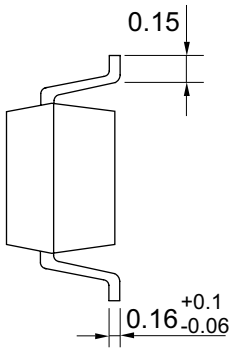


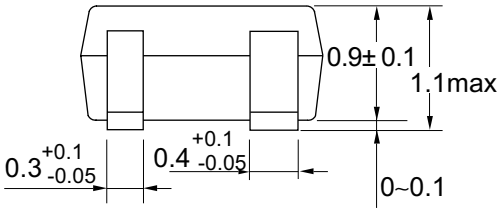
# ■ SC-82AB

Unit:mm

## ●Dimensions

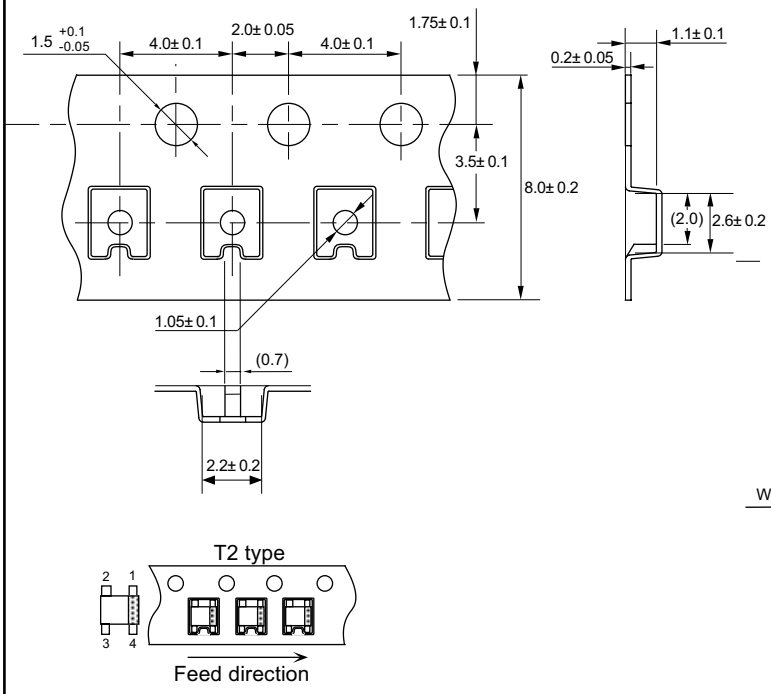



No.:NP004-A-P-SD-1.0

## ●Taping Specifications



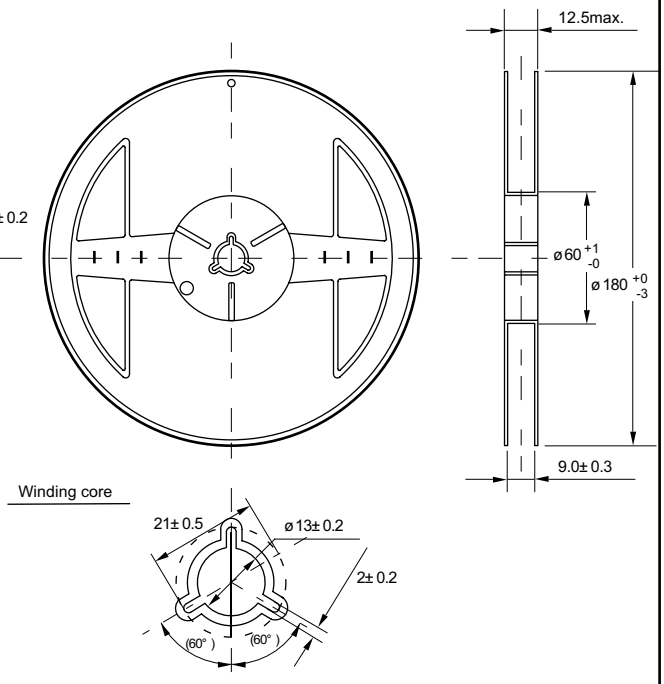




No.:NP004-A-C-SD-1.0

## ●Reel Specifications

1 reel holds 3000 ICs.



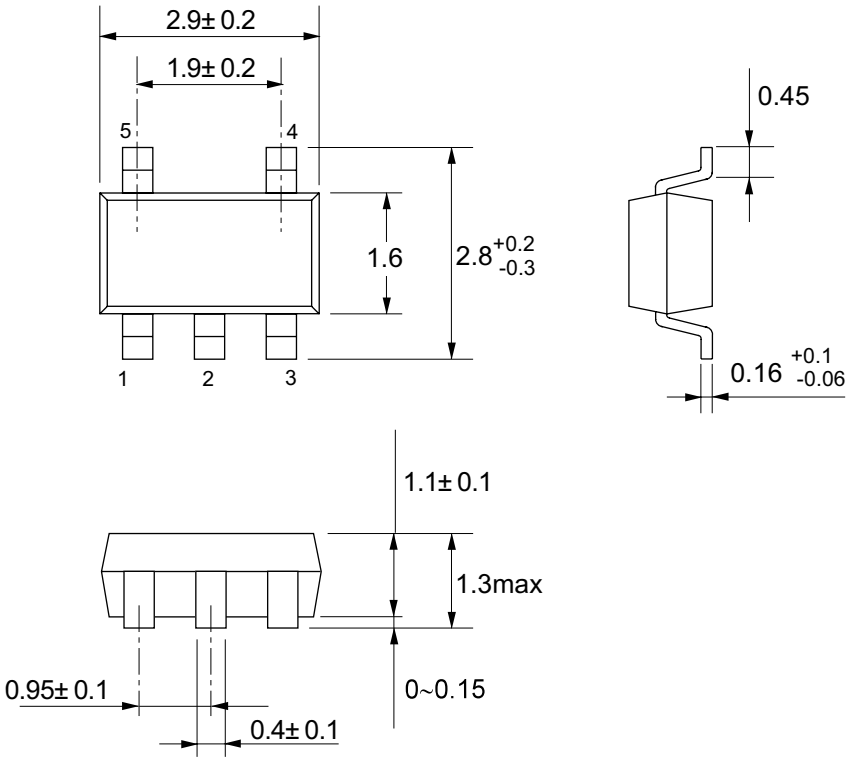

No.:NP004-A-R-SD-1.0

## ■ SOT-23-5

MP005-A 991105

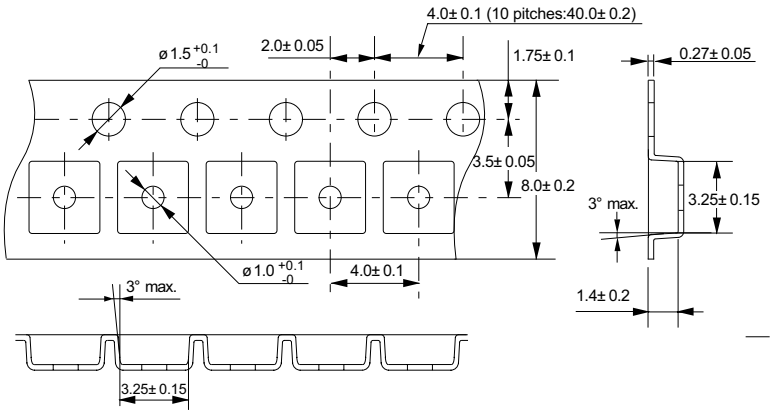
Unit: mm

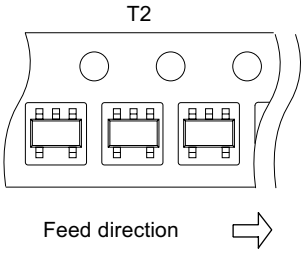
### ●Dimensions




No.:MP005-A-P-SD-1.0

### ●Taping Specifications

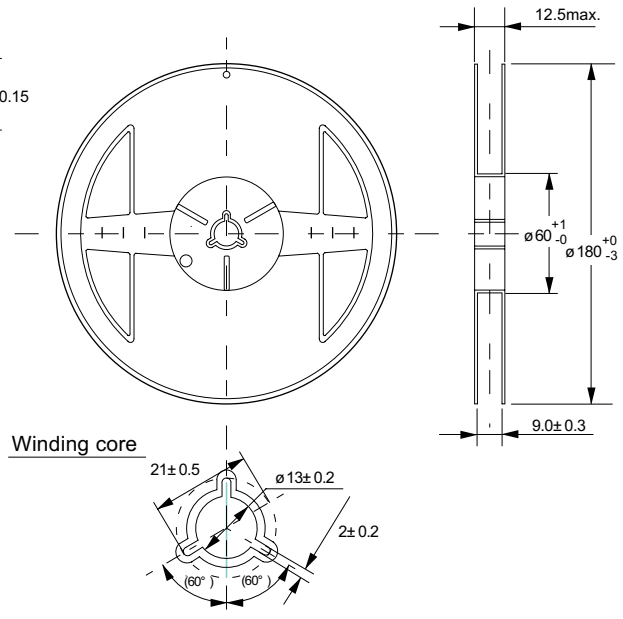



No.:MP005-A-C-SD-1.0

### ●Reel Specifications

3000 pcs./reel




No.:MP005-A-R-SD-1.0

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