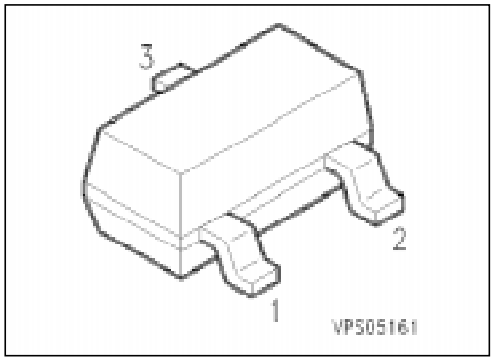
SIEMENS

Silicon N Channel MOS FET Triode — BF 543

Preliminary Data

- For RF stages up to 300 MHz preferably in FM applications
- I_{DSS} = 4 mA, g_{fs} = 12 mS



ESD: Electro**s**tatic **d**ischarge sensitive device, observe handling precautions!

Type	Marking	Ordering Code (tape and reel)	Pin Configuration 1	2	3	Package[1)]
BF 543	LDs	Q62702-F1372	G	D	S	SOT-23

Maximum Ratings

Parameter	Symbol	Values	Unit
Drain-source voltage	V_{DS}	20	V
Drain current	I_D	30	mA
Gate-source peak current	$\pm I_{GSM}$	10	
Total power dissipation, $T_A \leq 60$ °C	P_{tot}	200	mW
Storage temperature range	T_{stg}	– 55 … + 150	°C
Channel temperature	T_{ch}	150	
Ambient temperature range	T_A	– 55 … + 150	

Thermal Resistance

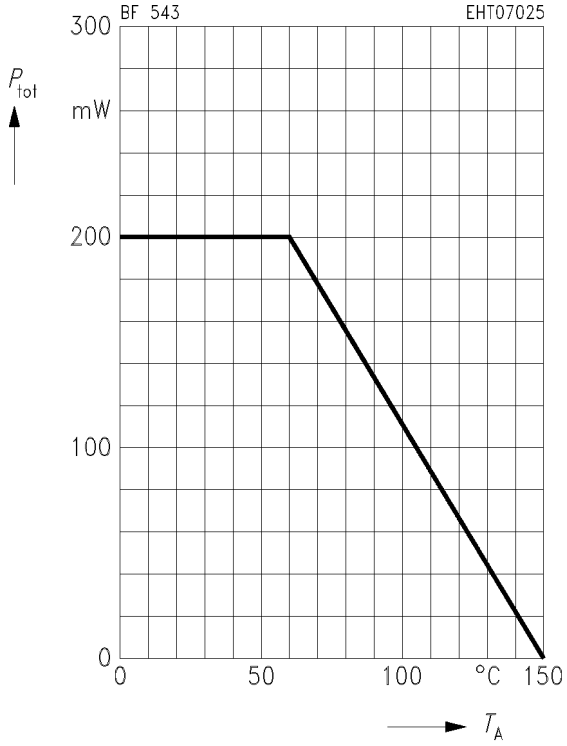
Junction - ambient[2)]	$R_{th\ JA}$	≤ 450	K/W

1) For detailed information see chapter Package Outlines.
2) Package mounted on alumina 15 mm × 16.7 mm × 0.7 mm.

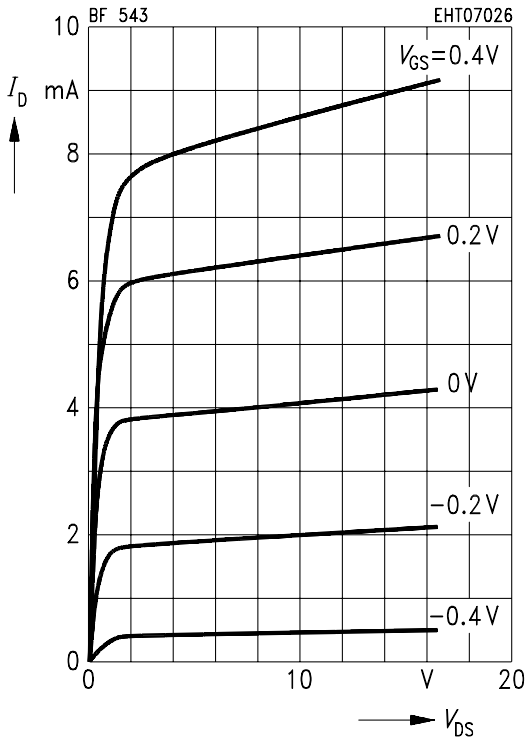
Electrical Characteristics
at T_A = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage I_D = 10 µA, – V_{GS} = 4 V	$V_{(BR)DS}$	20	–	–	V
Gate-source breakdown voltage ± I_{GS} = 10 mA, V_{DS} = 0	±$V_{(BR)GSS}$	7	–	12	
Gate cutoff current ± V_{GS} = 6 V, V_{DS} = 0	± I_{GSS}	–	–	50	nA
Drain current V_{DS} = 10 V, V_{GS} = 0	I_{DSS}	2.0	4	6.0	mA
Gate-source pinch-off voltage V_{DS} = 10 V, I_D = 20 µA	– $V_{GS(p)}$	–	0.7	1.5	V
AC Characteristics					
Forward transconductance V_{DS} = 10 V, I_D = 4 mA, f = 1 kHz	g_{fs}	9.5	12	–	mS
Gate-1 input capacitance V_{DS} = 10 V, I_D = 4 mA, f = 1 MHz	C_{gss}	–	2.7	–	pF
Reverse transfer capacitance V_{DS} = 10 V, I_D = 4 mA, f = 1 MHz	C_{dg}	–	18	–	fF
Output capacitance V_{DS} = 10 V, I_D = 4 mA, f = 1 MHz	C_{dss}	–	0.9	–	pF
Power gain (test circuit) V_{DS} = 10 V, I_D = 4 mA, f = 200 MHz G_G = 2 mS, G_L = 0.5 mS	G_p	–	22	–	dB
Noise figure (test circuit) V_{DS} = 10 V, I_D = 4 mA, f = 200 MHz G_G = 2 mS, G_L = 0.5 mS	F	–	1	–	

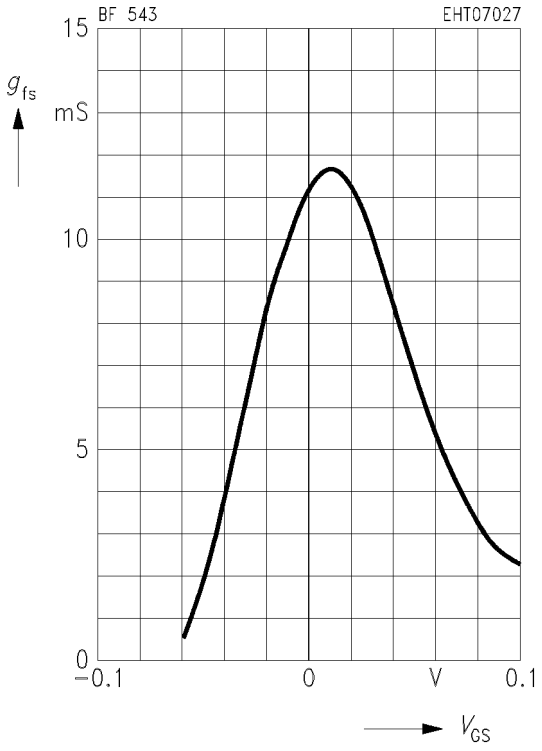
Total power dissipation $P_{tot} = f(T_A)$



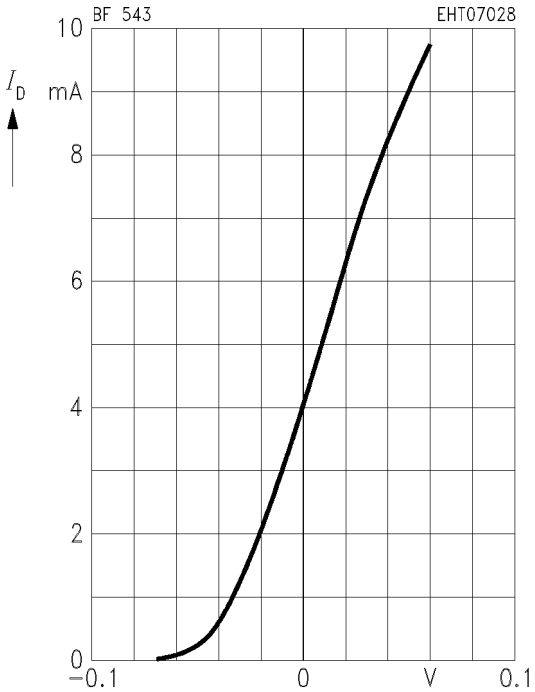
Typ. output characteristics $I_D = f(V_{DS})$



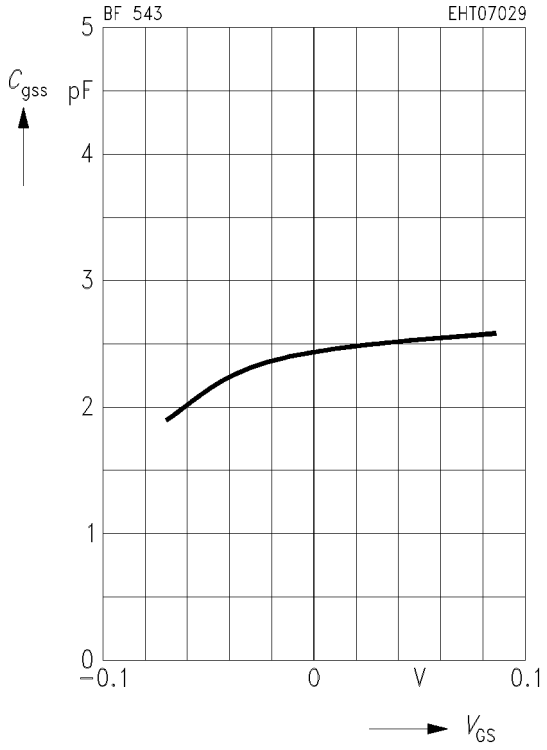
Gate transconductance $g_{fs} = f(V_{GS})$
V_{DS} = 10 V, I_{DSS} = 4 mA, f = 1 kHz



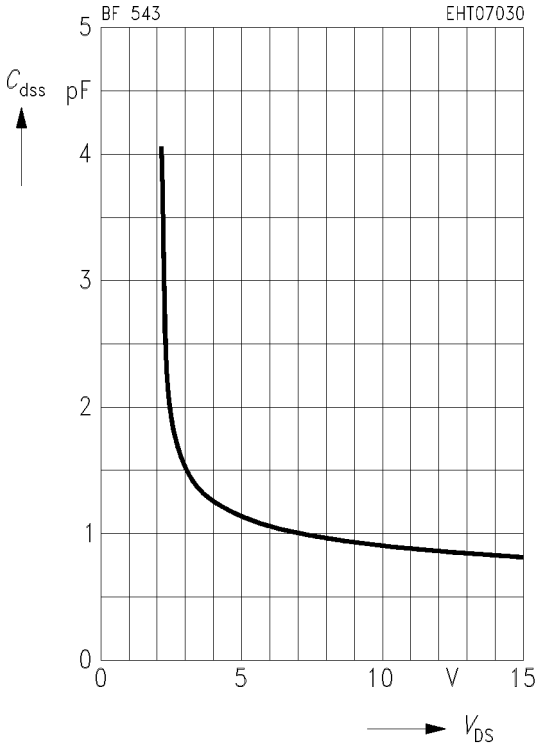
Drain current $I_D = f(V_{GS})$
V_{DS} = 10 V



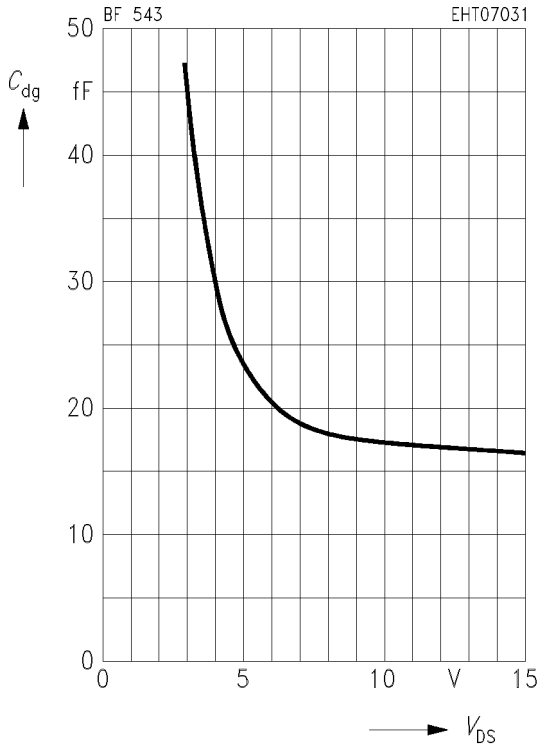
Gate input capacitance $C_{gss} = f(V_{GS})$
V_{DS} = 10 V, I_{DSS} = 4 mA, f = 1 MHz



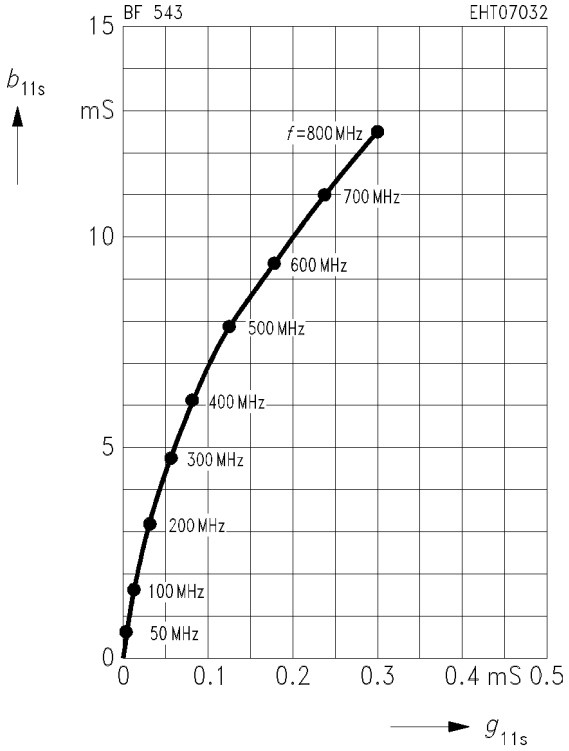
Output capacitance $C_{dss} = f(V_{DS})$
V_{GS} = 0, I_{DSS} = 4 mA, f = 1 MHz



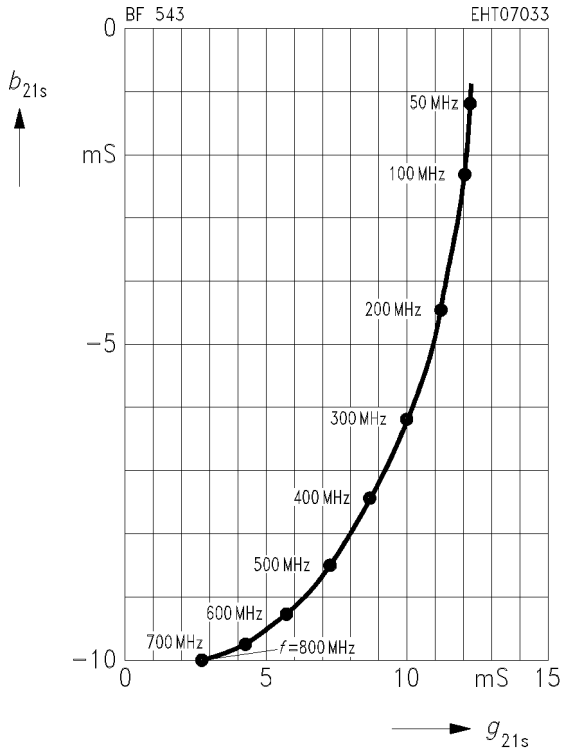
Reverse transfer capacitance $C_{dg} = f(V_{DS})$
V_{GS} = 0, I_{DSS} = 4 mA, f = 1 MHz



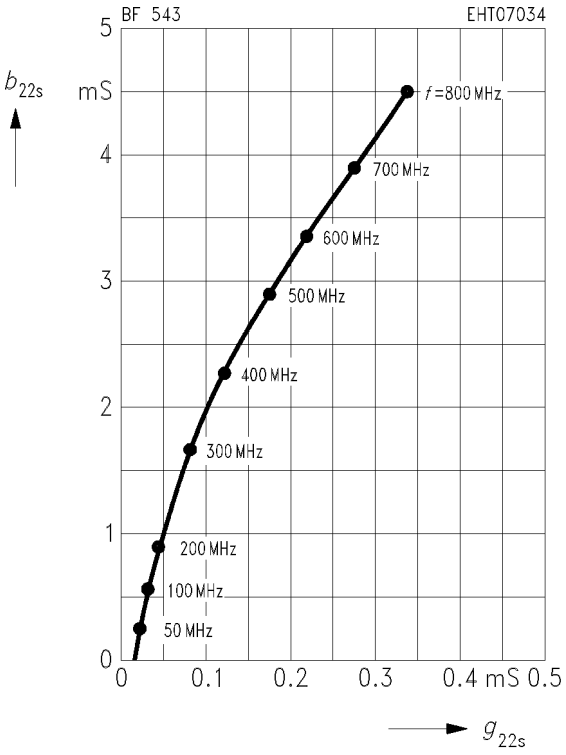
Gate 1 input admittance y_{11s}
V_{DS} = 10 V, I_{DSS} = 4 mA, V_{GS} = 0
(source circuit)



Gate 1 transconductance y_{21s}
V_{DS} = 10 V, I_{DSS} = 4 mA, V_{GS} = 0
(source circuit)



Output admittance y_{22s}
V_{DS} = 10 V, I_{DSS} = 10 mA, V_{GS} = 0
(source circuit)



Test circuit for power gain G_p and noise figure F
f= 200 MHz, G_G = 2 mS, G_L = 0.5 mS