SHARP

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FLASH MEMORY
LH28F016SANS-70
Ver.1.1

SHARP CORPORATION
Flash Memory Engineering Department 2
Memory Engineering Center
Tenri Integrated Circuits Development (IC) Group

LH28F016SANS-70
16 Mbit (1 Mbit x 16, 2 Mbit x 8)
Flash Memory

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FLASH MEMORY

FEATURES

- **User-Selectable 3.3V or 5V V_{CC}**
- **User-Configurable x8 or x16 Operation**
- **70 ns Maximum Access Time**
- **0.43 MB/sec Write Transfer Rate**
- **100 Thousand Erase Cycles per Block**
- **56-Lead, 1.2mm x 14mm x 20mm SSOP Package**
- **Revolutionary Architecture**
  - **Pipelined Command Execution**
  - **Write During Erase**
  - **Command Superset of Sharp LH28F008SA**
- **50 µA (TYP.) I_{CC} in CMOS Standby**
- **1 µA (TYP.) Deep Power-Down**
- **32 Independently Lockable Blocks**
- **State-of-the-Art 0.55 µm ETOX™* Flash Technology**
- **Not designed or rated as radiation hardened**

Sharp's LH28F016SANS-70 16-Mbit Flash Memory is a revolutionary architecture which enables the design of truly mobile, high performance, personal computing and communication products. With innovative capabilities and very high read/write performance, the LH28F016SANS-70 is also the ideal choice for designing embedded mass storage flash memory systems.

The LH28F016SANS-70 is a very high density, highest performance non-volatile read/write solution for solid-state storage applications. Its symmetrically blocked architecture (100% compatible with the LH28F008SA 8-Mbit Flash memory), extended cycling, low power 3.3V operation, very fast write and read performance and selective block locking provide a highly flexible memory component suitable for high density memory cards, Resident Flash Arrays and PCMCIA-ATA Flash Drives. The LH28F016SANS-70's dual read voltage enables the design of memory cards which can interchangeably be read/written in 3.3V and 5.0V systems. Its x8/x16 architecture allows the optimization of memory to processor interface. The flexible block locking option enables bundling of executable application software in a Resident Flash Array or memory card. Manufactured on Sharp's 0.55 µm ETOX™* process technology, the LH28F016SANS-70 is the most cost-effective, high-density flash memory.

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* ETOX is a trademark of Intel corporation.

1.0 INTRODUCTION

The specifications intended to give an overview of the chip feature-set and of the operating AC/DC specifications. Please refer to User's Manual also, to learn detail usage.

1.1 Product Overview

The LH28F016SANS-70 is a high performance 16 Mbit (16,777,216 bit) block erasable non-volatile random access memory organized as either 1 Mword × 16 or 2 Mbyte × 8. The LH28F016SANS-70 includes sixteen 64 KB (65,536) blocks or sixteen 32-KW (32,768) blocks. A chip memory map is shown in Figure 3.

The implementation of a new architecture, with many enhanced features, will improve the device operating characteristics and results in greater product reliability and ease of use.

Among the significant enhancements of the LH28F016SANS-70:

- 3.3V Low Power Capability
- Improved Write Performance
- Dedicated Block Write/Erase Protection

A 3/5# input pin reconfigures the device internally for optimized 3.3V or 5.0V read/write operation.

The LH28F016SANS-70 will be available in a 56-lead, SSOP. The form factor and pinout allow for very high board layout densities.

A Command User Interface (CUI) serves as the system interface between the microprocessor or micro-controller and the internal memory operation.

Internal Algorithm Automation allows Byte/Word Writes and Block Erase operations to be executed using a Two-Write command sequence to the CUI in the same way as the LH28F008SA 8-Mbit Flash memory.

A Superset of commands have been added to the basic LH28F008SA command-set to achieve higher write performance and provide additional capabilities. These new commands and features include:

- Page Buffer Writes to Flash
- Command Queuing Capability
- Automatic Data Writes During Erase
- Software Locking of Memory Blocks
- Two-Byte Successive Writes in 8-bit Systems
- Erase All Unlocked Blocks

Writing of memory data is performed in either byte or word increments typically within 6 µsec, a 33% improvement over the LH28F008SA. A Block Erase operation erases one of the 32 blocks in typically 0.6 sec, independent of the other blocks, which is about 65% improvement over the LH28F008SA.

The LH28F016SANS-70 incorporates two Page Buffers of 256 Bytes (128 Words) each to allow page data writes. This feature can improve a system write performance over previous flash memory devices.

All operations are started by a sequence of Write commands to the device. Three Status Registers (described in detail later) and a RY/BY# output pin provide information on the progress of the requested operation.

While the LH28F008SA requires an operation to complete before the next operation can be requested, the LH28F016SANS-70 allows queuing of the next operation while the memory executes the current operaion. This eliminates system overhead when writing several bytes in a row to the array or erasing several blocks at the same time. The LH28F016SANS-70 can also perform write operations to one block of memory while performing erase of another block.

The LH28F016SANS-70 provides suer-selectable block locking to protect code or data such as Device Drivers, PCMCIA card information, ROM-Executable O/S or Application Code. Each block has an associated non-volatile lock-bit which determines the lock status of the block. In addition, the LH28F016SANS-70 incorporates Master Write Protection Pin (WP#). When WP# turns V_{IL} after Block Lock command was issued, the device realizes Block Lock capability. When WP# is V_{IH}, any Write or Erase operation can be performed in spite of Block Lock status. When WP# is V_{IL}, please note following points.

1. When Wp# is V_{IL}, any execution for Block Lock command. It is accomplished by keeping WP# V_{IH} to execute Block Lock command.
2. When WP# is V_{IL} and also if power off occurs or Reset, Abort command is issued during executing Erase operation, there is a possibility that the Block in which Erase operation is in progress turns to protected Block and succeeding Erase/Write operation in that Block can not be executed. In this case, turn WP# to V_{IH} and also execute Block Erase operation for that Block or execute Full chip Erase operation.

The LH28F016SANS-70 contains three types of Status Registers to accomplish various functions:

- A Compatible Status Register (CSR) which is 100% compatible with the LH28F008SA Flash memory's Status Register. This register, when used alone, provides a straightforward upgrade capability to the LH28F016SANS-70 from a LH28F008SA-based design.
- A Global Status Register (GSR) which informs the system of command Queue status, Page Buffer status, and overall Write State Machine (WSM) status.
- 32 Block Status Registers (BSRs) which provide block-specific status information such as the block lock-bit status.

The GSR and BSR memory maps for Byte-Wide and Word-Wide modes are shown in Figures 4.1 and 4.2.

The LH28F016SANS-70 incorporates an open drain RY/BY# output pin. This feature allows the user to OR-tie many RY/BY# pins together in a multiple memory configuration such as a Resident Flash Array.

The LH28F016SANS-70 also incorporates a dual chip-enable function with two input pins, CE_0# and CE_1#. These pins have exactly the same functionality as the regular chip-enable pin CE# on the LH28F008SA. For minimum chip designs, CE_1# may be tied to ground and use CE_0# as the chip enable input. The LH28F016SANS-70 uses the logical combination of these two signals to enable or disable the entire chip. Both CE_0# and CE_1# must be active low to enable the device and if either one becomes inactive, the chip will be disabled. This feature, along with the open drain RY/BY# pin, allows the system designer to reduce the number of control pins used in a large array of 8-Mbit devices.

The BYTE# pin allows either x8 or x16 read/writes to the LH28F016SANS-70. BYTE# at logic low selects 8-bit mode with address A_0 selecting between low byte and high byte. On the other hand, BYTE# at logic high enables 16-bit operation with address A_1 becoming the lowest order address and address A_0 is not used (don't care). A device diagram is shown in Figure 1.

The LH28F016SANS-70 is specified for a maximum access time of each version, as follows:

LH28F016SANS-70

Operating Temperature	Vcc Suply	Max. Access (t_{ACC})
0 - 70 °C	4.75 - 5.25 V	70 ns
0 - 70 °C	4.5 - 5.5 V	80 ns
0 - 70 °C	3.0 - 3.6 V	120 ns

The LH28F016SANS-70 incorporates an Automatic Power Saving (APS) feature which substantially reduces the active current when the device is in static mode of operation (addresses not switching).

In APS mode, the typical I_{CC} current is 2 mA at 5.0V (1 mA at 3.3V).

A Deep Power-Down mode of operation is invoked when the RP# (called PWD# on the LH28F008SA) pin transitions low, any current operation is aborted and the device is put into the deep power-down mode. This mode brings the device power consumption to less than 5 µA, typically, and provides additional write protection by acting as a device reset pin during power transitions. When the power is turned on, RP# pin turned to low order to return the device to default configuration. When the 3/5# pin is switched, or when the power transition is occurred, or at the power on/off, RP# is required to stay low in order to protect data from noise. A recovery time of 400ns (Vcc=5.0V±0.25V) is required from RP# switching high until outputs are again valid. In the Deep Power-Down state, the WSM is reset (any current operation will abort) and the CSR, GSR and BSR registers are cleared.

A CMOS Standby mode of operation is enabled when either CE_0# or CE_1# transitions high and RP# stays high with all input control pins at CMOS levels. In this mode, the device typically draws an I_{CC} standby current of 10 µA.

Please do not execute reprogramming "0" for the bit which has already been programed "0". Overwrite operation may generate unerasable bit. In case of reprogramming "0" to the data which has been programed "1".

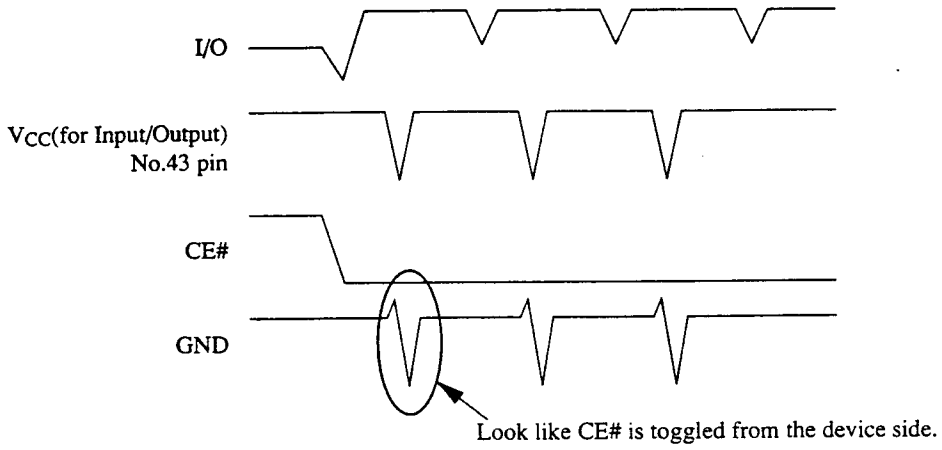
- Program "0" for the bit in which you want to change data from "1" to "0".
- Program "1" for the bit which has already been programmed "0".

For example, changing data from "10111101" to "10111100" requires "11111110" programming.

When you use LH28F016SANS-70, please note following points related to output buffer. When the device is in the reading mode, High-Low-High glidge may occurs (It is whithin the access time, not operation error.) In case of the device is used for application in which the GND/V_{CC} form system is tied by high-inductance connector or flat cable such as memory card, V_{CC} current which is generated by the glidge induces voltage difference at GND/V_{CC} between system and device. The detail mechanism is showed in following chart. In these kinds application, GND/V_{CC} pin (No. 42, No. 43) shoud be connected to a single line from outside. GND/V_{CC} lines from other devices should not be mixed.

Error operation caused by glidge occurs as follows.

1. Output High from I/O.
2. Glidge at I/O effects GND/V_{CC} for Input/Output.
3. Device judges CE# Low signal is reverced.
4. At the result Output is reset, outputs High again.



By way of example error operation caused mechanism by glidge occurs

2.0 DEVICE PINOUT

The LH28F016SANS-70 56L-SSOP configuration is shown in Figure 2.

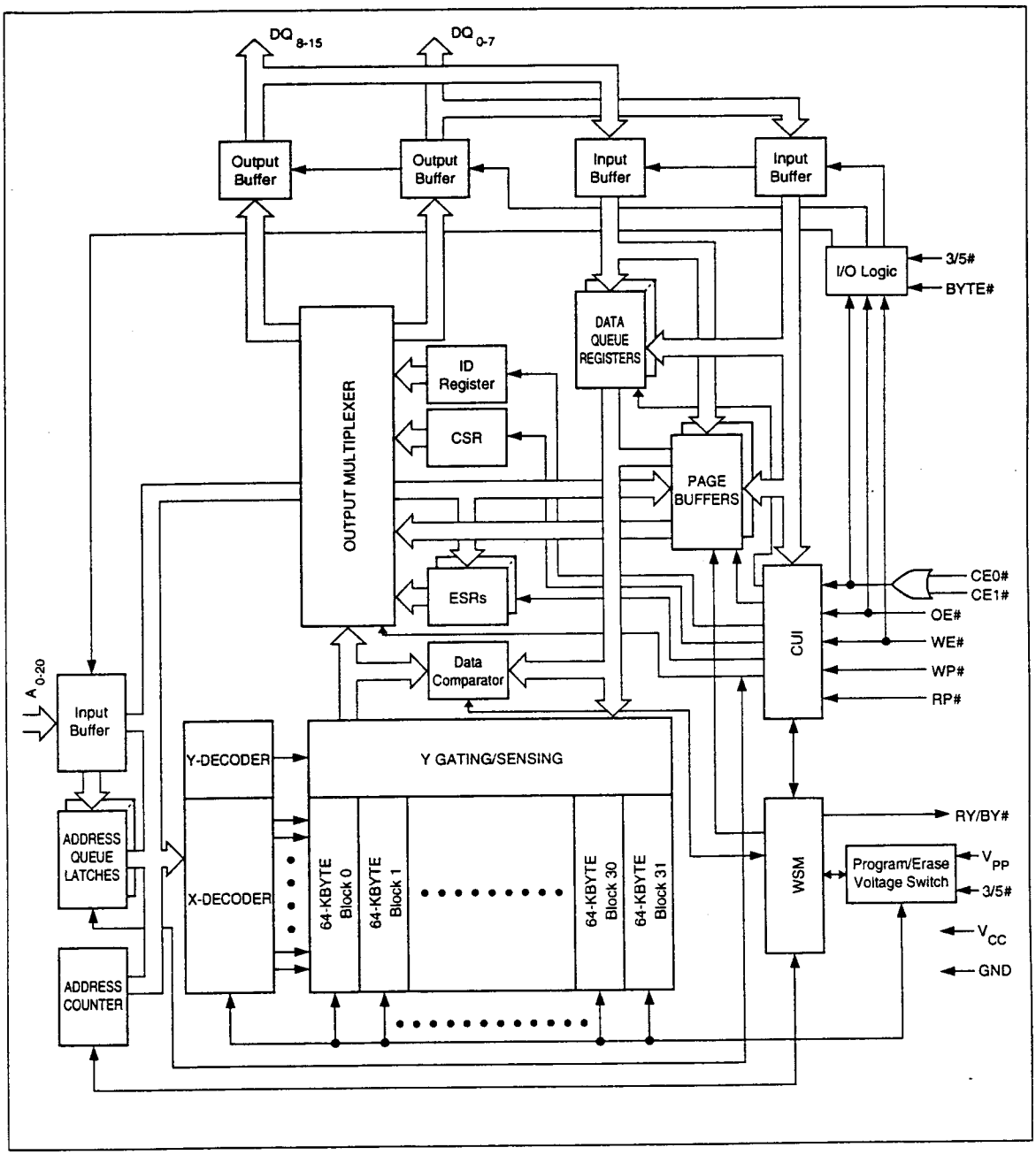


Figure 1. LH28F016SANS-70 Block Diagram

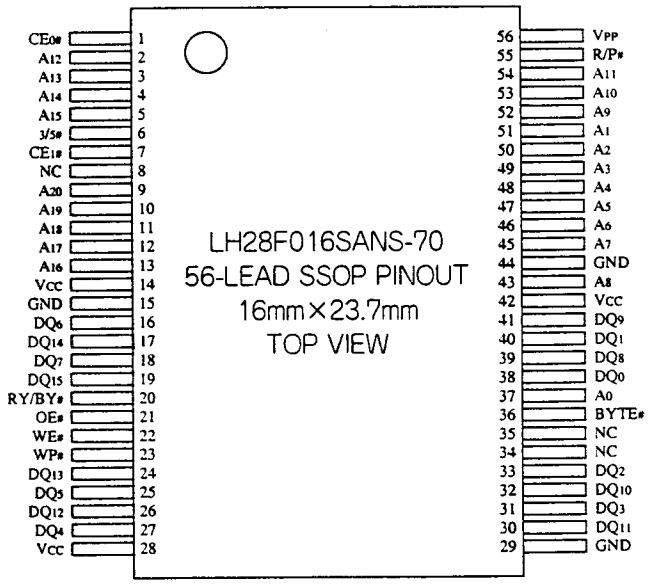
Architectural Evolution Includes Page Buffers, Queue Registers and Extended Status Registers.

2.1 Lead Descriptions

Symbol	Type	Name and Function
A_0	INPUT	**BYTE-SELECT ADDRESS:** Selects between high and low byte when device is in x8 mode. This address is latched in x8 Data Writes. Not used in x16 mode (i.e., the A_0 input buffer is turned off when BYTE# is high).
A_1-A_{15}	INPUT	**WORD-SELECT ADDRESSES:** Select a word within one 64-Kbyte block. $A_{6\text{-}15}$ selects 1 of 1024 rows, and $A_{1\text{-}5}$ selects 16 of 512 columns. These addresses are latched during Data Writes.
A_{16}-A_{20}	INPUT	**BLOCK-SELECT ADDRESSES:** Select 1 of 32 Erase blocks. These addresses are latched during Data Writes, Erase and Lock-Block operations.
DQ_0-DQ_7	INPUT/OUTPUT	**LOW-BYTE DATA BUS:** Inputs data and commands during CUI write cycles. Outputs array, buffer, identifier or status data in the appropriate Read mode. Floated when the chip is de-selected or the outputs are disabled.
DQ_8-DQ_{15}	INPUT/OUTPUT	**HIGH-BYTE DATA BUS:** Inputs data during x16 Data-Write operations. Outputs array, buffer or identifier data in the appropriate Read mode; not used for Status register reads. Floated when the chip is de-selected or the outputs are disabled.
CE_0#, CE_1#	INPUT	**CHIP ENABLE INPUTS:** Activate the device's control logic, input buffers, decoders and sense amplifiers. With either CE_0# or CE_1# high, the device is de-selected and power consumption reduces to Standby levels upon completion of any current Data-Write or Erase operations. Both CE_0#, CE_1# must be low to select the device. All timing specifications are the same for both signals. Device Selection occurs with the latter falling edge of CE_0# or CE_1#. The first rising edge of CE_0# or CE_1# disables the device.
RP#	INPUT	**RESET/POWER-DOWN:** With RP# low, the device is reset, any current operation is aborted and device is put into the deep power down mode. When the power is turned on, RP# pin is turned to low in order to return the device to default configuration. When the 3/5# pin is switched, or when the power transition is occurred, or at the power on/off, RP# is required to stay low in order to protect data from noise. When returning from Deep Power-Down, a recovery time of 400ns (Vcc=5.0V$\pm$0.25V) is required to allow these circuits to power-up. When RP# goes low, any current or pending WSM operation(s) are terminated, and the device is reset. All Status registers return to ready (with all status flags cleared). After returning, the device is in read array mode.
OE#	INPUT	**OUTPUT ENABLE:** Gates device data through the output buffers when low. The outputs float to tri-state off when OE# is high. **NOTE:** CE_X# overrides OE#, and OE# overrides WE#.
WE#	INPUT	**WRITE ENABLE:** Controls access to the CUI, Page Buffers, Data Queue Registers and Address Queue Latches. WE# is active low, and latches both address and data (command or array) on its rising edge.
RY/BY#	OPEN DRAIN OUTPUT	**READY/BUSY:** Indicates status of the internal WSM. When low, it indicates that the WSM is busy performing an operation. RY/BY# high indicates that the WSM is ready for new operations (or WSM has completed all pending operations), or Erase is Suspended, or the device is in deep power-down mode. This output is always active (i.e., not floated to tri-state off when OE# or CE_0#, CE_1# are high), except if a RY/BY# Pin Disable command is issued.

2.1 Lead Descriptions (Continued)

Symbol	Type	Name and Function
WP#	INPUT	WRITE PROTECT: Erase blocks can be locked by writing a non-volatile lock-bit for each block. When WP# is low, those locked blocks as reflected by the Block-Lock Status bits (BSR. 6), are protected from inadvertent Data Writes or Erases. When WP# is high, all blocks can be Written or Erased regardless of the state of the lock-bits. The WP# input buffer is disabled when RP# transitions low (deep power-down mode).
BYTE#	INPUT	**BYTE ENABLE:** BYTE# low places device in x8 mode. All data is then input or output on DQ_{0-7}, and DQ_{8-15} float. Address A_0 selects between the high and low byte. BYTE#high places the device in x16 mode, and turns off the A_0 input buffer. Address A_1, then becomes the lowest order address.
3/5#	INPUT	**3.3/5.0 VOLT SELECT:** 3/5# high configures internal circuits for 3.3V operation. 3/5# low configures internal circuits for 5.0V operation. **NOTES:** Reading the array with 3/5# high in a 5.0V system could damage the device. There is a significant delay from 3/5# switching to valid data.
V_{PP}	SUPPLY	**ERASE/WRITE POWER SUPPLY:** For erasing memory array blocks or writing words/bytes/pages into the flash array.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY (3.3V ±0.3V, 5.0V±0.5V):** Do not leave any power pins floating.
GND	SUPPLY	**GROUND FOR ALL INTERNAL CIRCUITRY:** Do not leave any ground pins floating.
NC		**NO CONNECT:** No internal connection to die, lead may be driven or left floating.



NOTE:
56-LEAD SSOP Mechanical Diagrams and Dimensions are shown at the end of this specificaion

Figure 2. SSOP Configuration

3.0 MEMORY MAPS

1FFFFFH	64 KByte Block	31
1F0000H		
1EFFFFH	64 KByte Block	30
1E0000H		
1DFFFFH	64 KByte Block	29
1D0000H		
1CFFFFH	64 KByte Block	28
1C0000H		
1BFFFFH	64 KByte Block	27
1B0000H		
1AFFFFH	64 KByte Block	26
1A0000H		
19FFFFH	64 KByte Block	25
190000H		
18FFFFH	64 KByte Block	24
180000H		
17FFFFH	64 KByte Block	23
170000H		
16FFFFH	64 KByte Block	22
160000H		
15FFFFH	64 KByte Block	21
150000H		
14FFFFH	64 KByte Block	20
140000H		
13FFFFH	64 KByte Block	19
130000H		
12FFFFH	64 KByte Block	18
120000H		
11FFFFH	64 KByte Block	17
110000H		
10FFFFH	64 KByte Block	16
100000H		
0FFFFFH	64 KByte Block	15
0F0000H		
0EFFFFH	64 KByte Block	14
0E0000H		
0DFFFFH	64 KByte Block	13
0D0000H		
0CFFFFH	64 KByte Block	12
0C0000H		
0BFFFFH	64 KByte Block	11
0B0000H		
0AFFFFH	64 KByte Block	10
0A0000H		
09FFFFH	64 KByte Block	9
090000H		
08FFFFH	64 KByte Block	8
080000H		
07FFFFH	64 KByte Block	7
070000H		
06FFFFH	64 KByte Block	6
060000H		
05FFFFH	64 KByte Block	5
050000H		
04FFFFH	64 KByte Block	4
040000H		
03FFFFH	64 KByte Block	3
030000H		
02FFFFH	64 KByte Block	2
020000H		
01FFFFH	64 KByte Block	1
010000H		
00FFFFH	64 KByte Block	0
000000H		

Figure 3. LH28F016SANS-70 Memory Map (Byte-wide mode)

3.1 Extended Status Registers Memory Map

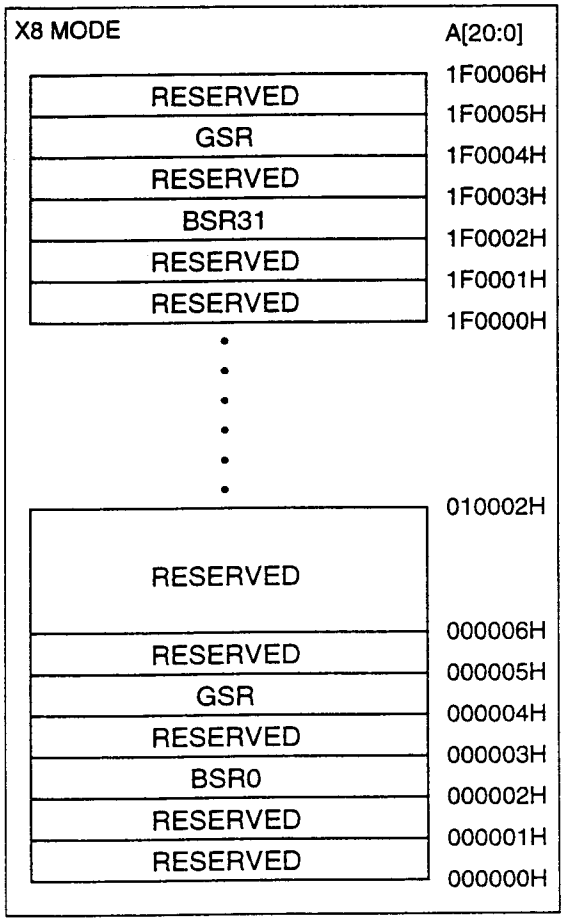


Figure 4.1 Extended Status Register Memory Map (Byte-wide mode)

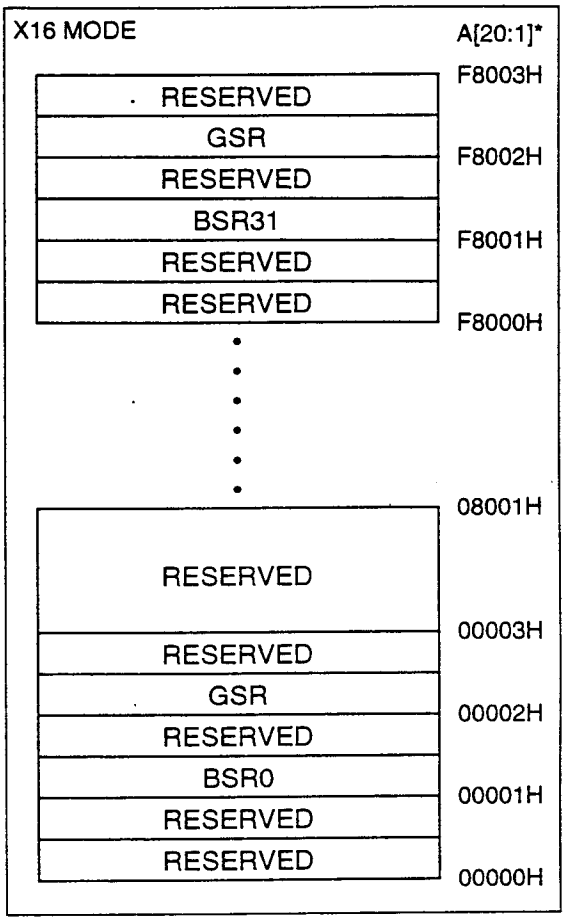


Figure 4.2 Extended Status Register Memory Map (Word-wide mode)

* In Word-wide mode A_0 don't care, address values are ignored A_0

4.0 BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS

4.1 Bus Operations for Word-Wide Mode (BYTE# = V_{IH})

Mode	Notes	RP#	CE_1#	CE_0#	OE#	WE#	A_1	DQ_{0-15}	RY/BY#
Read	1,2,7	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X
Output Disable	1,6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	High Z	X
Standby	1,6,7	V_{IH}	V_{IL} V_{IH} V_{IH}	V_{IH} V_{IL} V_{IH}	X	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Manufacturer ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	0089H	V_{OH}
Device ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	66A0H	V_{OH}
Write	1,5,6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X

4.2 Bus Operations For Byte-Wide Mode (BYTE# =V_{IL})

Mode	Notes	RP#	CE_1#	CE_0#	OE#	WE#	A_0	DQ_{0-7}	RY/BY#
Read	1,2,7	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X
Output Disable	1,6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	High Z	X
Standby	1,6,7	V_{IH}	V_{IL} V_{IH} V_{IH}	V_{IH} V_{IL} V_{IH}	X	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Manufacturer ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	89H	V_{OH}
Device ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A0H	V_{OH}
Write	1,5,6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X

NOTES:

1. X can be V_{IH} or V_{IL} for address or control pins except for RY/BY#, which is either V_{OL} or V_{OH}.
2. RY/BY# output is open drain. When the WSM is ready, Erase is suspended or the device is in deep power-down mode, RY/BY# will be at V_{OH} if it is tied to V_{CC} through a resistor. When the RY/BY# at V_{OH} is independent of OE# while a WSM operation is in progress.
3. RP# at GND ± 0.2V ensures the lowest deep power-down current.
4. A_0 and A_1 at V_{IL} provide manufacturer ID codes in x8 and x16 modes respectively.
   A_0 and A_1 at V_{IH} provide device ID codes in x8 and x16 modes respectively. All other addresses are set to zero.
5. Commands for different Erase operations, Data Write operations of Lock-Block operations can only be successfully completed when $V_{PP} = V_{PPH}$.
6. While the WSM is running, RY/BY# in Level-Mode (default) stays at V_{OL} until all operations are complete. RY/BY# goes to V_{OH} when the WSM is not busy or in erase suspend mode.
7. RY/BY# may be at V_{OL} while the WSM is busy performing various operations. For example, a status register read during a write operation.

4.3 LH28F008SA-Compatible Mode Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH	Read	AA	AD
Intelligent Identifier	1	Write	X	90H	Read	IA	ID
Read Compatible Status Register	2	Write	X	70H	Read	X	CSRD
Clear Status Register	3	Write	X	50H			
Word/Byte Write		Write	X	40H	Write	WA	WD
Alternate Word/Byte Write		Write	X	10H	Write	WA	WD
Block Erase/Confirm	4	Write	X	20H	Write	BA	D0H
Erase Suspend/Resume	4	Write	X	B0H	Write	X	D0H

ADDRESS
AA = Array Address
BA = Block Address
IA = Identifier Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
CSRD = CSR Data
ID = Identifier Data
WD = Write Data

NOTES:
1. Following the intelligent identifier command, two Read operations access the manufacturer and device signature codes.
2. The CSR is automatically available after device enters Data Write, Erase, or Suspend operations.
3. Clears CSR.3, CSR.4 and CSR.5. Also clears GSR.5 and all BSR.5 and BSR.2 bits.
See Status register definitions.
4. While device performs Block Erase, if you issue Erase Suspend Command (B0H), be sure to confirm ESS (Erase-Suspend-Status) is set to 1 on compatible status register. In the case, ESS bit was not set to 1, also completed the Erase (ESS=0, WSMS=1), be sure to issue Resume command (D0H) after completed next Erase command. Beside, when the Erase Suspend command is issued, while the device is not in Erase, be sure to issue Resume command (D0H) after the next erase completed. When you use Erase-Suspend /Resume command, we recommend to issue serial Block Erase command (20H, D0H) and Resume command (D0H). (Refer to 4.4 Performance Enhancement Command Bus Definitions.)

4.4 LH28F016SANS-70 -Performance Enhancement Command Bus Definitions

Command	Mode	Notes	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
			Oper	Addr	Data	Oper	Addr	Data	Oper	Addr	Data
Read Extended Status Register		1	Write	X	71H	Read	RA	GSRD BSRD			
Page Buffer Swap		7	Write	X	72H						
Read Page Buffer			Write	X	75H	Read	PA	PD			
Single Load to Page Buffer			Write	X	74H	Write	PA	PD			
Sequential Load to Page Buffer	x8	4,6,10	Write	X	E0H	Write	X	BCL	Write	X	BCH
	x16	4,5,6,10	Write	X	E0H	Write	X	WCL	Write	X	WCH
Page Buffer Write to Flash	x8	3,4,9,10	Write	X	0CH	Write	A0	BC(L,H)	Write	WA	BC(H,L)
	x16	4,5,10	Write	X	0CH	Write	X	WCL	Write	WA	WCH
Two-Byte Write	x8	3	Write	X	FBH	Write	A0	WD(L,H)	Write	WA	WD(H,L)
Block Erase /Confirm		11	Write	X	20H	Write	BA	D0H	Write	X	D0H
Lock Block /Confirm			Write	X	77H	Write	BA	D0H			
Upload Status Bits /Confirm		2	Write	X	97H	Write	X	D0H			
Upload Device Information			Write	X	99H	Write	X	D0H			
Erase All Unlocked Blocks/Confirm		11	Write	X	A7H	Write	X	D0H	Write	X	D0H
RY/BY# Enable to Level-Mode		8	Write	X	96H	Write	X	01H			
RY/BY# Pulse-On-Write		8	Write	X	96H	Write	X	02H			
RY/BY# Pulse-On-Erase		8	Write	X	96H	Write	X	03H			
RY/BY# Disable		8	Write	X	96H	Write	X	04H			
Sleep			Write	X	F0H						
Abort			Write	X	80H						

ADDRESS
BA = Block Address
PA = Page Buffer Address
RA = Extended Register Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
PD = Page Buffer Data
BSRD = BSR Data
GSRD = GSR Data

WC (L.H) = Word Count (Low, High)
BC (L.H) = Byte Count (Low, High)
WD (L.H) = Write Data (Low, High)

NOTES:
1. RA can be the GSR address or any BSR address. See Figure 4.1 and 4.2 for Extended Status Register Memory Maps.
2. Upon device power-up, all BSR lock-bits come up locked. The Upload Status Bits command must be written to reflect the actual lock-bit status.
3. A_0 is automatically complemented to load second byte of data. BYTE# must be at V_{IL}.
A_0 value determines which WD/BC is supplied first: A_0 = 0 looks at the WDL/BCL, A_0 = 1 looks at the WDH/BCH.
4. BCH/WCH must be at 00H for this product because of the 256-Byte (128 Word) Page Buffer size and to avoid writing the Page Buffer contents into more than one 256-Byte segment within an array block. They are simply shown for future Page Buffer expandability.
5. In x16 mode, only the lower byte DQ_{0-7} is used for WCL and WCH. The upper byte DQ_{8-15} is a don't care.
6. PA and PD (Whose count is given in cycles 2 and 3) are supplied starting in the 4th cycle which is not shown.
7. This command allows the user to swap between available Page Buffers (0 or 1).
8. These commands reconfigure RY/BY# output to one of two pulse-modes or enable and disable the RY/BY# function.
9. Write address, WA, is the Destination address in the flash array which must match the Source address in the Page Buffer. Refer to the LH28F800SU User's Manual.
10. BCL = 00H corresponds to a Byte count of 1. Similarly, WCL = 00H corresponds to a Word count of 1.
11. Unless you issue Erase-Suspend command, It is no necessary to input DOH on third bus cycle.

4.5 Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

CSR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
0 = Busy

CSR.6 = ERASE-SUSPEND STATUS (ESS)
1 = Erase Suspended
0 = Erase in Progress/Completed

CSR.5 = ERASE STATUS (ES)
1 = Error in Block Erasure
0 = Successful Block Erase

CSR.4 = DATA-WRITE STATUS (DWS)
1 = Error in Data Write
0 = Data Write Successful

CSR.3 = V_{PP} STATUS (VPPS)
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

NOTES:

RY/BY# output or WSMS bit must be checked to determine completion of an operation (Erase Suspend, Erase or Data Write) before the appropriate Status bit (ESS, ES or DWS) is checked for success.

If DWS and ES are set to "1" during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.

The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP}'s level only after the Data-Write or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

CSR.2-0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use: mask them out when polling the CSR.

4.6 Global Status Register

WSMS	OSS	DOS	DSS	QS	PBAS	PBS	PBSS
7	6	5	4	3	2	1	0

GSR.7 = WRITE STATE MACHINE STATUS (WSMS)
- 1 = Ready
- 0 = Busy

GSR.6 = OPERATION SUSPEND STATUS (OSS)
- 1 = Operation Suspended
- 0 = Operation in Progress/Completed

GSR.5 = DEVICE OPERATION STATUS (DOS)
- 1 = Operation Unsuccessful
- 0 = Operation Successful or Currently Running

GSR.4 = DEVICE SLEEP STATUS (DSS)
- 1 = Device in Sleep
- 0 = Device Not in Sleep

MATRIX 5/4
- 00 = Operation Successful or Currently Running — If operation currently running, then GSR.7 = 0.
- 01 = Device in Sleep Mode or Pending Sleep — If device pending sleep, then GSR.7 = 0.
- 10 = Operation Unsuccessful
- 11 = Operation Unsuccessful or Aborted — Operation aborted: Unsuccessful due to Abort command.

GSR.3 = QUEUE STATUS (QS)
- 1 = Queue Full
- 0 = Queue Available

GSR.2 = PAGE BUFFER AVAILABLE STATUS (PBAS)
- 1 = One or Two Page Buffers Available — The device contains two Page Buffers.
- 0 = No Page Buffer Available

GSR.1 = PAGE BUFFER STATUS (PBS)
- 1 = Selected Page Buffer Ready
- 0 = Selected Page Buffer Busy — Selected Page Buffer is currently busy with WSM operation.

GSR.0 = PAGE BUFFER SELECT STATUS (PBSS)
- 1 = Page Buffer 1 Selected
- 0 = Page Buffer 0 Selected

NOTES:

[1] RY/BY# output or WSMS bit must be checked to determine completion of an operation (Block Lock, Suspend, any RY/BY# reconfiguration, Upload Status Bits, Erase or Data Write) before the appropriate Status bit (OSS or DOS) is checked for success.

NOTE:

1. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.

4.7 Block Status Register

BS	BLS	BOS	BOAS	QS	VPPS	R	R
7	6	5	4	3	2	1	0

BSR.7 = BLOCK STATUS (BS)
1 = Ready
0 = Busy

BSR.6 = BLOCK-LOCK STATUS (BLS)
1 = Block Unlocked for Write/Erase
0 = Block Locked for Write/Erase

BSR.5 = BLOCK OPERATION STATUS (BOS)
1 = Operation Unsuccessful
0 = Operation Successful or
Currently Running

BSR.4 = BLOCK OPERATION ABORT STATUS (BOAS)
1 = Operation Aborted
0 = Operation Not Aborted

MATRIX 5/4
00 = Operation Successful or
Currently Running
01 = Not a valid Combination
10 = Operation Unsuccessful
11 = Operation Aborted

BSR.3 = QUEUE STATUS (QS)
1 = Queue Full
0 = Queue Available

BSR.2 = V_{PP} STATUS (VPPS)
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

NOTES:
[1] RY/BY# output or BS bit must be checked to determine completion of an operation (Block Lock, Suspend, Erase or Data Write) before the appropriate Status bits (BOS, BLS) is checked for success.

The BOAS bit will not be set until BSR.7 = 1.

Operation halted via Abort command.

NOTES:
BSR.1-0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use; mask them out when polling the BSRs.
1. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.

5.0 ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to + 80°C
Storage Temperature ..... - 65°C to + 125°C

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

V_{CC} = 3.3V ± 0.3V Systems[4]

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
T_A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V_{CC}	V_{CC} with Respect to GND	2	- 0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	2	- 0.2	14.0	V	
V	Voltage on any Pin (except V_{CC}, V_{PP}) with Respect to GND	2	- 0.5	V_{CC} + 0.5	V	
I	Current into any Non-Supply Pin			± 30	mA	
I_{OUT}	Output Short Circuit Current	3		100	mA	

V_{CC} = 5.0V ± 0.5V Systems[4]

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
T_A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V_{CC}	V_{CC} with Respect to GND	2	- 0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	2	- 0.2	14.0	V	
V	Voltage on any Pin (except V_{CC}, V_{PP}) with Respect to GND	2	- 0.5	7.0	V	
I	Current into any Non-Supply Pin			± 30	mA	
I_{OUT}	Output Short Circuit Current	3		100	mA	

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is - 0.5V on input/output pins. During transitions, this level may undershoot to - 2.0V for periods < 20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. AC specifications are valid at both voltage ranges. See DC Characteristics tables for voltage range-specific specifications.

5.2 Capacitance

For a 3.3V System:

Symbol	Parameter	Note	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T_A = 25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	8	12	pF	T_A = 25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1		50	pF	For V_{CC} = 3.3V ± 0.3V
	Equivalent Testing Load Circuit			2.5	ns	50Ω transmission line delay

For a 5.0V System:

Symbol	Parameter	Note	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T_A = 25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	8	12	pF	T_A = 25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1		100	pF	For V_{CC} = 5.0V ± 0.5V
				30	pF	For V_{CC} = 5.0V ± 0.25V
	Equivalent Testing Load Circuit V_{CC} ±10%			2.5	ns	25Ω transmission line delay
	Equivalent Testing Load Circuit V_{CC} ±5%			2.5	ns	83Ω transmission line delay

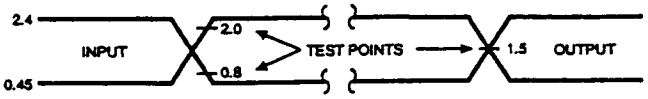
NOTE:
1. Sampled, not 100% tested.

5.3 Timing Nomenclature

All 3.3V system timings are measured from where signals cross 1.5V.
For 5.0V systems use the standard JEDEC cross point definitions.
Each timing parameter consists of 5 characters. Some common examples are defined below:

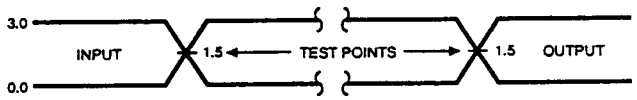
t_{CE} t_{ELQV} time(t) from CE# (E) going low (L) to the outputs (Q) becoming valid (V)
t_{OE} t_{GLQV} time(t) from OE# (G) going low (L) to the outputs (Q) becoming valid (V)
t_{ACC} t_{AVQV} time(t) from address (A) valid (V) to the outputs (Q) becoming valid (V)
t_{AS} t_{AVWH} time(t) from address (A) valid (V) to WE# (W) going high (H)
t_{DH} t_{WHDX} time(t) from WE# (W) going high (H) to when the data (D) can become undefined (X)

	Pin Characters		Pin States
A	Address Inputs	H	High
D	Data Inputs	L	Low
Q	Data Outputs	V	Valid
E	CE# (Chip Enable)	X	Driven, but not necessarily valid
G	OE# (Output Enable)	Z	High Impedance
W	WE# (Write Enable)		
P	RP# (Deep Power-Down Pin)		
R	RY/BY# (Ready/Busy#)		
V	Any Voltage Level		
Y	3/5# Pin		
5V	V_{CC} at 4.5V Minimum		
3V	V_{CC} at 3.0V Minimum		



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends, at 1.5V. Input rise and fall times (10% to 90%) < 10 ns.

Figure 5. Transient Input/Output Reference Waveform (V_{CC} = 5.0V)



AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) < 10 ns.

Figure 6. Transient Input/Output Reference Waveform (V_{CC} = 3.3V)

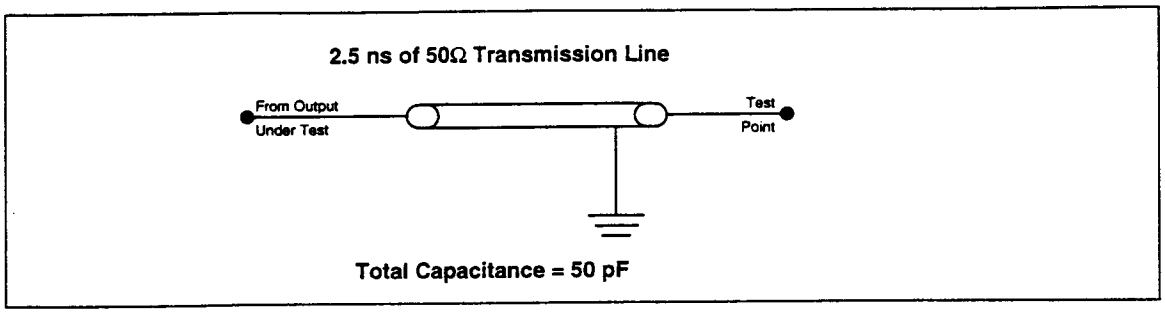


Figure 7. Transient Equivalent Testing Load Circuit (V_{CC} = 3.3V)

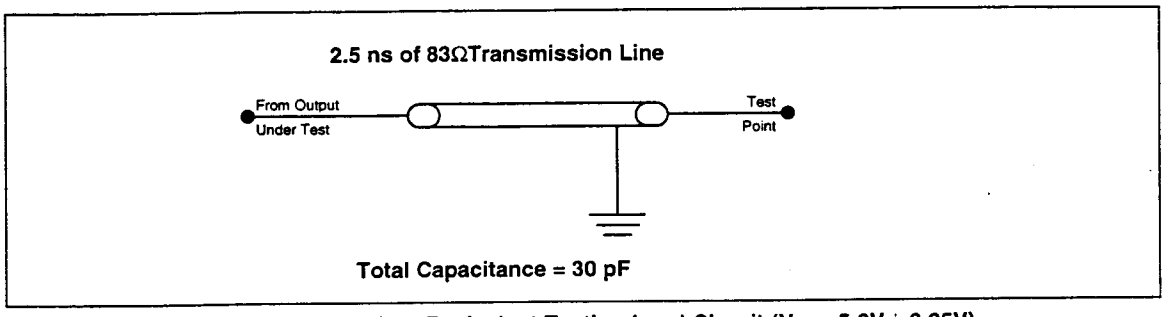


Figure 8(1). Transient Equivalent Testing Load Circuit (V_{CC} = 5.0V ± 0.25V)

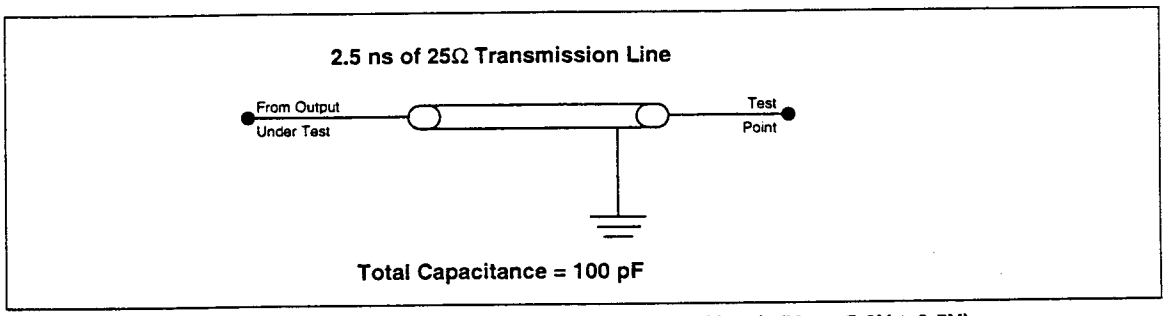


Figure 8(2). Transient Equivalent Testing Load Circuit (V_{CC} = 5.0V ± 0.5V)

5.4 DC Characteristics

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to + 70°C
3/5# = Pin Set High for 3.3V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Load Current	1			± 1	µA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1			± 10	µA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1,4		50	100	µA	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
				1	4	mA	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{IH} BYTE#, WP#, 3/5# = V_{IH} or V_{IL}
I_{CCD}	V_{CC} Deep Power-Down Current	1		1	5	µA	RP# = GND ± 0.2V
$I_{CCR}1$	V_{CC} Read Current	1,3,4		30	35	mA	V_{CC} = V_{CC} Max, CMOS: CE_0#, CE_1# = GND ± 0.2V BYTE# = GND ± 0.2V or V_{CC} ± 0.2V Inputs = GND ± 0.2V or V_{CC} ± 0.2V, TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or V_{IH} Inputs = V_{IL} or V_{IH}, f = 8 MHz, I_{OUT} = 0 mA
$I_{CCR}2$	V_{CC} Read Current	1,3,4		15	20	mA	V_{CC} = V_{CC} Max, CMOS: CE_0#, CE_1# = GND ± 0.2V, BYTE# = V_{CC} ± 0.2V or GND ± 0.2V Inputs = GND ± 0.2V or V_{CC} ± 0.2V, TTL: CE_0#, CE_1# = V_{IL} BYTE# = V_{IH} or V_{IL} Inputs = V_{IL} or V_{IH}, f = 4 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Write Current	1		8	12	mA	Word/Byte Write in Progress
I_{CCE}	V_{CC} Block Erase Current	1		6	12	mA	Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		3	6	mA	CE_0#, CE_1# =V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby Current	1		± 1	± 10	µA	V_{PP} ≤ V_{CC}
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.2	5	µA	RP# = GND ± 0.2V

DC Characteristics (Continued)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to + 70°C
3/5# = Pin Set High for 3.3V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{PPR}	V_{PP} Read Current	1			200	µA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Write Current	1		10	15	mA	$V_{PP} = V_{PPH}$, Word/Byte Write in Progress
I_{PPE}	V_{PP} Erase Current	1		4	10	mA	$V_{PP} = V_{PPH}$, Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1			200	µA	$V_{PP} = V_{PPH}$, Block Erase Suspended
V_{IL}	Input Low Voltage		- 0.3		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage				0.4	V	$V_{CC} = V_{CC}$ Min and I_{OL} = 4 mA
$V_{OH}1$	Output High Voltage		2.4			V	I_{OH} = - 2.0 mA $V_{CC} = V_{CC}$ Min
$V_{OH}2$			V_{CC} - 0.2			V	I_{OH} = - 100 µA $V_{CC} = V_{CC}$ Min
V_{PPL}	V_{PP} during Normal Operations	5	0.0		0.2	V	
			Vcc -0.2		6.5	V	
V_{PPH}	V_{PP} during Write/ Erase Operations		11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.0			V	

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 3.3V, V_{PP} = 5.0V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Automatic Power Saving (APS) reduces I_{CCR} to less than 1 mA in static operation.
4. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.
5. V_{PPL} in read is V_{CC}- 0.2V < V_{PPL} < 5.5V or GND < V_{PPL} < GND + 0.2V .

5.5 DC Characteristics

V_{CC} = 5.0V ± 0.5V, T_A = 0°C to + 70°C
3/5# Pin Set Low for 5V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Load Current	1			± 1	µA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1			± 10	µA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1,4		50	100	µA	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
				2	4	mA	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{IH} BYTE#, WP#, 3/5# = V_{IH} or V_{IL}
I_{CCD}	V_{CC} Deep Power-Down Current	1		1	5	µA	RP# = GND ± 0.2V
$I_{CCR}1$	V_{CC} Read Current	1,3,4		50	60	mA	V_{CC} = V_{CC} Max, CMOS: CE_0#, CE_1# = GND ± 0.2V BYTE# = GND ± 0.2V or V_{CC} ± 0.2V Inputs = GND ± 0.2V or V_{CC} ± 0.2V, TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or V_{IH} Inputs = V_{IL} or V_{IH}, f = 10 MHz, I_{OUT} = 0 mA
$I_{CCR}2$	V_{CC} Read Current	1,3,4		30	35	mA	V_{CC} = V_{CC} Max, CMOS: CE_0#, CE_1# = GND ± 0.2V, BYTE# = V_{CC} ± 0.2V or GND ± 0.2V Inputs = GND ± 0.2V or V_{CC} ± 0.2V, TTL: CE_0#, CE_1# = V_{IL} BYTE# = V_{IH} or V_{IL} Inputs = V_{IL} or V_{IH}, f = 5 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Write Current	1		25	35	mA	Word/Byte Write in Progress
I_{CCE}	V_{CC} Block Erase Current	1		18	25	mA	Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		5	10	mA	CE_0#, CE_1# =V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby Current	1			± 10	µA	V_{PP} ≤ V_{CC}
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.2	5	µA	RP# = GND ± 0.2V

DC Characteristics (Continued)

V_{CC} = 5.0V ± 0.5V, T_A = 0°C to + 70°C
3/5# Pin Set Low for 5V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{PPR}	V_{PP} Read Current	1		65	200	µA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Write Current	1		7	12	mA	$V_{PP} = V_{PPH}$, Word/Byte Write in Progress
I_{PPE}	V_{PP} Erase Current	1		5	10	mA	$V_{PP} = V_{PPH}$, Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		65	200	µA	$V_{PP} = V_{PPH}$, Block Erase Suspended
V_{IL}	Input Low Voltage		- 0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	$V_{CC} = V_{CC}$ Min and I_{OL} = 5.8 mA
$V_{OH}1$	Output High Voltage		0.85 V_{CC}			V	I_{OH} = - 2.5 mA $V_{CC} = V_{CC}$ Min
$V_{OH}2$			V_{CC} - 0.4			V	I_{OH} = - 100 µA $V_{CC} = V_{CC}$ Min
V_{PPL}	V_{PP} during Normal Operations	5	0.0		0.2	V	
			Vcc -0.2		6.5	V	
V_{PPH}	V_{PP} during Write/ Erase Operations		11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.0			V	

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 5.0V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Automatic Power Saving (APS) reduces I_{CCR} to less than 2 mA in Static operation.
4. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.
5. V_{PPL} in read is V_{CC}- 0.2V < V_{PPL} < 5.5V or GND < V_{PPL} < GND + 0.2V .

5.6 AC Characteristics - Read Only Operations[1]

T_A =0°C to +70°C

Symbol	Parameter	Notes	Vcc=3.3V±0.3V		Units
			Min	Max	
t_{AVAV}	Read Cycle Time		120		ns
t_{AVEL}	Address Setup to CE# Going Low	3,4	10		ns
t_{AVGL}	Address Setup to OE# Going Low	3,4	0		ns
t_{AVQV}	Address to Output Delay			120	ns
t_{ELQV}	CE# to Output Delay	2		120	ns
t_{PHQV}	RP# High to Output Delay			620	ns
t_{GLQV}	OE# to Output Delay	2		45	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# to Output in High Z	3		50	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# to Output in High Z	3		30	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		120	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		30	ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3		5	ns

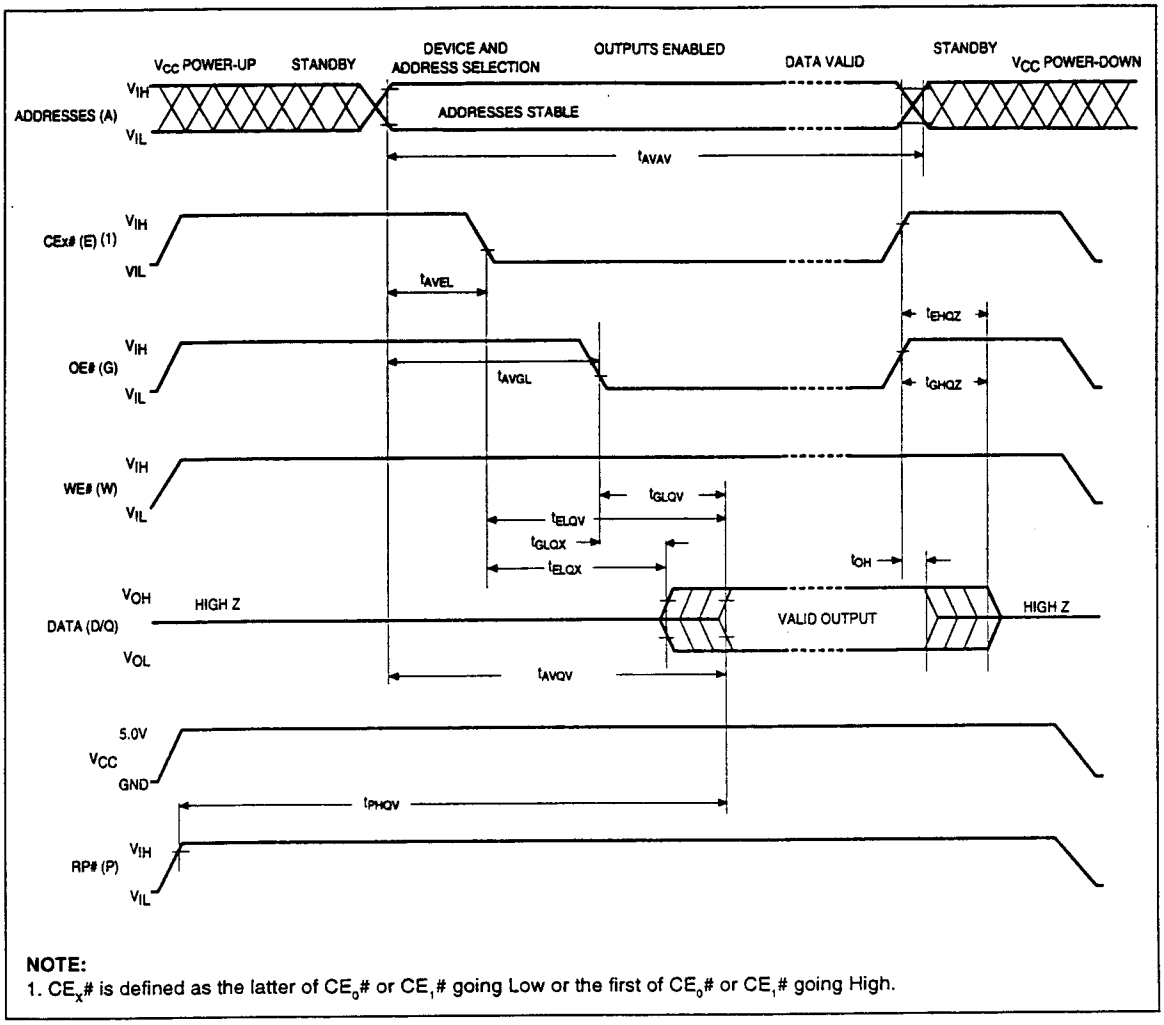
AC Characteristics - Read Only Operations[1] (Continued)

T_A =0°C to +70°C

Symbol	Parameter	Notes	Vcc=5.0V±0.25V		Vcc=5.0V±0.5V		Units
			Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time		70		80		ns
t_{AVEL}	Address Setup to CE# Going Low	3,4	10		10		ns
t_{AVGL}	Address Setup to OE# Going Low	3,4	0		0		ns
t_{AVQV}	Address to Output Delay			70		80	ns
t_{ELQV}	CE# to Output Delay	2		70		80	ns
t_{PHQV}	RP# High to Output Delay			400		480	ns
t_{GLQV}	OE# to Output Delay	2		30		35	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		ns
t_{EHQZ}	CE# to Output in High Z	3		25		30	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		ns
t_{GHQZ}	OE# to Output in High Z	3		25		30	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		70		80	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		25		30	ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3		5		5	ns

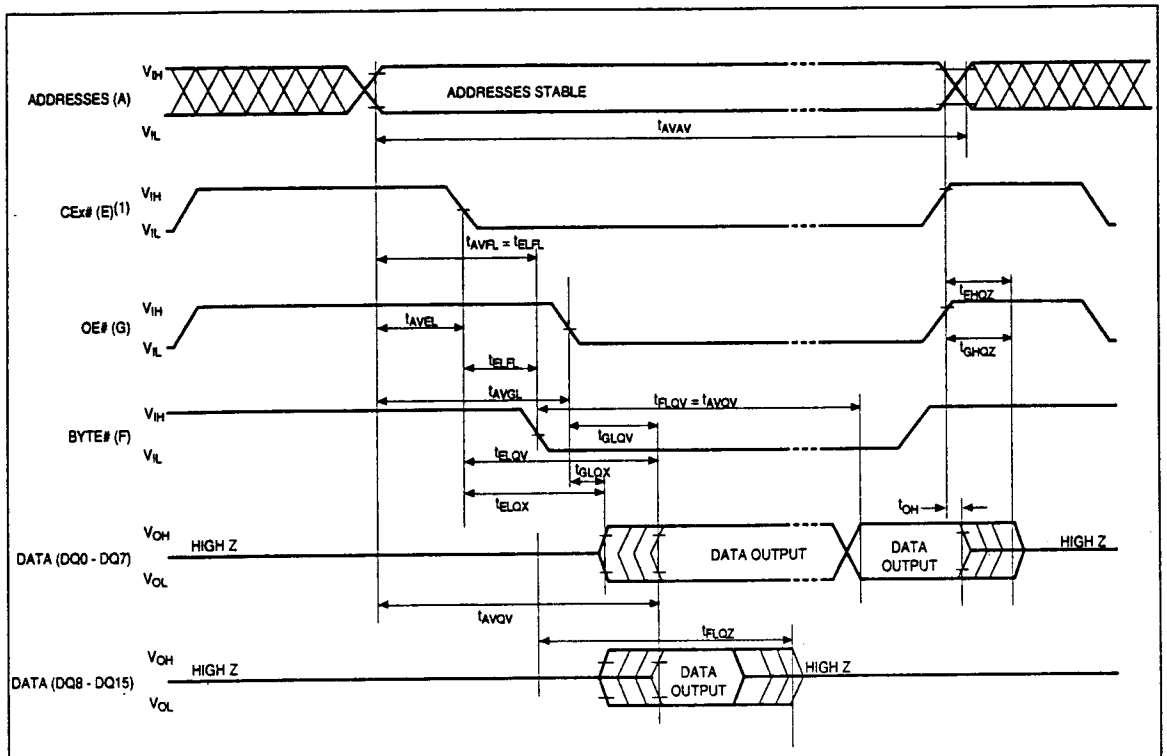
NOTES:

1. See AC Input/Output Reference Waveforms for timing measurements, Figures 5 and 6.
2. OE# may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. This timing parameter is used to latch the correct BSR data onto the outputs.



NOTE:
1. CE_x# is defined as the latter of CE_0# or CE_1# going Low or the first of CE_0# or CE_1# going High.

Figure 9. Read Timing Waveforms



NOTE:
1. CE_x# is defined as the latter of CE_0# or CE_1# going Low or the first of CE_0# or CE_1# going High.

Figure 10. BYTE# Timing Waveforms

5.7 Power-Up and Reset Timings

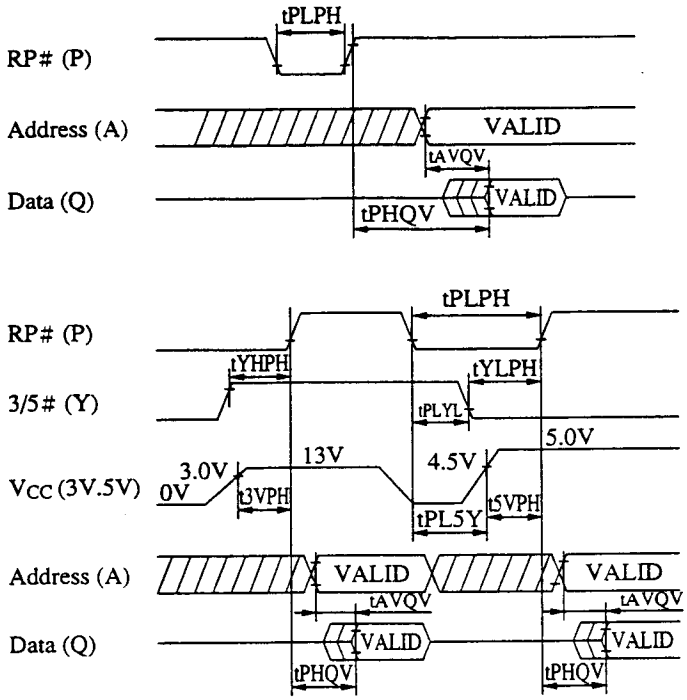


Figure 11. V_{CC} Power-Up and RP# Reset Waveforms

Symbol	Parameter	Note	Min.	Max.	Unit
t_{PLYL} t_{PLYH}	RP# Low to 3/5# Low (High)		0		µs
t_{YLPH} t_{YHPH}	3/5# Low (High) to RP# High	1	2		µs
t_{PL5V} t_{PL3V}	RP# Low to V_{CC} at 4.5V Minimum (to V_{CC} at 3.0V min or 3.6V max.)	2	0		µs
t_{PLPH}	RP# Low Hold Time		100		ns
t_{5VPH}	V_{CC} at 4.5V to RP# High	3	100		ns
t_{3VPH}	V_{CC} at 3.0V to RP# High	3	100		ns
t_{AVQV}	Address Valid to Data Valid for V_{CC} = 5V±10%	4		80	ns
t_{PHQV}	RP# High to Data Valid for V_{CC} = 5V±10%	4		480	ns

NOTES:
CE_0#, CE_1# and OE# are switched low after Power-Up.
1. Minimum of 2µs is required to meet the specified tPHQV times.
2. The power supply may start to switch concurrently with RP# going Low. RP# is required to stay low, until V_{CC} stays at recommended operating voltage.
3. Th address access time and RP# high to data valid time are shown for 5V V_{CC} operation. Refer to the AC Characteristics Read Only Operations 3.3V V_{CC} operation and all other speed options.

5.8 AC Characteristics for WE# - Controlled Command Write Operations[1]

T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Vcc=3.3V±0.3V			Unit
			Min	Typ	Max	
t_{AVAV}	Write Cycle Time		120			ns
t_{VPWH}	V_{PP} Setup to WE# Going High	3	100			ns
t_{PHEL}	RP# Setup to CE# Going Low		480			ns
t_{ELWL}	CE# Setup to WE# Going Low		10			ns
t_{AVWH}	Address Setup to WE# Going High	2,6	75			ns
t_{DVWH}	Data Setup to WE# Going High	2,6	75			ns
t_{WLWH}	WE# Pulse Width		75			ns
t_{WHDX}	Data Hold from WE# High	2	10			ns
t_{WHAX}	Address Hold from WE# High	2	10			ns
t_{WHEH}	CE# Hold from WE# High		10			ns
t_{WHWL}	WE# Pulse Width High		45			ns
t_{GHWL}	Read Recovery before Write		0			ns
t_{WHRL}	WE# High to RY/BY# Going Low				100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			ns
t_{PHWL}	RP# High Recovery to WE# Going Low		1			µs
t_{WHGL}	Write Recovery before Read		95			ns
t_{QVVL}	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			µs
t_{WHQV1}	Duration of Word/Byte Write Operation	4,5	5	9		µs
t_{WHQV2}	Duration of Block Erase Operation	4	0.3			s

AC Characteristics for WE# - Controlled Command Write Operations[1] (Continued)

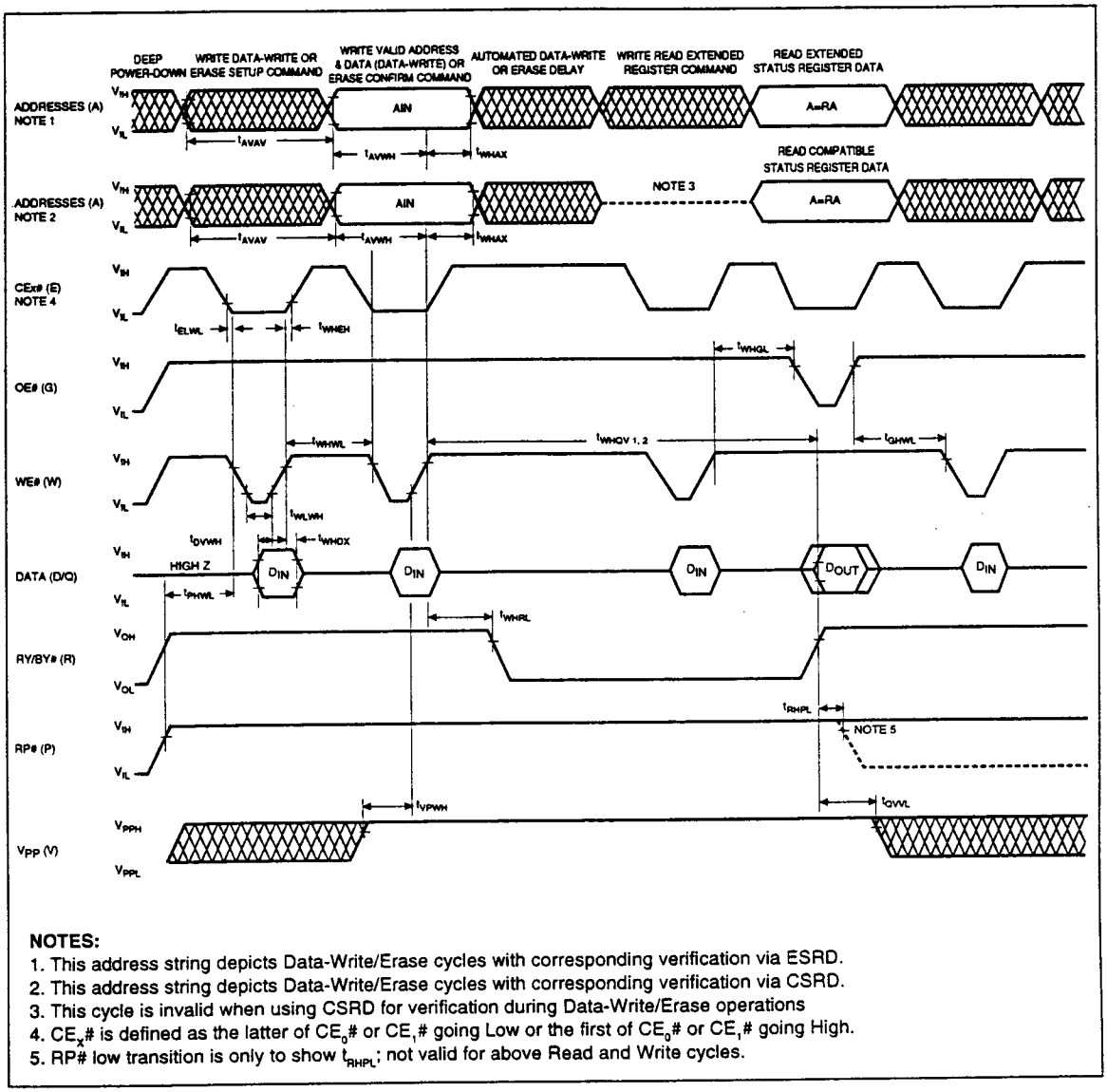
T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Vcc=5.0V±0.25V			Vcc=5.0V±0.5V			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{AVAV}	Write Cycle Time		70			80			ns
t_{VPWH}	V_{PP} Setup to WE# Going High	3	100			100			ns
t_{PHEL}	RP# Setup to CE# Going Low		480			480			ns
t_{ELWL}	CE# Setup to WE# Going Low		0			0			ns
t_{AVWH}	Address Setup to WE# Going High	2,6	50			50			ns
t_{DVWH}	Data Setup to WE# Going High	2,6	50			50			ns
t_{WLWH}	WE# Pulse Width		40			50			ns
t_{WHDX}	Data Hold from WE# High	2	0			0			ns
t_{WHAX}	Address Hold from WE# High	2	10			10			ns
t_{WHEH}	CE# Hold from WE# High		10			10			ns
t_{WHWL}	WE# Pulse Width High		30			30			ns
t_{GHWL}	Read Recovery before Write		0			0			ns
t_{WHRL}	WE# High to RY/BY# Going Low				100			100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			ns
t_{PHWL}	RP# High Recovery to WE# Going Low		1			1			µs
t_{WHGL}	Write Recovery before Read		60			65			ns
t_{QVVL}	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			0			µs
t_{WHQV1}	Duration of Word/Byte Write Operation	4,5	4.5	6		4.5	6		µs
t_{WHQV2}	Duration of Block Erase Operation	4	0.3			0.3			s

NOTES:

CE# is defined as the latter of CE_0# or CE_1# going Low or the first of CE_0# or CE_1# going High.

1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Word/Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of WE# for all Command Write operations.



NOTES:
1. This address string depicts Data-Write/Erase cycles with corresponding verification via ESRD.
2. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations
4. CE_x# is defined as the latter of CE_0# or CE_1# going Low or the first of CE_0# or CE_1# going High.
5. RP# low transition is only to show t_{RHPL}; not valid for above Read and Write cycles.

Figure 12. AC Waveforms for Command Write Operations

5.9 AC Characteristics for CE# - Controlled Command Write Operations[1]

T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Vcc=3.3V±0.3V			Unit
			Min	Typ	Max	
t_{AVAV}	Write Cycle Time		120			ns
t_{PHWL}	RP# Setup to WE# Going Low	3	480			ns
t_{VPEH}	V_{PP} Setup to CE# Going High	3	100			ns
t_{WLEL}	WE# Setup to CE# Going Low		0			ns
t_{AVEH}	Address Setup to CE# Going High	2,6	75			ns
t_{DVEH}	Data Setup to CE# Going High	2,6	75			ns
t_{ELEH}	CE# Pulse Width		75			ns
t_{EHDX}	Data Hold from CE# High	2	10			ns
t_{EHAX}	Address Hold from CE# High	2	10			ns
t_{EHWH}	WE# Hold from CE# High		10			ns
t_{EHEL}	CE# Pulse Width High		45			ns
t_{GHEL}	Read Recovery before Write		0			ns
t_{EHRL}	CE# High to RY/BY# Going Low				100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			ns
t_{PHEL}	RP# High Recovery to CE# Going Low		1			µs
t_{EHGL}	Write Recovery before Read		95			ns
t_{QVVL}	VPP Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			µs
t_{EHQV1}	Duration of Word/Byte Write Operation	4,5	5	9		µs
t_{EHQV2}	Duration of Block Erase Operation	4	0.3			s

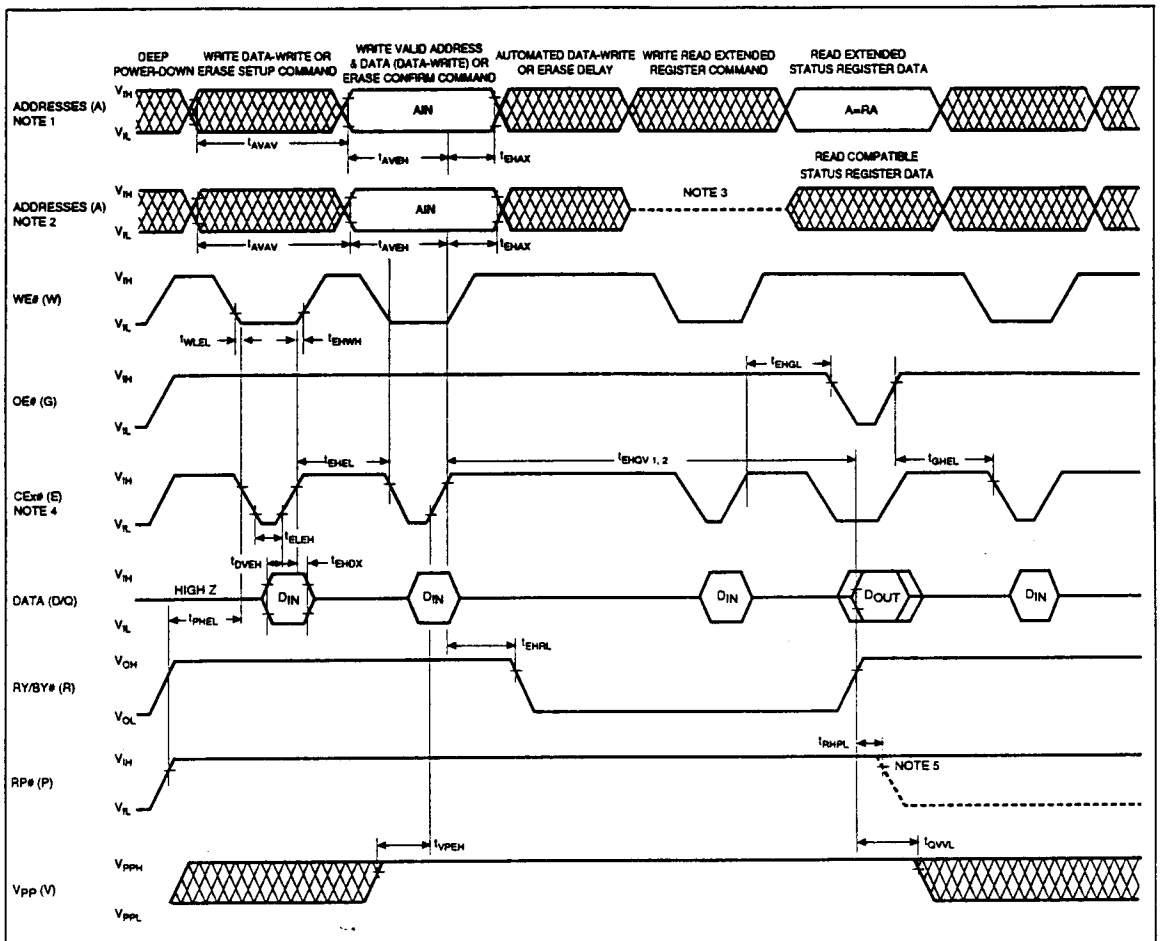
AC Characteristics for CE# - Controlled Command Write Operations[1] (Continued)

T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Vcc=5.0V±0.25V			Vcc=5.0V±0.5V			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{AVAV}	Write Cycle Time		70			80			ns
t_{PHWL}	RP# Setup to WE# Going Low		480			480			ns
t_{VPEH}	V_{PP} Setup to CE# Going High	3	100			100			ns
t_{WLEL}	WE# Setup to CE# Going Low		0			0			ns
t_{AVEH}	Address Setup to CE# Going High	2,6	50			50			ns
t_{DVEH}	Data Setup to CE# Going High	2,6	50			50			ns
t_{ELEH}	CE# Pulse Width		40			50			ns
t_{EHDX}	Data Hold from CE# High	2	0			0			ns
t_{EHAX}	Address Hold from CE# High	2	10			10			ns
t_{EHWH}	WE# Hold from CE# High		10			10			ns
t_{EHEL}	CE# Pulse Width High		30			50			ns
t_{GHEL}	Read Recovery before Write		0			0			ns
t_{EHRL}	CE# High to RY/BY# Going Low				100			100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			ns
t_{PHEL}	RP# High Recovery to CE# Going Low		1			1			µs
t_{EHGL}	Write Recovery before Read		60			65			ns
t_{QVVL}	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			0			µs
t_{EHQV1}	Duration of Word/Byte Write Operation	4,5	4.5	8		4.5	8		µs
t_{EHQV2}	Duration of Block Erase Operation	4	0.3			0.3			s

NOTES:
CE# is defined as the latter of CE_0# or CE_1# going Low or the first of CE_0# or CE_1# going High.

1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Word/Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of CE# for all Command Write Operations.



NOTES:

1. This address string depicts Data-Write/Erase cycles with corresponding verification via ESRD.
2. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations
4. CE_x# is defined as the latter of CE_0# or CE_1# going Low or the first of CE_0# or CE_1# going High.
5. RP# low transition is only to show t_{RHPL}; not valid for above Read and Write cycles.

Figure 13. Alternate AC Waveforms for Command Write Operations

5.10 AC Characteristics for Page Buffer Write Operations[1]

T_A =0°C to + 70°C

Symbol	Parameter	Notes	Vcc=3.3V±0.3V			Unit
			Min	Typ	Max	
t_{AVAV}	Write Cycle Time		120			ns
t_{ELWL}	CE# Setup to WE# Going Low		10			ns
t_{AVWL}	Address Setup to WE# Going Low	3	0			ns
t_{DVWH}	Data Setup to WE# Going High	2	75			ns
t_{WLWH}	WE# Pulse Width		75			ns
t_{WHDX}	Data Hold from WE# High	2	10			ns
t_{WHAX}	Address Hold from WE# High	2	10			ns
t_{WHEH}	CE# Hold from WE# High		10			ns
t_{WHWL}	WE# Pulse Width High		45			ns
t_{GHWL}	Read Recovery before Write		0			ns
t_{WHGL}	Write Recovery before Read		95			ns

Symbol	Parameter	Notes	Vcc=5.0V±0.25V			Vcc=5.0V±0.5V			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{AVAV}	Write Cycle Time		70			80			ns
t_{ELWL}	CE# Setup to WE# Going Low		0			0			ns
t_{AVWL}	Address Setup to WE# Going Low	3	0			0			ns
t_{DVWH}	Data Setup to WE# Going High	2	50			50			ns
t_{WLWH}	WE# Pulse Width		40			50			ns
t_{WHDX}	Data Hold from WE# High	2	0			0			ns
t_{WHAX}	Address Hold from WE# High	2	10			10			ns
t_{WHEH}	CE# Hold from WE# High		10			10			ns
t_{WHWL}	WE# Pulse Width High		30			30			ns
t_{GHWL}	Read Recovery before Write		0			0			ns
t_{WHGL}	Write Recovery before Read		60			65			ns

NOTES:

CE# is defined as the latter of CE_0# or CE_1# going Low or the first of CE_0# or CE_1# going High.

1. These are WE#-controlled write timings, equivalent CE#-controlled write timings apply.
2. Sampled, but not 100% tested.
3. Address must be valid during the entire WE# Low pulse.

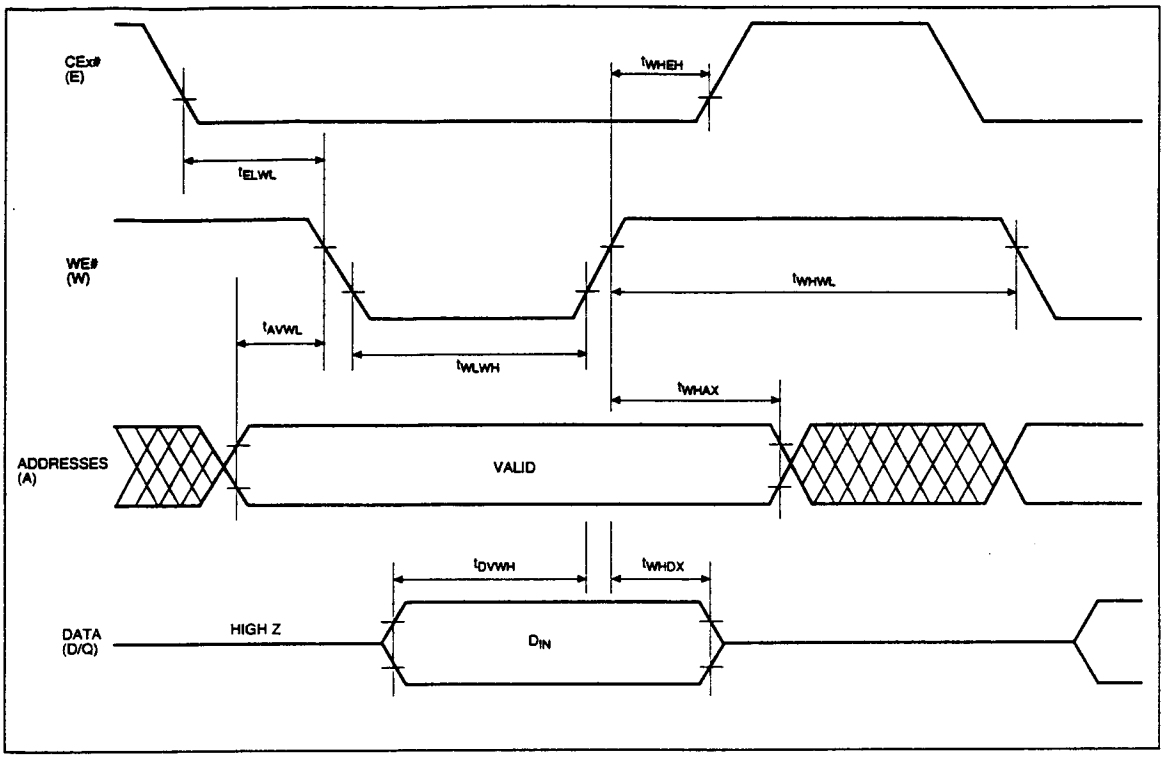


Figure 14. Page Buffer Write Timing Waveforms

5.11 Erase and Word/Byte Write Performance

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
$t_{WHRH}1$	Word/Byte Write Time	2		9		µs	
$t_{WHRH}2$	Block Write Time	2		0.6	2.1	s	Byte Write Mode
$t_{WHRH}3$	Block Write Time	2		0.3	1.0	s	Word Write Mode
	Block Erase Time	2		0.8	10	s	
	Full Chip Erase Time	2		25.6		s	

V_{CC} = 5.0V ± 0.5V, T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
$t_{WHRH}1$	Word/Byte Write Time	2		6		µs	
$t_{WHRH}2$	Block Write Time	2		0.4	2.1	s	Byte Write Mode
$t_{WHRH}3$	Block Write Time	2		0.2	1.0	s	Word Write Mode
	Block Erase Time	2		0.6	10	s	
	Full Chip Erase Time	2		19.2		s	

NOTES:
1. 25°C, V_{PP} = 5.0V.
2. Excludes System-Level Overhead.

Flash Memory, 16 Mbit, 56 SSOP, Flashfile, Symmetrically Block, LH28F016SANS-70