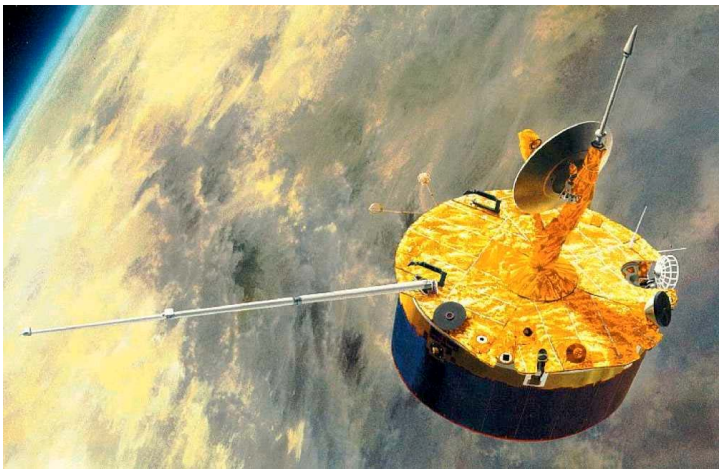


XE16BB10

Enhanced GPS Channel Correlator

1.
Features

- 8 GPS channels, 32 correlators
- Operating voltages:
  - VDDC (Core Power Supply Voltage): 1.6V – 2.0V
  - VDDR (RF IC Power Supply Voltage): 2.7V – 3.3V
- Ultra low power consumption
  - Core maximum current < 3.0mA at 1.8V
  - Four power control states
- Serial Interface:
  - UART: Full duplex asynchronous, 2.4k, up to 115.2k Bd

Ordering Information

Part	Temp. range	Pin-package
XE16BB10I11 (shipped only as part of the XE1610 kit)	-40 to 85°C	SO16NB

General Description

The XE16BB10 is part of the XE1610 chipset based on the advanced FirstGPS™ architecture. This enhanced GPS channel correlator is designed to receive and decode digital signals from the Colossus™ RF IC. The enhanced GPS correlator outputs GPS measurements (i.e pseudorange, carrier phase, Doppler etc.) to the "Navigation Platform" where these measurements are used to compute position, velocity and/or time solutions. The enhanced GPS 8 channel, 32 correlators design enables parallel tracking of the GPS L1 (1.575 GHz) frequency.

Applications

- Laptop computer
- PDA & Palmtop
- Leisure & Sports GPS receiver
- Asset management & tracking
- Automotive
- Cell phone

XEMICS SA • e-mail: info@xemics.com • web: www.xemics.com

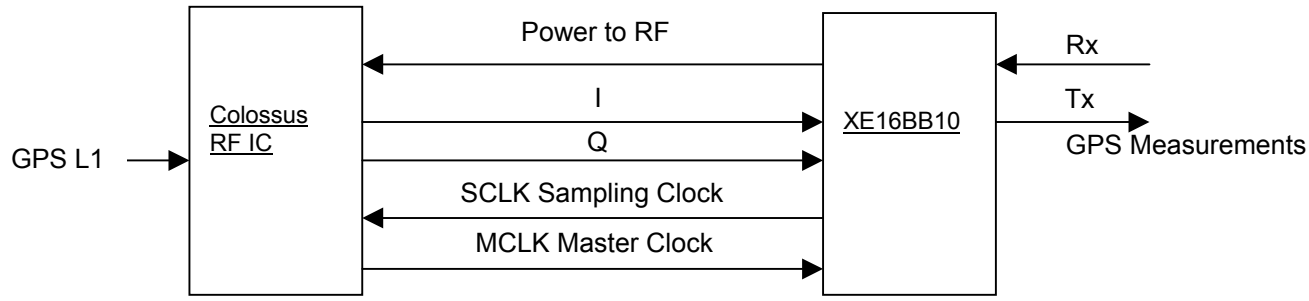
1. Functional Description

The XE16BB10 enhanced GPS channel correlator is designed to receive and decode digital signals from the Colossus RF IC. The enhanced GPS correlator outputs GPS measurements (i.e pseudorange, carrier phase, Doppler etc.) to the "Navigation Platform" where these measurements are used to compute position, velocity and/or time solutions. The enhanced GPS 8 channel, 32 correlators design enables parallel tracking of the GPS L1 (1.575 GHz) frequency.

2. Features

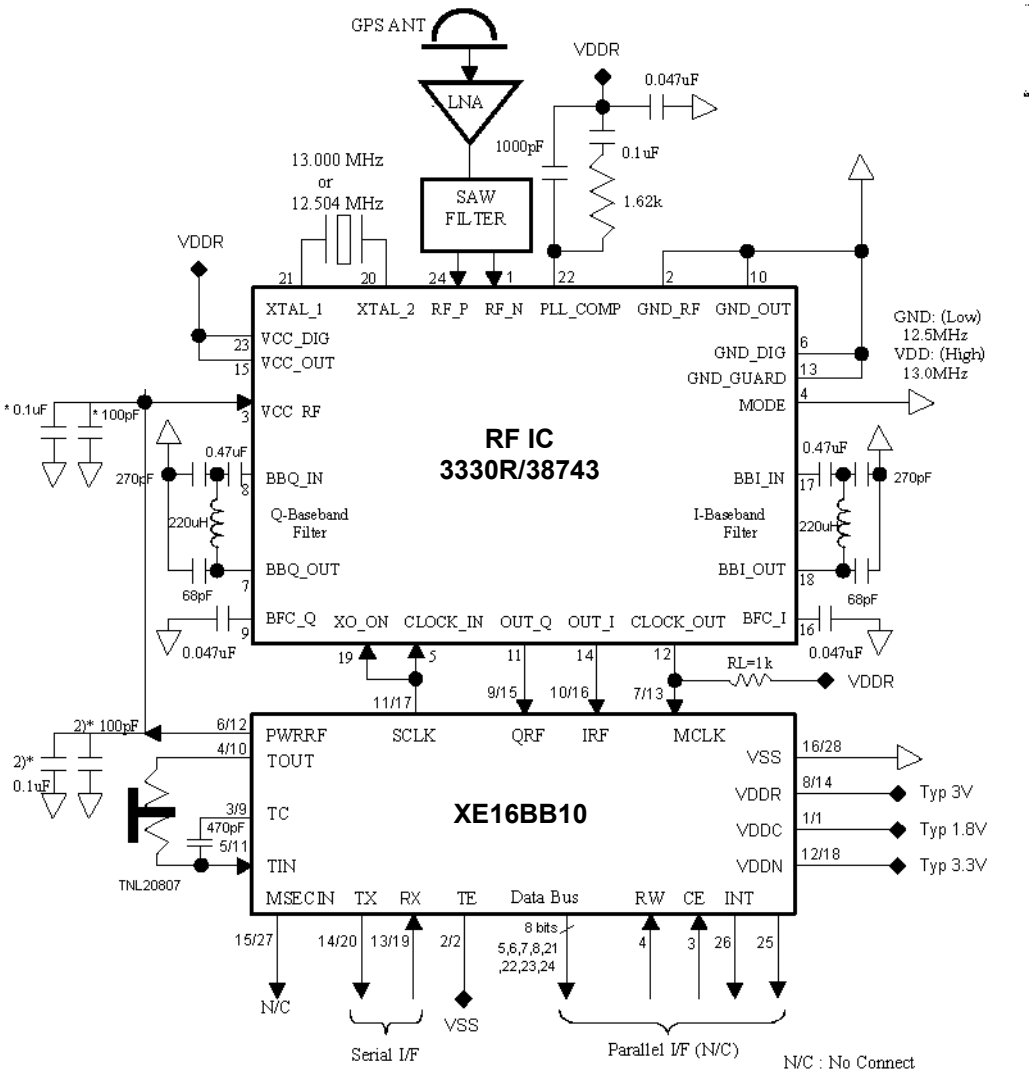
- 8 GPS channels that output GPS pseudorange, carrier phase and Doppler
- Operating voltages:
  - VDDC (Core Power Supply Voltage): 1.6V – 2.0V
  - VDDR (Colossus RF IC Power Supply Voltage): 2.7V – 3.3V
- Ultra low power consumption
  - Core maximum current < 3.0mA at 1.8V
  - Four power control states
- Serial Interface:
  - UART: Full duplex asynchronous channel with fixed data format of 8 data bits, 1 stop bit and odd parity bit
  - Speed (baud): 2.4k, 9.6k, 14.4k, 19.2k, 28.8k, 38.4k, 57.6k, 115.2k
- SO16NB package (Footprint: 9.9mm x 6.0mm: Pitch: 1.27mm)
- Extended operating temperature range: -40°C to 85°C

3. Architecture

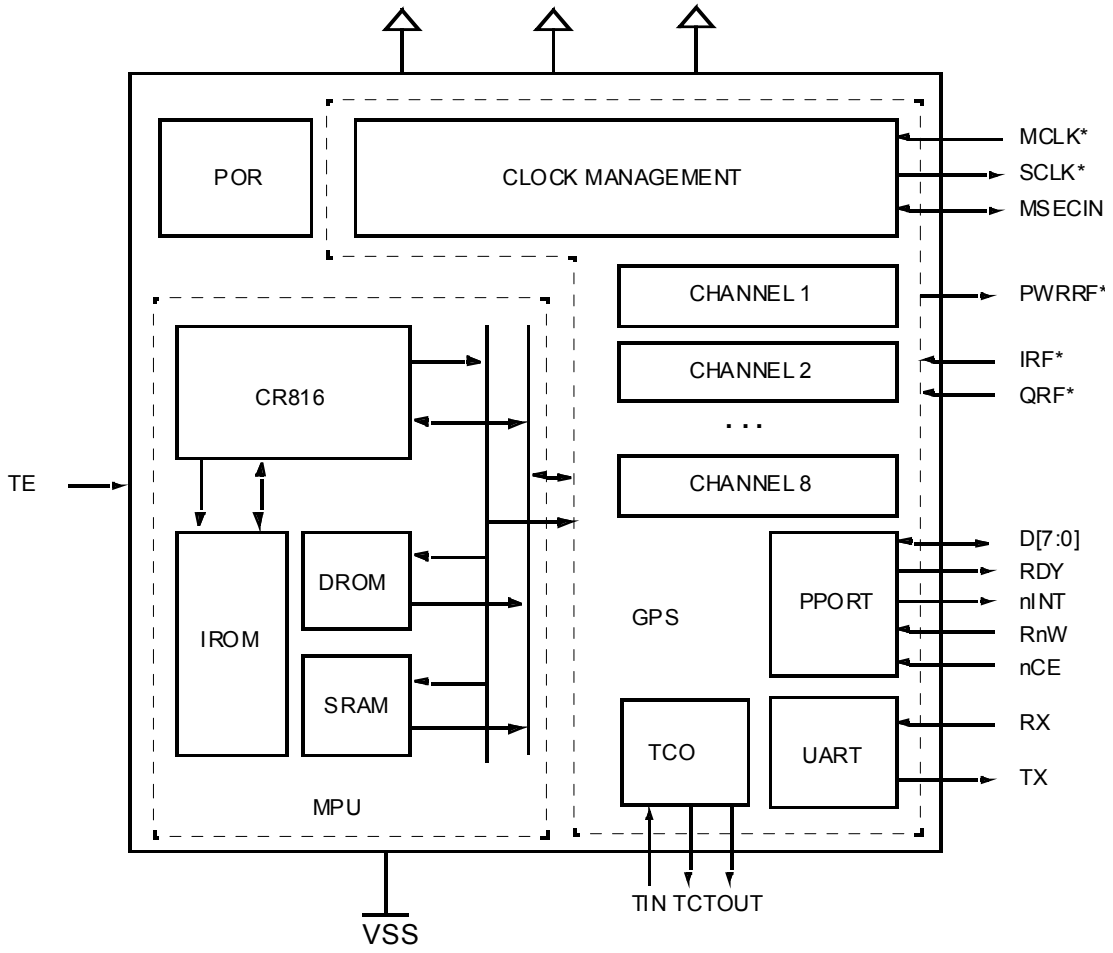


4. General Application

The enhanced channel correlator is the digital front-end part of a GPS receiver. It receives the digital signal from the Colossus RF front-end and decodes the data contained in this signal. The measurement outputs are available both on a parallel port and a serial port. Application information on the fine-tuning of the RF IC is available in its datasheet.



5. Block Diagram



The Channel correlator IC has its own embedded micro-controller: the CoolRISC™ 816 (CR816). The on-chip controller coordinates the various measurement functions and interfaces with the host system. The communication to the host system “navigation platform” takes place through a proprietary protocol but uses a standard RS232 link. Direct access to the CR816 micro-controller is not possible. The channel correlation functions are invoked through an API that is part of the navigation software running on the host processor.

6. Absolute Maximum Ratings and Storage Conditions

6.1 External Conditions

The power supplies for the chip need to be properly decoupled. This means that at least one external capacitor CDD must be connected between VSS and each of the positive supply (VDDx).

6.2 Absolute Maximum Ratings

Stresses above those listed in this clause may cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess to those given in the operating range section. Exposure to absolute maximum ratings for extended periods may affect device reliability

Parameter	Description	Min	Max	Unit
VDDC	core power supply voltage	VSS – 0.3	2.5	V
VDDN	navigation interface power supply voltage	VSS – 0.3	5.0	V
VDDR	RF front-end power supply voltage	VSS – 0.3	5.0	V
Tmr	Ambient temperature under bias	-40	+85	°C

6.3 Operating Range

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied. Total cumulative dwell time outside the normal power supply voltage range or the ambient temperature under bias, must be less than 0.1% of the useful life as defined.

Parameter	**Description**	**Min**	**Typ**	**Max**	**Unit**
VDDC	Core power supply voltage	1.6	1.8	2.0	V
VDDN	Navigation interface power supply voltage	3.0	3.3	3.6	V
VDDR	RF front end power supply voltage	2.7	3.0	3.3	V
VIHN	High level input voltage Navigation	2.1	-	VDDN	V
VILN	Low level input voltage Navigation	0	-	0.9	V
VIHR	High level input voltage RF	2.1	-	VDDR	V
VILR	Low level input voltage RF	0	-	0.9	V
VOHN	High level output voltage Navigation	2.4	-	VDDN	V
VOLN	Low level output voltage Navigation	0	-	0.4	V
VOHR	High level output voltage RF	2.4	-	VDDR	V
VOLR	Low level output voltage RF	0	-	0.4	V
I_{PWRRF}	Power RF current	-	-	6	mA
$I_{outN,\ source}$	Current source at VDDN supply (VOH= 2.4V)	-	-	4	mA

6.4 Operating Range continued

Parameter	Description	Min	Typ	Max	Unit
$I_{outN, sink}$	Current sink at VDDN supply (VOL=0.4V)	-	-	-4	mA
$I_{outR, source}$	Current source at VDDR supply (VOH=2.4V	-	-	3	mA
$I_{outR, sink}$	Current sink at VDDR supply (VOL=0.4V)	-	-	-3	mA
T_{amb}	Ambient temperature	-40	-	+85	°C
t_{rise}	Maximum input riding time from 10% to 90%	-	-	20	ns
t_{fall}	Maximum input falling time from 90% to 10%	-	-	20	ns
Cl_{sclk}	Load capacitance on SCLK output	-	10	20*	pF
Cl_{pp}	Load capacitance on parallel port outputs	-	15	40*	pF
Cl_{tx}	Load capacitance on Tx output	-	15	40*	pF
Cl_{tc}	Load capacitance on TC, TOUT	-	470	-	pF
Cl_{prwrf}	Load capacitance on PWRRF	-	100	-	pF
Cl_{other}	Load capacitance on other outputs	-	15	70*	pF

* Power consumption increases with capacitance values.

6.5 Current consumption

Typical current consumption for the core is reached under the following assumptions:

VDDC = 1.8V
Freq(SCLK) = 4.185 MHz
Freq(MCLK) = 12.504 MHz
Freq out (parallel port) < 14kWords/sec.
Freq CR816 = 3MHz

Maximum current under these assumptions: < 3.4mA

6.6 Storage conditions

* Temperature should be in the range –55°C to +110°C
* In case of IC deliveries not in dry bag, the conditions for a maximum storage period of two years are as follows :

Ambient Temperature (°C)	Relative humidity (%)
20	80
30	70
40	60
50	50

6.7 External Stress Immunity

Electrostatic discharges:
The device withstands 2000 volts Standardized Human Body Model ESD pulses when tested according to MIL883C method 3015.5 (pin combination 2).

Latch-up:
Static latch-up protection level is 300mA at 25°C when tested according to JEDEC no. 17.

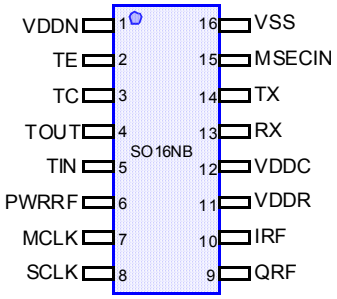
7. Packages and Pin-out

7.1 Available Packages

The circuit may be delivered as a 16-pin or 28-pin package. Part of the chip functionality is lost when the chip is enclosed in a 16-pin package.

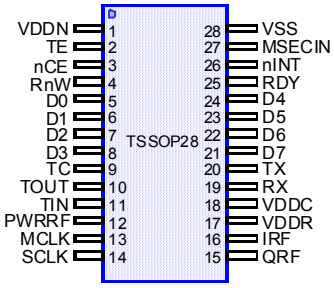
7.2

7.3 SO16NB



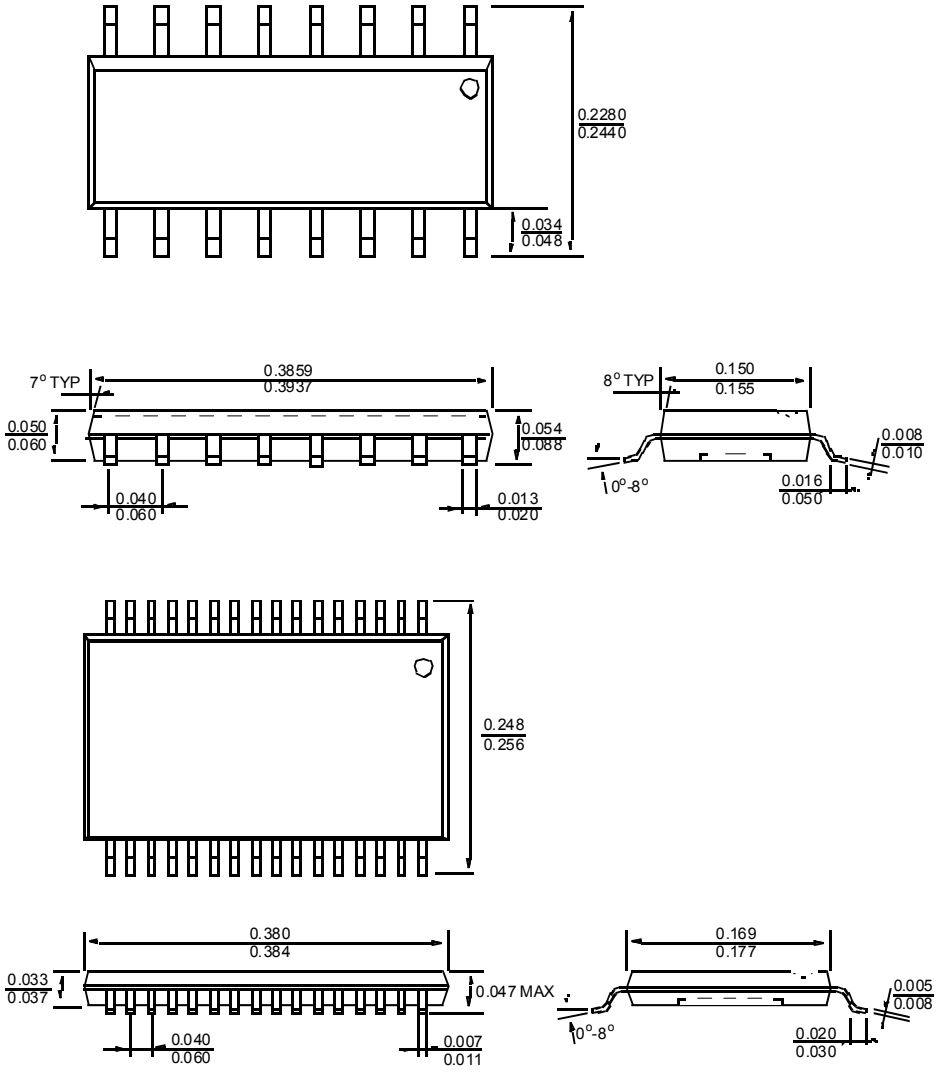
Pin No.	Pin Name	Description
1	VDDN	Power Supply for pads connected to the NAV platform
2	TE	Test Enable
3	TC	Temperature controlled oscillator compensation
4	TOUT	Temperature controlled oscillator square-wave output
5	TIN	Temperature controlled oscillator input from thermistor
6	PWRRF	Power to Colossus RF chip (digital circuit)
7	MCLK	Master clock input
8	SCLK	Sample clock
9	QRF	Incoming data, data changes with leading edge of SCLK
10	IRF	Incoming data, data changes with leading edge of SCLK
11	VDDR	Power to RF for Colossus RF chip
12	VDDC	Core power supply
13	RX	Receive input to UART
14	TX	Transmit output from UART
15	MSECIN	Synchronization for other IO
16	VSS	Ground

7.4 TSSOP28



Pin Nb	Pin Name	Description
1	VDDN	Power Supply for pads connected to the NAV platform
2	TE	Test Enable
3	nCE	Parallel port Chip Enable signal
4	RnW	Parallel port Read/Write signal
5	D0	Parallel port data bit 0
6	D1	Parallel port data bit 1
7	D2	Parallel port data bit 2
8	D3	Parallel port data bit 3
9	TC	Temperature controlled oscillator compensation
10	TOUT	Temperature controlled oscillator square-wave output
11	TIN	Temperature controlled oscillator input from thermistor
12	PWRRF	Power to Colossus RF chip (digital circuit)
13	MCLK	Master clock input
14	SCLK	Sample clock
15	QRF	Incoming data, data changes with leading edge of SCLK
16	IRF	Incoming data, data changes with leading edge of SCLK
17	VDDR	Power to RF for Colossus RF chip
18	VDDC	Core power supply
19	RX	Receive input to UART
20	TX	Transmit output from UART
21	D7	Parallel port data bit 7
22	D6	Parallel port data bit 6
23	D5	Parallel port data bit 5
24	D4	Parallel port data bit 4
25	RDY	Parallel port ready signal
26	nINT	Parallel port data bit interrupt signal
27	MSECIN	Synchronization for other IO
28	VSS	Ground

7.5 Mechanical drawings



.