1 PRODUCT OVERVIEW

OVERVIEW

The S3C72K8 singl-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM48 (Samsung Arrageable Microcontrollers). With a two-channel comparator, up-to-320-dot LCD direct drive capability, 8-bit timer/counter, watchdog timer and serial I/O, the S3C72K8 offers an excellent design solution for a wide variety of applications which require LCD functions.

Up to 27 pins of the 80-pin QFP package can be dedicated to I/O. Seven vectored interrupts provide fast response to internal and external events. In addition, the S3C72K8's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The S3C72K8 microcontroller is also available is OTP (one time programmable) version, S3P72K8. S3P72K8 microcontroller has an one-chop 8 Kbyte one time programmable EPROM instead of masked ROM. The S3P72K8 is comparable to S3C72K8, both in function and in pin configuration.

FEATURES

Memory

— 8 K × 8-bit RAM

— 1,024 × 4-bit ROM

27 I/O Pins

— Input only: 4 pins

— I/O: 15 pins

— Output: maximum 8 pins for 1-bit level output (sharing with segment driver outputs)

Comparator

— Two channel mode: internal reference (4-bit resolution)

— One channel mode: external reference

LCD Controller/Driver

— 40 segments and 8 common terminals

— 3, 4 and 8 common selectable

— Internal resistor circuit for LCD bias

— All dot can be switched on/off

8-Bit Basic Timer

— 4 interval timer functions

— Watchdog timer

8-Bit Timer/Counter

— Programmable 8-bit timer

— External event counter

— Arbitrary clock frequency output

— External clock signal divider

— Serial I/O interface clock generator

8-Bit Serial I/O Interface

— 8-bit transmit/receive mode

— 8-bit receive only mode

— LSB-first or MSB-first transmission selectable

— Internal or external clock source

Bit Sequential Carrier

— Support 16-bit serial data transfer in arbitrary format

Watch Timer

— Timer interval generation: 0.5 s, 3.9 ms at 32,768 Hz

— Four frequency outputs to BUZ pin

— Clock source generation for LCD

Interrupts

— Three internal vectored interrupts: INTB, INTT0, INTS

— Four external vectored interrupts: INT0, INT1, INT4, INTK

— Two quasi-interrupts: INT2, INTW

Memory-Mapped I/O Structure

— Data memory bank 15

Two Power-Down Modes

— Idle mode (only CPU clock stops)

— Stop mode (main system oscillation stops)

— Subsystem clock stop mode

Oscillation Sources

— Crystal, ceramic, or External RC for system clock

— Main system clock frequency: 0.4 MHz–6 MHz

— Subsystem clock frequency: 32,768 kHz

— CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

— 0.67 us at 6 MHz (minimum)

— 0.95 μs at 4.19 MHz (minimum)

— 122 μs at 32,768 kHz (minimum)

Operating Temperature

— – 40 °C to 85 °C

Operating Voltage Range

— 2.0 V to 5.5 V

Package Type

— 80-pin QFP

BLOCK DIAGRAM

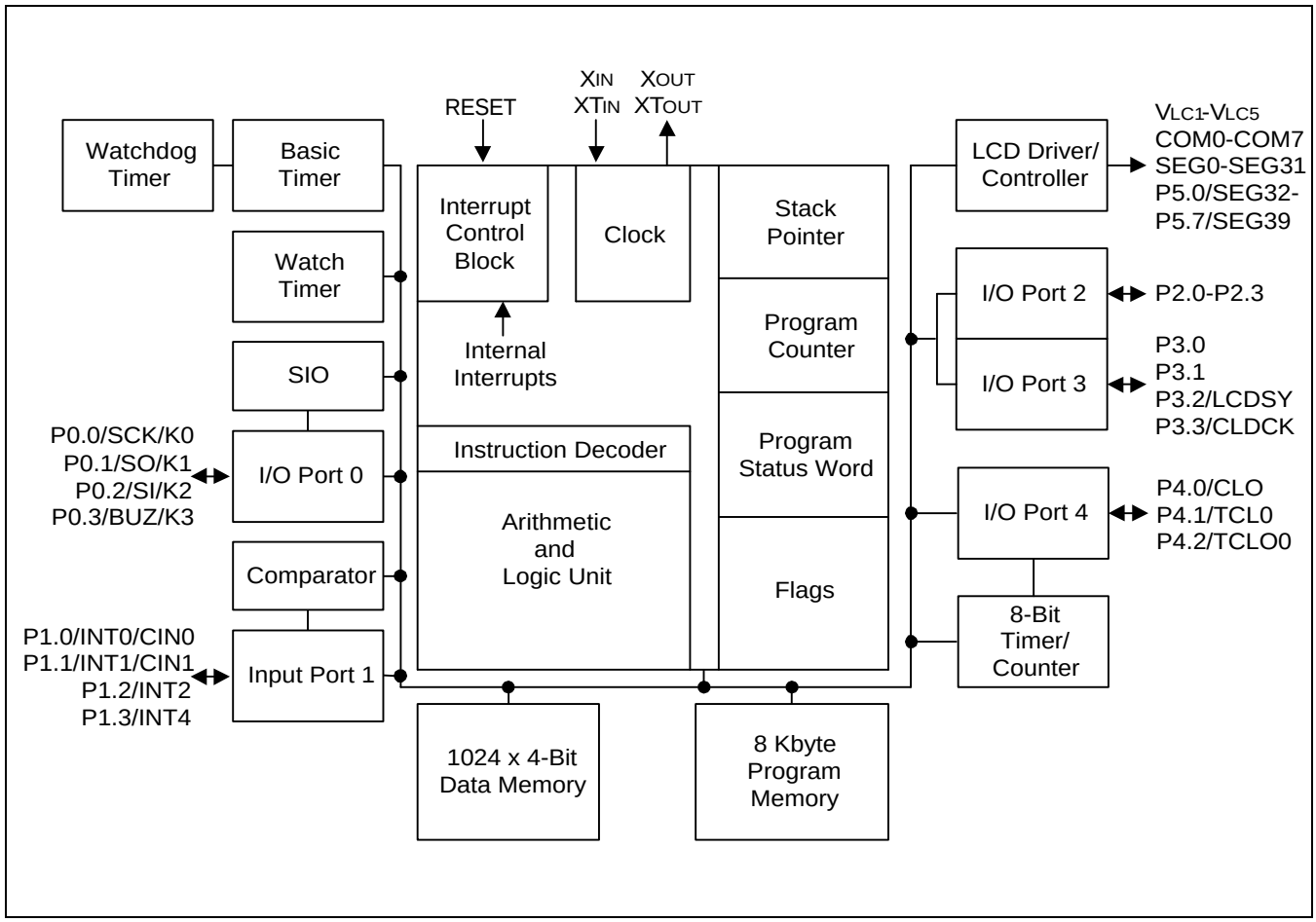


Figure 1-1. S3C72K8 Simplified Block Diagram

PIN ASSIGNMENTS

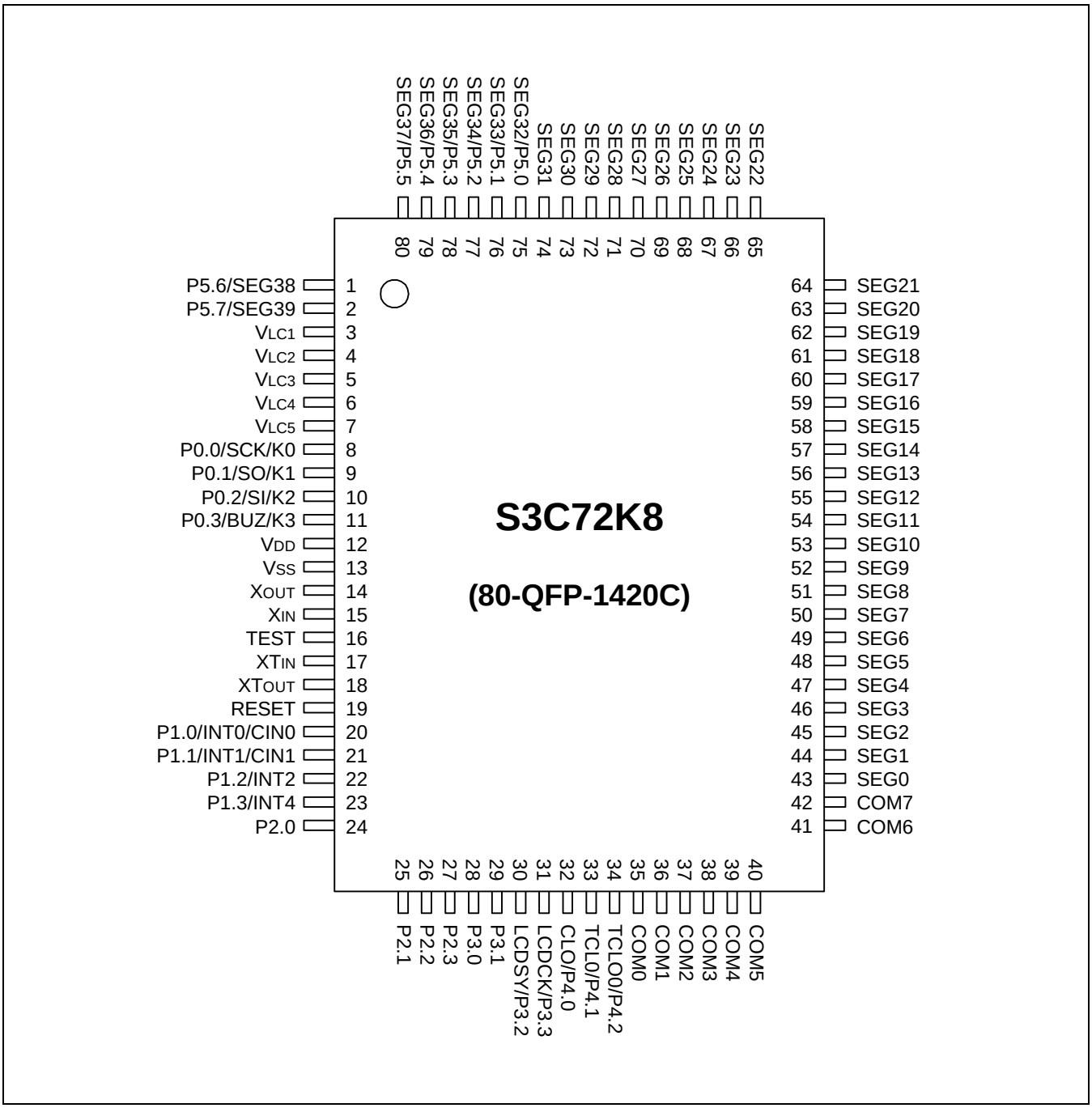


Figure 1-2. S3C72K8 80-QFP Pin Assignment

PIN DESCRIPTIONS

Table 1-1. S3C72K8 Pin Descriptions

Pin Name	Pin Type	Description	Circuit Type	Pin Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. Individual pins are software configurable as open-drain or push-pull output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	E–2	8 9 10 11	K0/SCK K1/SO K2/SI K3/BUZ
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit or 4-bit read and test are possible. The 1-bit unit pull-up resistors are assigned to input pins by software. An interrupt is generated by digital input at P1.0, P1.1.	F–4 F–4 A–3 A–3	20 21 22 23	INT0/CIN0 INT1/CIN1 INT2 INT4
P2.0–P2.3	I/O	Same as port 0 except that 8-bit read/write and test is possible.	E–2	24–27	–
P3.0 P3.1 P3.2 P3.3				28 29 30 31	– – LCDSY LCDCK
P4.0 P4.1 P4.2	I/O	Same as port 0 except that port 4 is 3-bit I/O port.	E–2	32 33 34	CLO TCL0 TCLO0
P5.0–P5.7	O	Output port for 1-bit data	H–11	75–80,1,2	SEG32–SEG39
SCK	I/O	Serial I/O interface clock signal	E–2	8	P0.0/K0
SO	I/O	Serial data output	E–2	9	P0.1/K1
SI	I/O	Serial data input	E–2	10	P0.2/K2
BUZ	I/O	2 KHz, 4 KHz, 8 KHz or 16 KHz frequency output at the watch timer clock frequency of 32.768 kHz.	E–2	11	P0.3/K3
K0–K3	I/O	External interrupt. The triggering edge is selectable.	E–2	8–11	P0.0–P0.3
INT0 INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	F–4	20 21	P1.0/CIN0 P1.1/CIN1
INT2	I	Quasi-interrupt with detection of rising or falling edges	A–3	22	P1.2
INT4	I	External interrupts with detection of rising and falling edges	A–3	23	P1.3

Table 1-1. S3C72K8 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Circuit Type	Pin Number	Share Pin
CIN0 CIN1	I	2-channel comparator input. CIN0: comparator input or external reference input CIN1: comparator input only.	F–4	20 21	P1.0/INT0 P1.1/INT1
LCDSY	I/O	LCD synchronization clock output for display expansion	E–2	30	P3.2
LCDCK	I/O	LCD clock output for display expansion	E–2	31	P3.3
CLO	I/O	Clock output	E–2	32	P4.0
TCL0	I/O	External clock input for timer/counter 0	E–2	33	P4.1
TCLO0	I/O	Timer/counter 0 clock output	E–2	34	P4.2
SEG32– SEG39	O	LCD segment signal output	H–11	75– 80,1,2	P5.0–P5.7
SEG0– SEG31	O	LCD segment signal output	H–6	43–74	–
COM0– COM7	O	LCD common signal output	H–6	35–42	–
V_{LC1}–V_{LC5}	–	LCD power supply. Voltage dividing resistors are assignable by mask option.	–	3–7	–
X_{IN}, X_{OUT}	–	Crystal, ceramic or RC oscillator pins for system clock.	–	15, 14	–
XT_{IN}, XT_{OUT}	–	Crystal oscillator pins for subsystem clock.	–	17, 18	–
V_{DD}	–	Main power supply	–	12	–
V_{SS}	–	Ground	–	13	–
RESET	I	Chip reset signal input	B	19	–
TEST	I	Chip test signal input (must be connected to V_{SS})	–	16	–

NOTE: Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode

PIN CIRCUIT DIAGRAMS

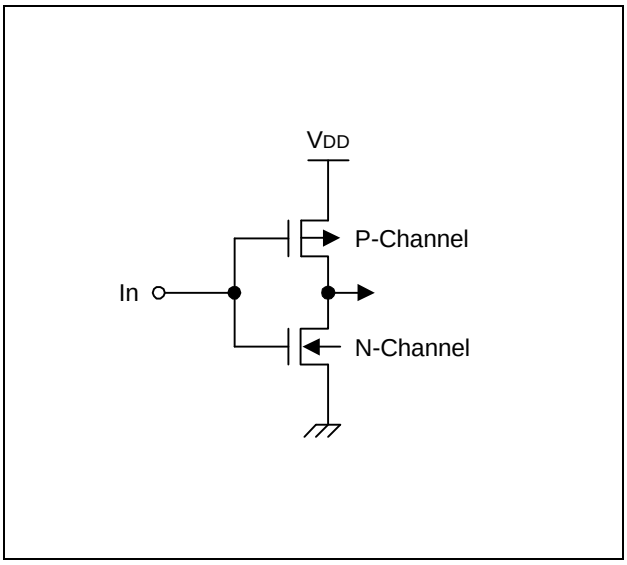


Figure 1-3. Pin Circuit Type A

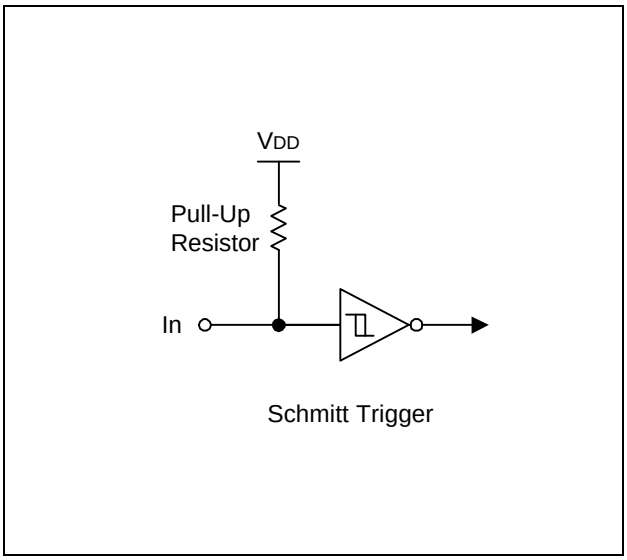


Figure 1-5. Pin Circuit Type B

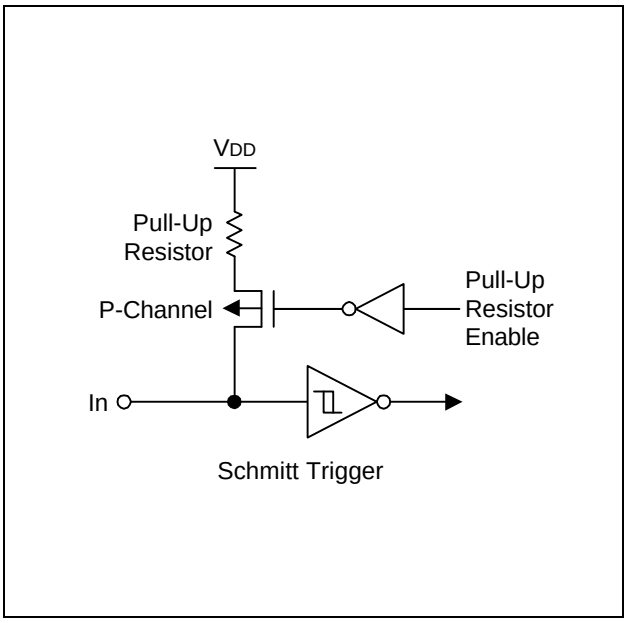


Figure 1-4. Pin Circuit Type A-3

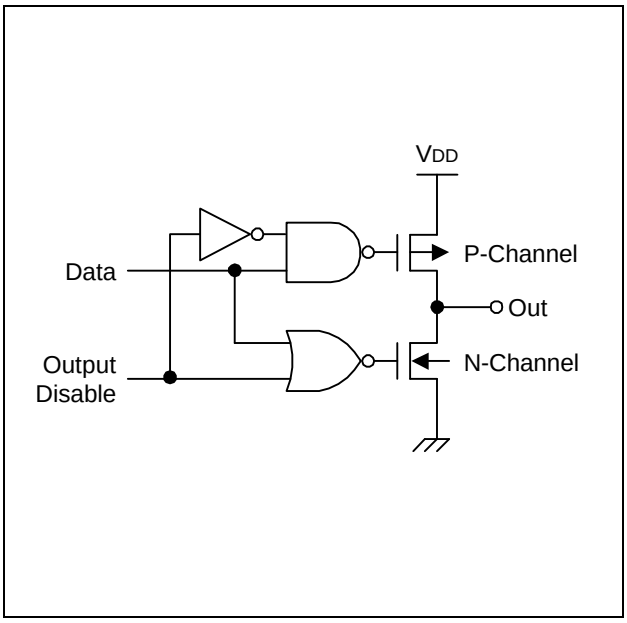


Figure 1-6. Pin Circuit Type 7

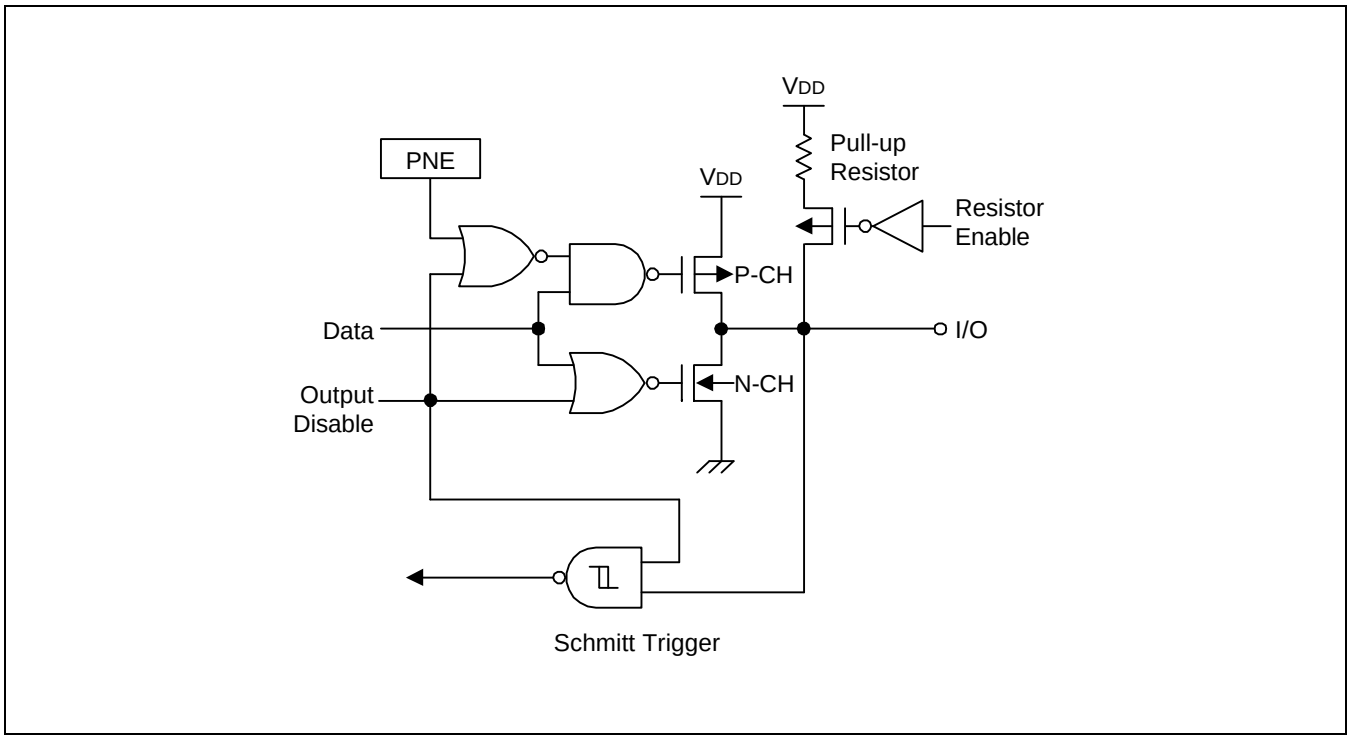


Figure 1-7. Pin Circuit Type E-2

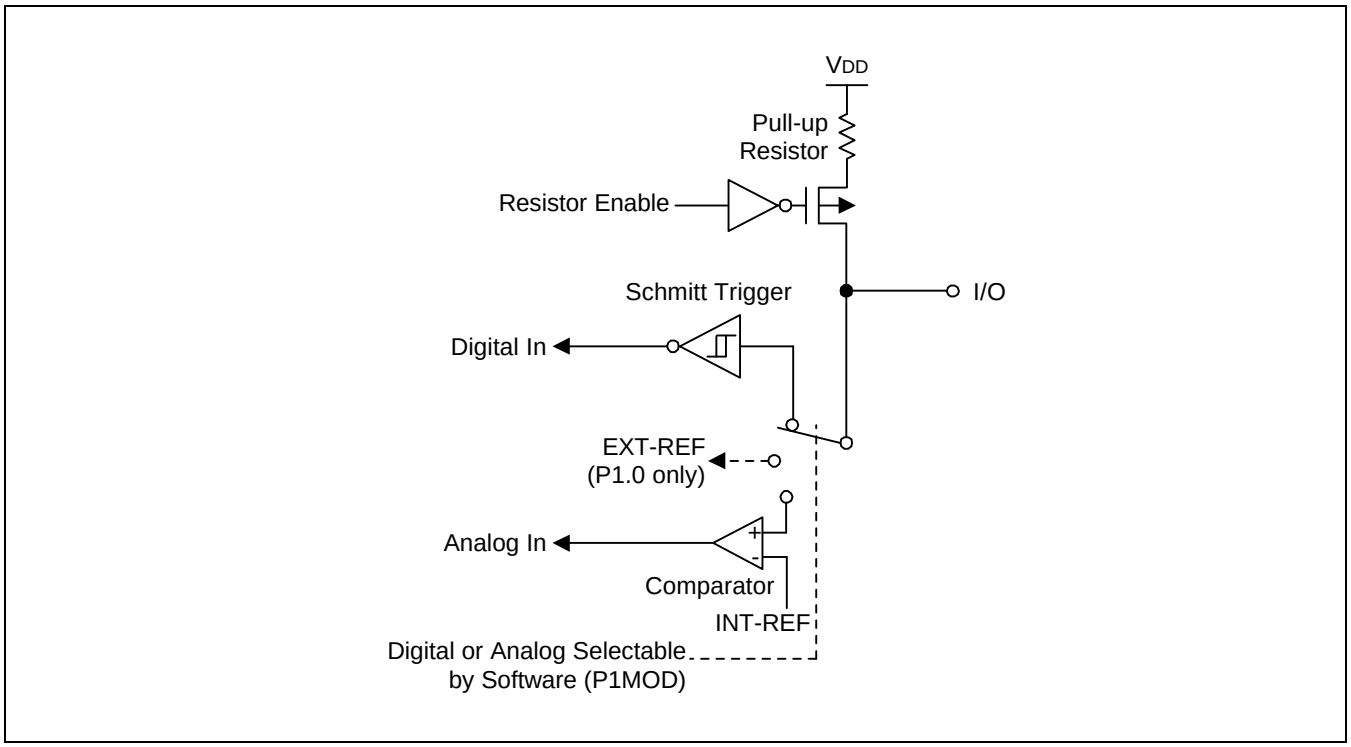


Figure 1-8. Pin Circuit Type F-4

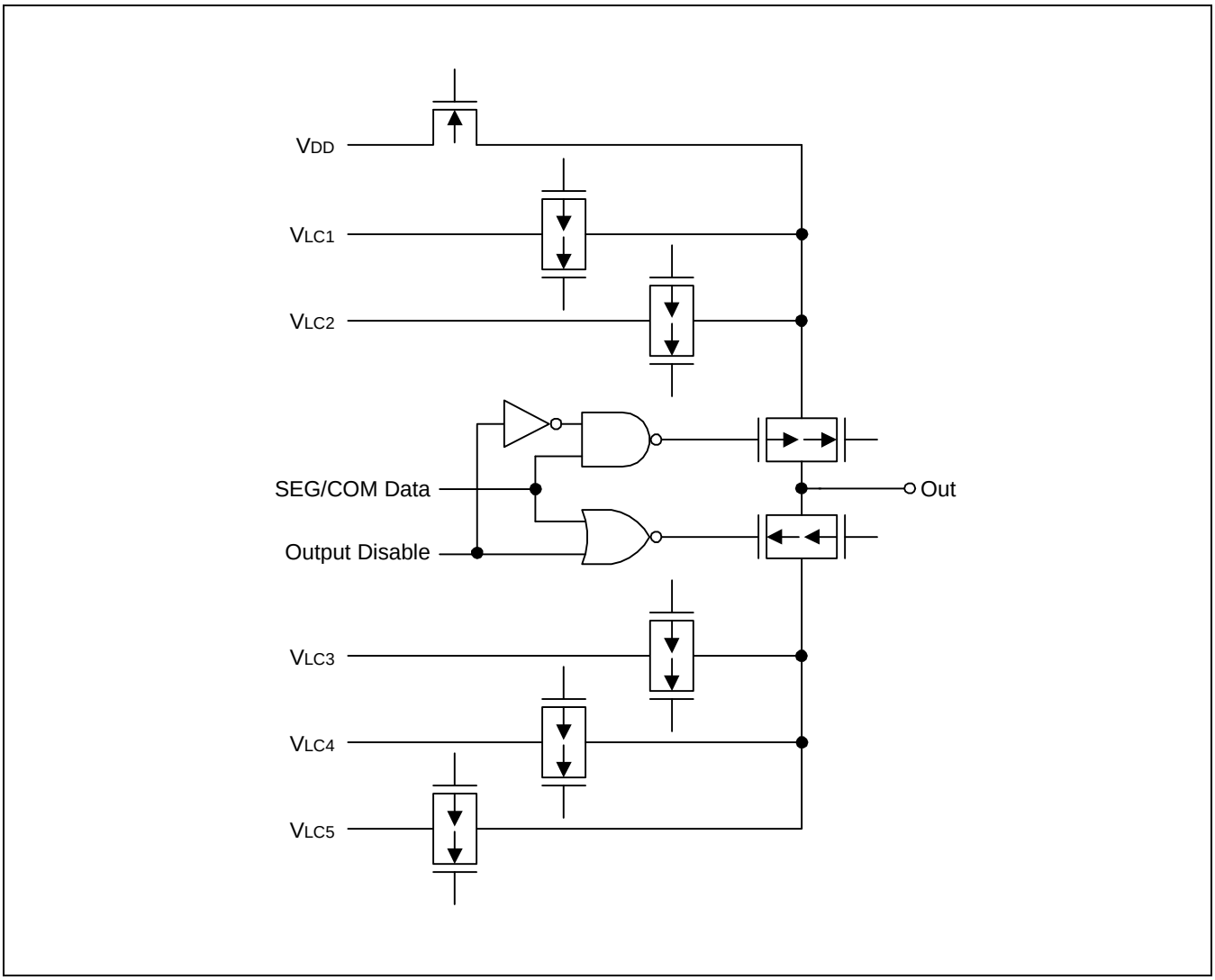


Figure 1-9. Pin Circuit Type H-5

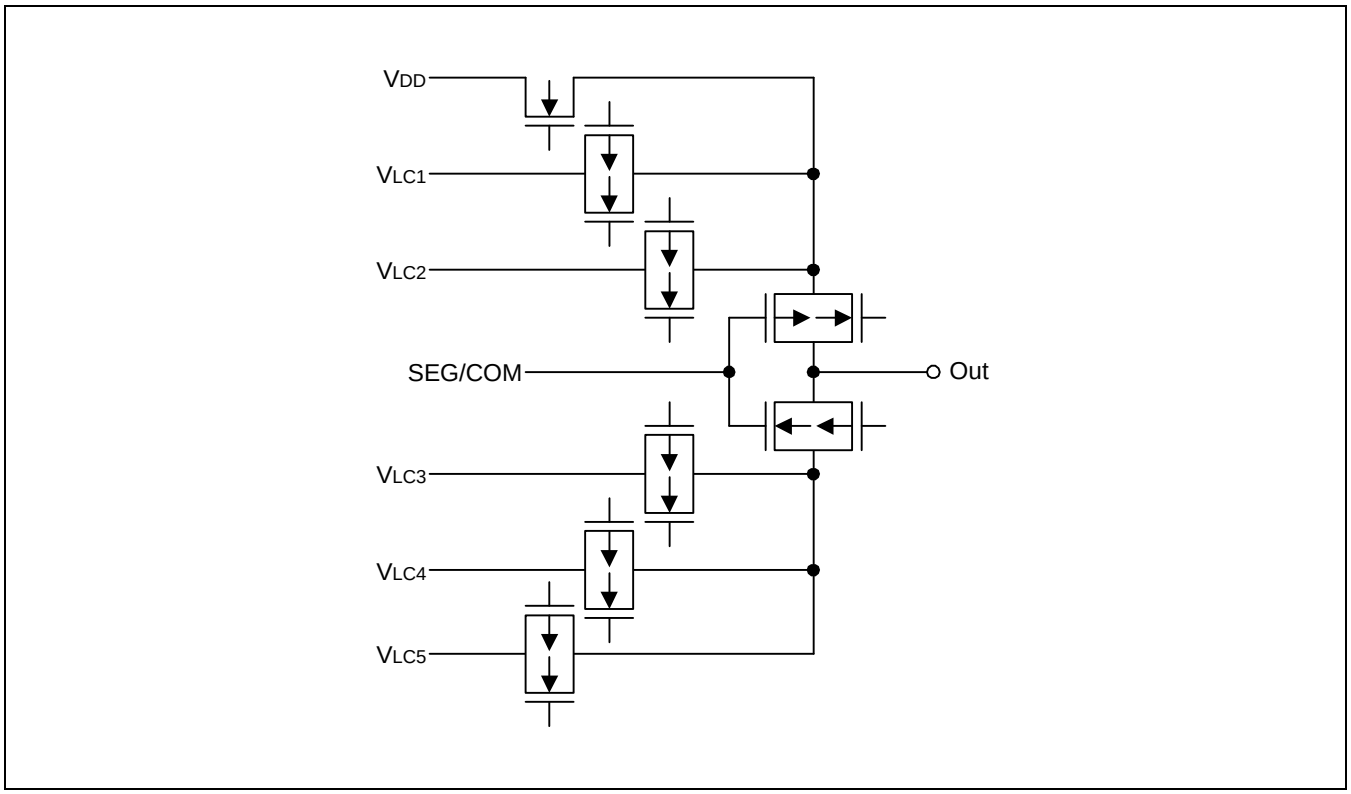


Figure 1-10. Pin Circuit Type H-6

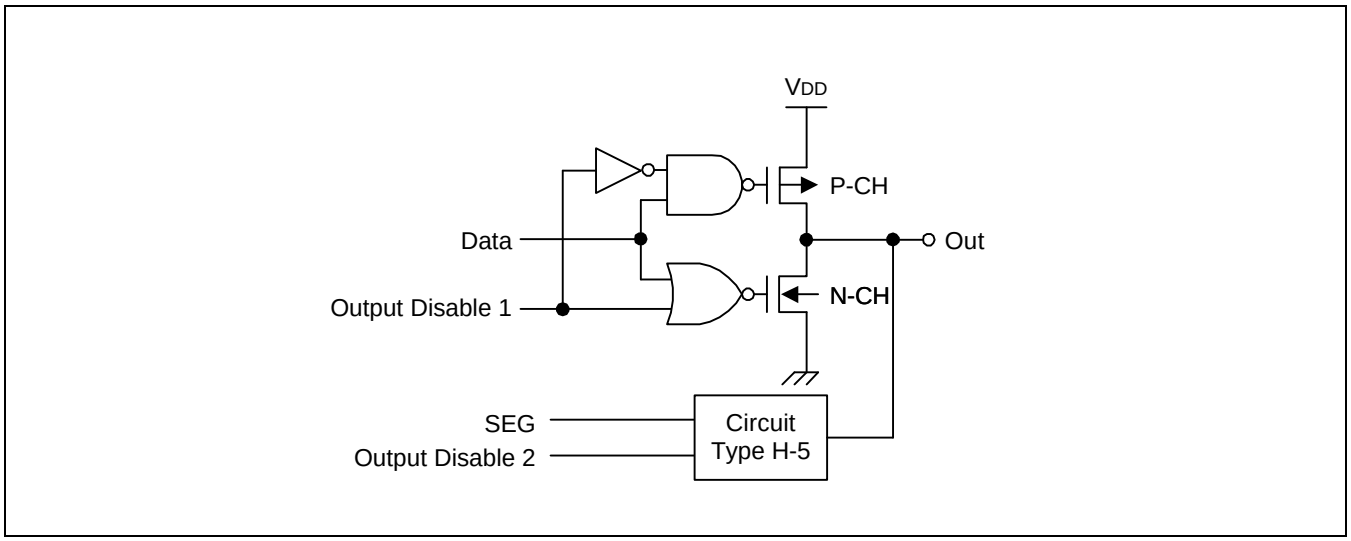


Figure 1-11. Pin Circuit Type H-11

15 ELECTRICAL DATA

OVERVIEW

In this section, information on S3C72K8 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— Main system clock oscillator characteristics
— Subsystem clock oscillator characteristics
— I/O capacitance
— Comparator electrical characteristics
— A.C. electrical characteristics
— Operating voltage range

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Miscellaneous Timing Waveforms

— A.C timing measurement points
— Clock timing measurement at X_{IN}
— Clock timing measurement at XT_{IN}
— TCL timing
— Input timing for RESET signal
— Input timing for external interrupts
— Serial data transfer timing

Table 15-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_{I1}	All I/O pins active	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active	– 15	mA
		All I/O pins active	– 35	
Output Current Low	I_{OL}	One I/O pin active	+ 30 (Peak value)	mA
			+ 15 (note)	
		All I/O port, total	+ 100 (Peak value)	
			+ 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 15-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	Ports 2, 3, P4.0 and P4.2	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, P4.1 and RESET	0.8 V_{DD}		V_{DD}	
	V_{IH3}	X_{IN}, X_{OUT} and XT_{IN}	V_{DD} – 0.1		V_{DD}	
Input Low Voltage	V_{IL1}	Ports 2, 3, P4.0 and P4.2	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, P4.1 and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT} and XT_{IN}			0.1	
Output High Voltage	V_{OH1}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 3 mA Ports 0, 2, 3 and 4	V_{DD} – 2.0	V_{DD} – 0.4	–	V
	V_{OH2}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 100 µA Ports 5	V_{DD} – 2.0	–	–	
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA Ports 0, 2, 3 and 4	–	0.4	2	V
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 100 µA Ports 5	–	–	1	
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}, X_{OUT} and XT_{IN}			20	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, X_{OUT}, XT_{IN}, and RESET	–	–	– 3	µA
	I_{LIL2}	V_{IN} = 0 V X_{IN}, X_{OUT} and XT_{IN}			– 20	
Output High Leakage Current	I_{LOH}	V_O = V_{DD} All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	– 3	µA

Table 15-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Pull-Up Resistor	R_{LI}	V_{IN} = 0 V; V_{DD} = 5 V ± 10 % Ports 0-4	15	40	80	kΩ
		V_{DD} = 3 V ± 10 %	30	80	200	
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ± 10 % RESET	150	220	350	
		V_{DD} = 3 V ± 10 %	300	400	800	
LCD Voltage Dividing Resistor	R_{LCD}	–	40	60	90	kΩ
$\|V_{DD}$-COMi$\|$ Voltage Drop (i = 0-7)	V_{DC}	V_{DD} = 2.7 V to 5.5 V – 15 μA per common pin	–	–	120	mV
$\|V_{DD}$-SEGx$\|$ Voltage Drop (x = 0-39)	V_{DS}	V_{DD} = 2.7 V to 5.5 V – 15 μA per segment pin	–	–	120	
V_{LC1} Output Voltage	V_{LC2}	V_{DD} = 2.0 V to 5.5 V (1) LCD clock = 0 Hz, V_{LC5} = 0 V	0.8 V_{DD} – 0.2	0.8 V_{DD}	0.8 V_{DD} + 0.2	V
V_{LC2} Output Voltage	V_{LC3}		0.6 V_{DD} – 0.2	0.6 V_{DD}	0.6 V_{DD} + 0.2	
V_{LC3} Output Voltage	V_{LC4}		0.4 V_{DD} – 0.2	0.4 V_{DD}	0.4 V_{DD} + 0.2	
V_{LC4} Output Voltage	V_{LC5}		0.2 V_{DD} – 0.2	0.2 V_{DD}	0.2 V_{DD} + 0.2	

Table 15-2. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

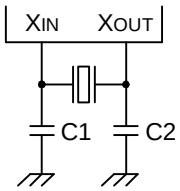
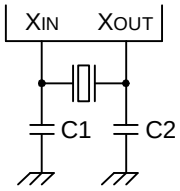
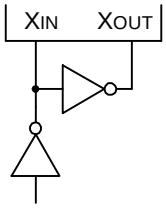
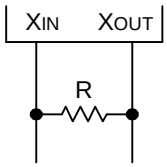
Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1} (2)	V_{DD} = 5 V ± 10% Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 4.19 MHz	–	3.5 2.5	8.0 5.5	mA
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		1.8 1.3	4.0 3.0	
	I_{DD2} (2)	Idle mode V_{DD} = 5 V ± 10% Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 4.19 MHz		1.3 1.2	2.5 1.8	
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		0.5 0.4	1.5 1.0	
	I_{DD3} (3)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	15	30	µA
	I_{DD4} (3)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator			6	15	
	I_{DD5}	Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0000B XT_{IN} = 0V		2.5	5	
		Stop mode; V_{DD} = 3 V ± 10%			0.5	3	
		V_{DD} = 5 V ± 10%	SCMOD = 0100B		0.2	3	
		V_{DD} = 3 V ± 10%			0.1	2	

NOTES:

1. Currents in the following circuits are not included; on-chip pull-up resistors, internal LCD voltage dividing resistors, output port drive currents, comparator.
2. Data includes power consumption for subsystem clock oscillation.
3. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.
4. Every values in this table is measured when the power control register (PCON) is set to "0011B".

Table 15-3. Main System Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 2.0 V to 5.5 V)

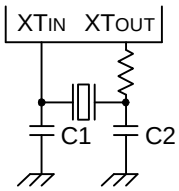
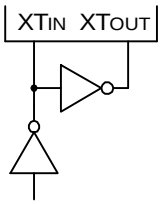
Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	V_{DD} = 4.5 V to 5.5 V	–	–	10	ms
			V_{DD} = 2.7 V to 4.5 V	–	–	30	
External Clock		X_{IN} input frequency (1)	–	0.4	–	6.0	MHz
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns
RC Oscillator		Frequency	R = 10 kΩ, V_{DD} = 5 V	–	2	–	MHz
			R = 30 kΩ, V_{DD} = 3 V	–	1	–	

NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 15-4. Subsystem Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 4.5 V to 5.5 V	–	1.0	2	s
			V_{DD} = 2.0 V to 4.5 V	–	–	10	
External Clock		XT_{IN} input frequency (1)	–	32	–	100	kHz
		XT_{IN} input high and low level width (t_{XTL}, t_{XTH})	–	5	–	15	µs

NOTES:

1. Oscillation frequency and XT_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs.

Table 15-5. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF

Table 15-6. Comparator Electrical Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 4.0 V to 5.5 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	–	–	0	–	V_{DD}	V
Reference Voltage Range	V_{REF}		0		V_{DD}	V
Input Voltage Accuracy	V_{CIN}		–		± 150	mV
Input Leakage Current	I_{CIN}, I_{REF}		– 3		3	µA

Table 15-7. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

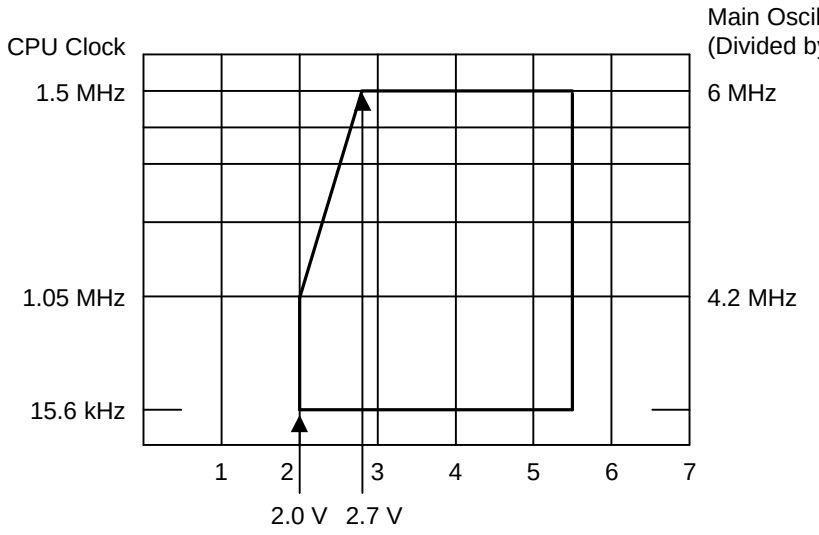
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (note)	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 2.0 V to 5.5 V	0.95	–	64	
		With subsystem clock (fxt)	114	122	125	
TCL0 Input Frequency	f_{TI0}, f_{TI1}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 2.0 V to 5.5 V			1	
TCL0 Input High, Low Width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 2.0 V to 5.5 V	1.8			
SCK Cycle Time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V External SCK source	800	–	–	ns
		Internal SCK source	650			
		V_{DD} = 2.0 V to 5.5 V External SCK source	3200			
		Internal SCK source	3800			
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 2.7 V to 5.5 V External SCK source	325	–	–	ns
		Internal SCK source	$t_{KCY}/2 - 50$			
		V_{DD} = 2.0 V to 5.5 V External SCK source	1600			
		Internal SCK source	$t_{KCY}/2 - 150$			
SI Setup Time to SCK High	t_{SIK}	V_{DD} = 2.7 V to 5.5 V External SCK source	100	–	–	ns
		Internal SCK source	150			
		V_{DD} = 2.0 V to 5.5 V External SCK source	150			
		Internal SCK source	500			
SI Hold Time to SCK High	t_{KSI}	V_{DD} = 2.7 V to 5.5 V External SCK source	400	–	–	ns
		Internal SCK source	400			
		V_{DD} = 2.0 V to 5.5 V External SCK source	600			
		Internal SCK source	500			

NOTE: Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock (fx) source.

Table 15-7. A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Delay for SCK to SO	t_{KSO}	V_{DD} = 2.7 V to 5.5 V External SCK source	–	–	300	ns
		Internal SCK source			250	
		V_{DD} = 2.0 V to 5.5 V External SCK source			1000	
		Internal SCK source			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0, INT1, INT2, INT4, K0–K3	10	–	–	µs
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs



CPU clock = 1/n x oscillator frequency (n = 4, 8 or 64)

Figure 15-1. Standard Operating Voltage Range

Table 15-8. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	2.0	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17} / fx	–	ms
		Released by interrupt	–	(2)	–	

NOTES:

1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

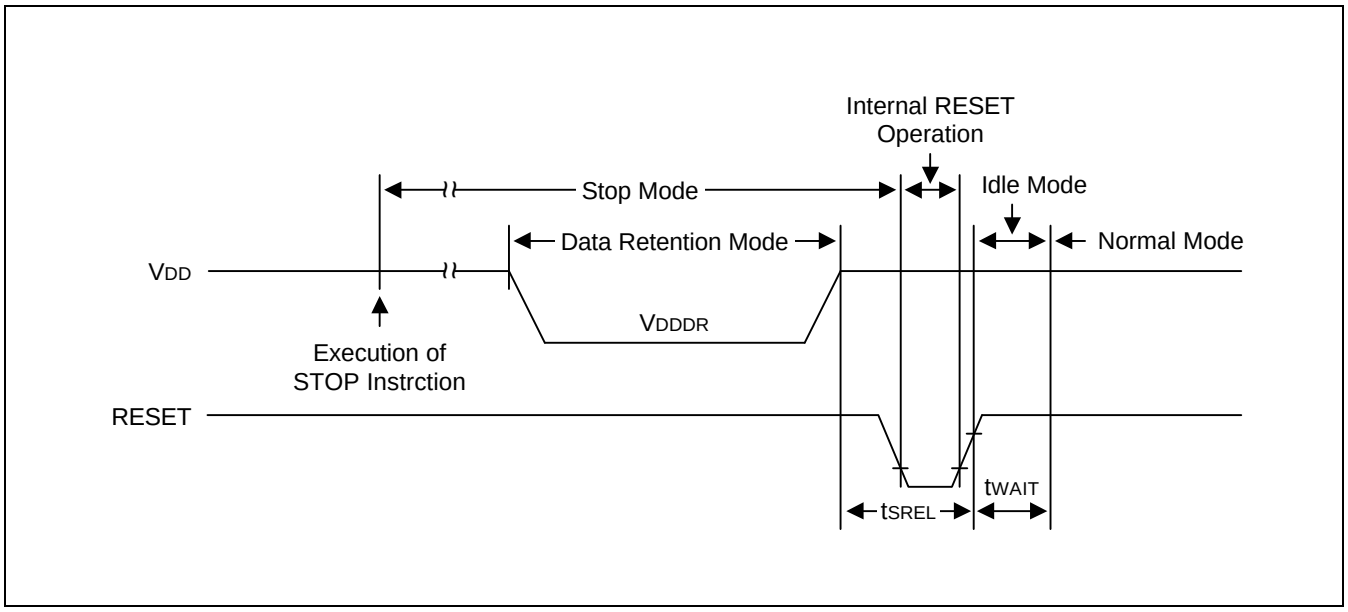


Figure 15-2. Stop Mode Release Timing When Initiated By RESET

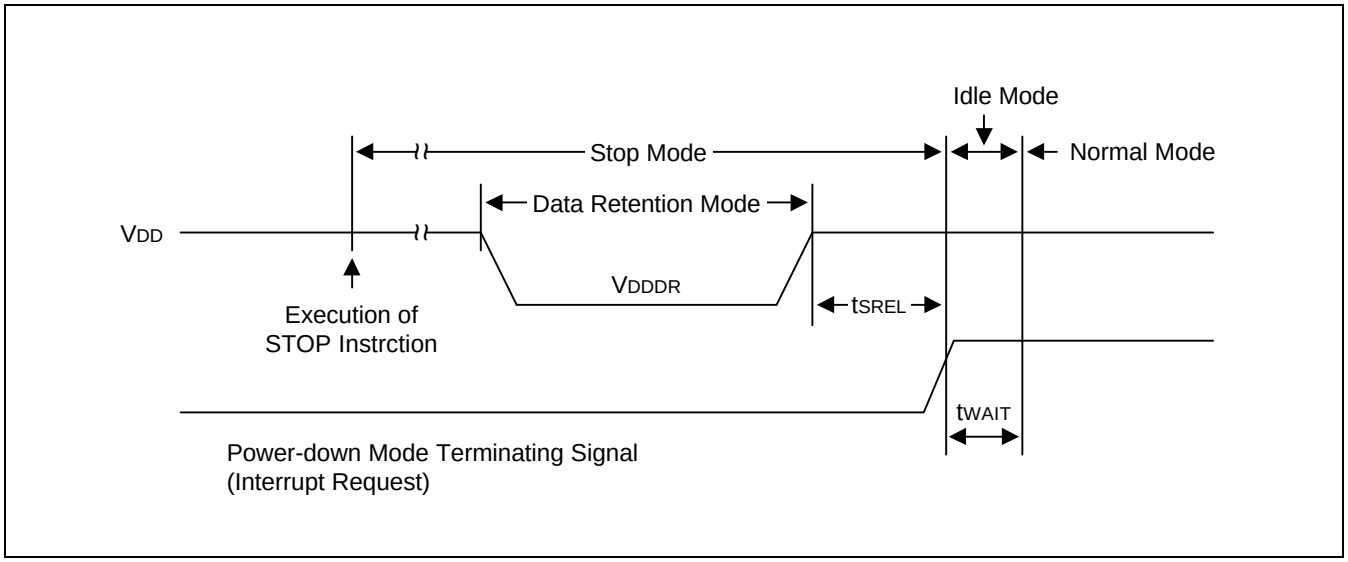


Figure 15-3. Stop Mode Release Timing When Initiated By Interrupt Request

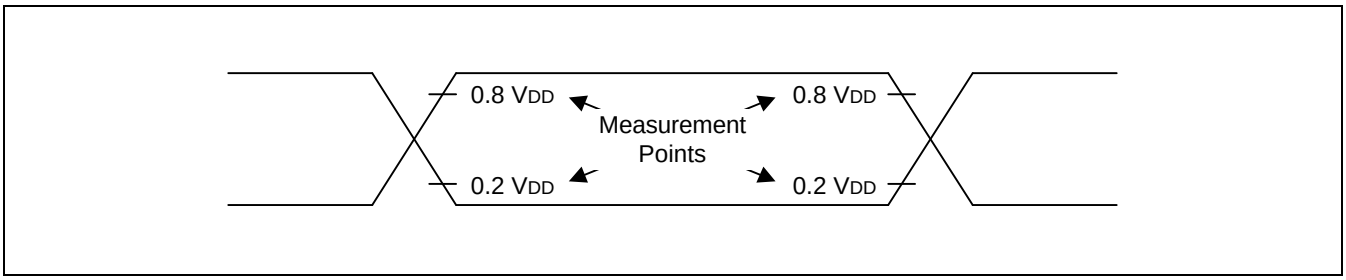


Figure 15-4. A.C. Timing Measurement Points (Except for X_{IN} and XT_{IN})

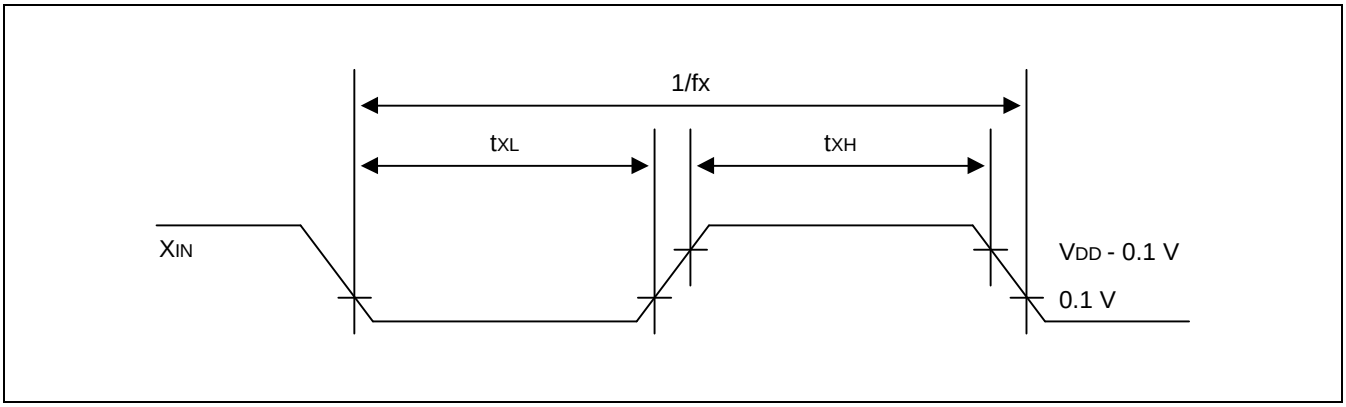


Figure 15-5. Clock Timing Measurement at X_{IN}

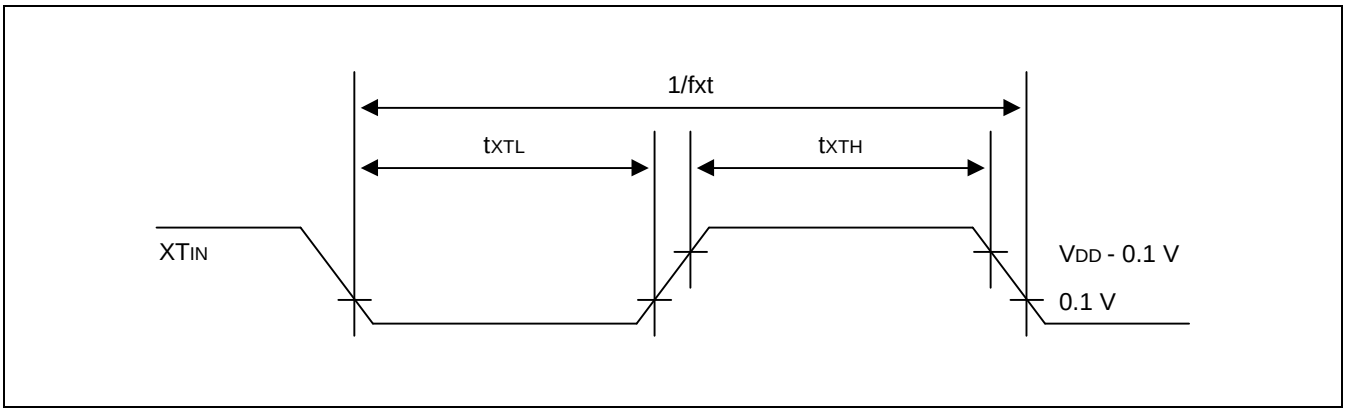


Figure 15-6. Clock Timing Measurement at XT_{IN}

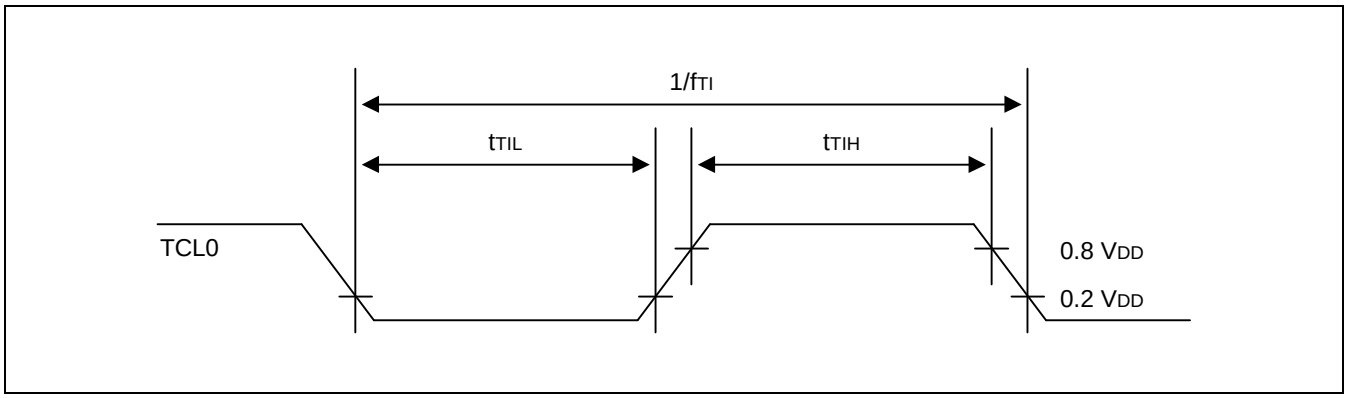


Figure 15-7. TCL Timing

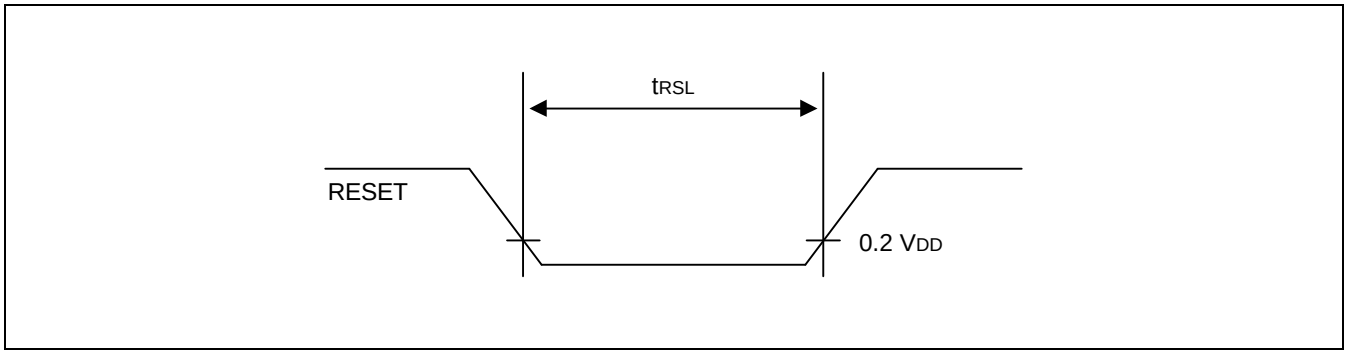


Figure 15-8. Input Timing for RESET Signal

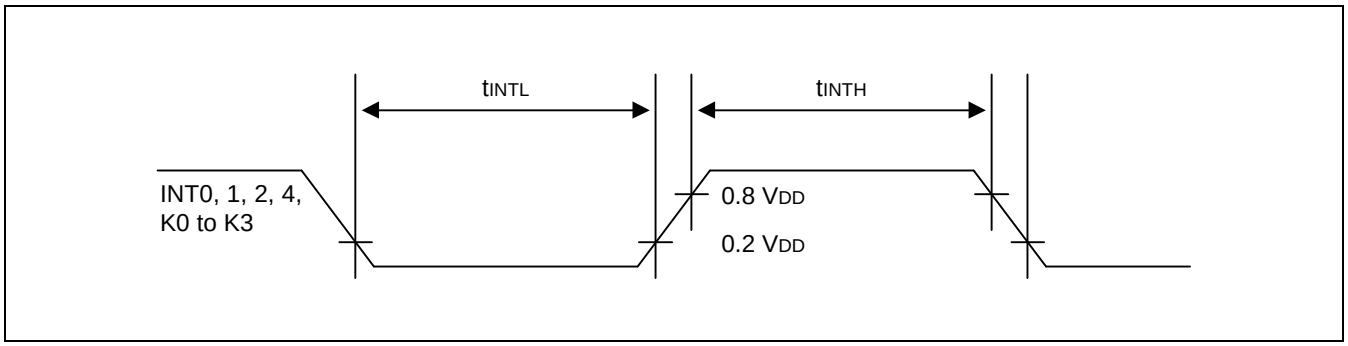


Figure 15-9. Input Timing for External Interrupts and Quasi-Interrupts

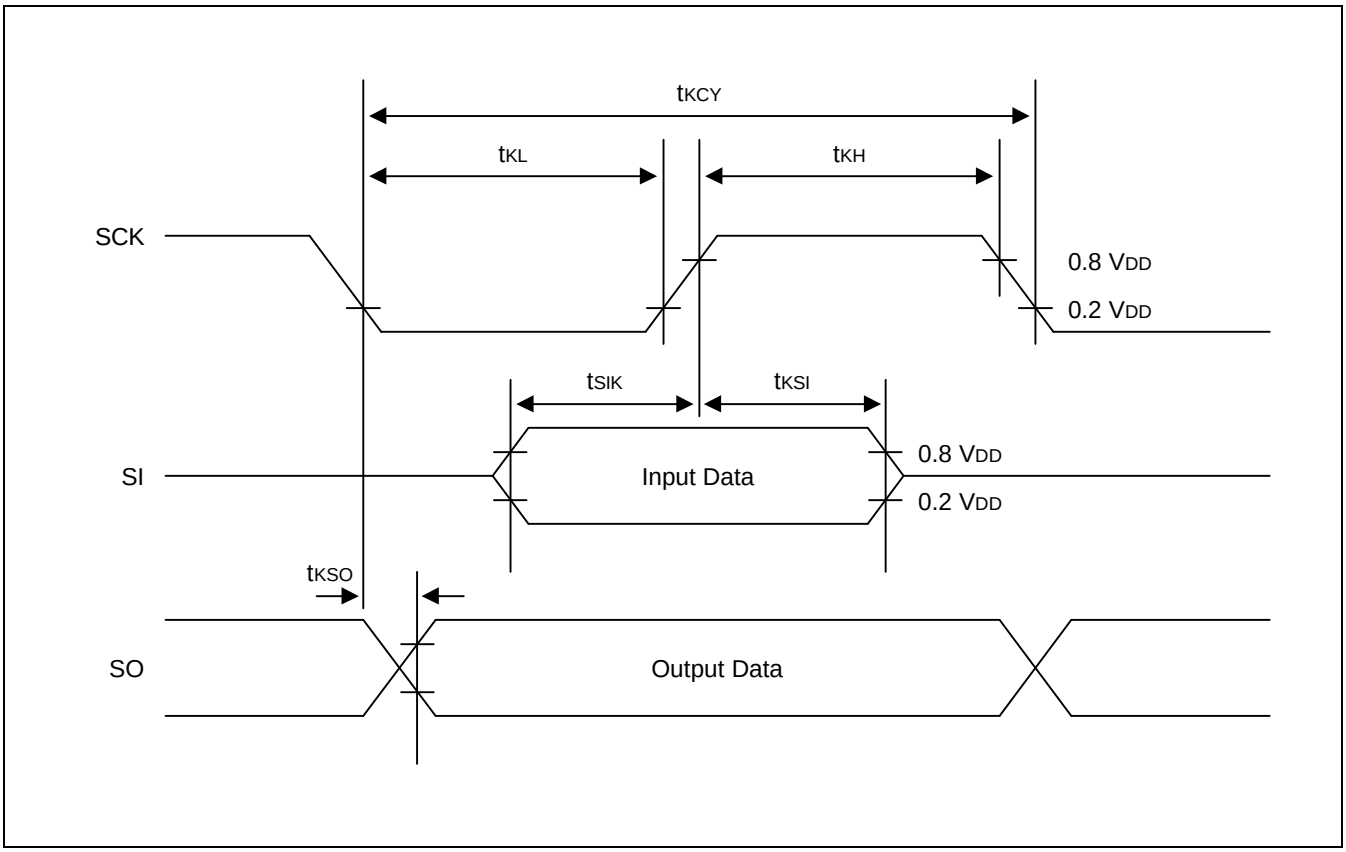
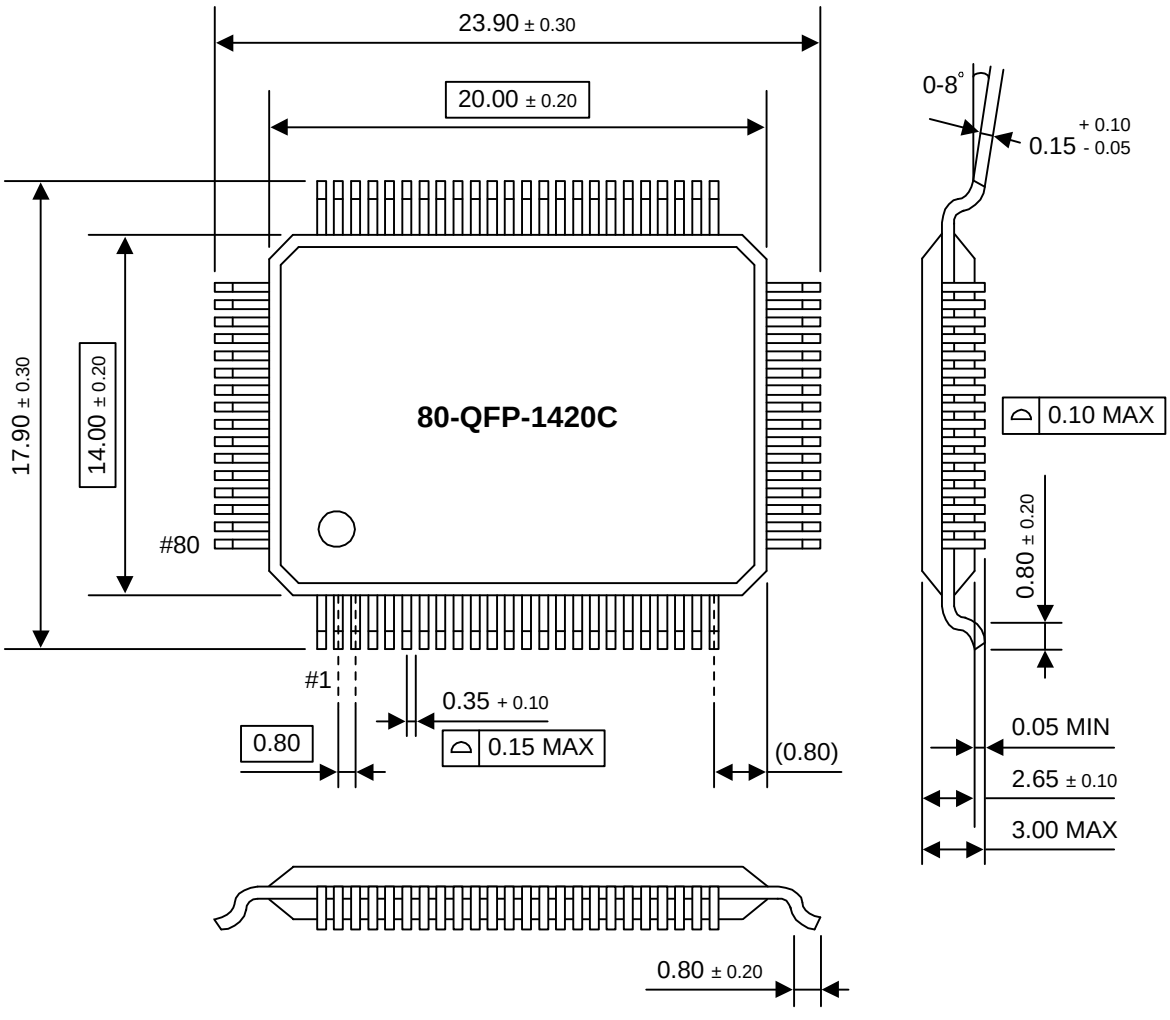


Figure 15-10. Serial Data Transfer Timing

16 MECHANICAL DATA

OVERVIEW

The S3C72K8 microcontroller is currently available in a 80-pin QFP package.



NOTE: Dimensions are in millimeters.

Figure 16-1. 80-QFP-1420C Package Dimensions

17 S3P72K8 OTP

OVERVIEW

The S3P72K8 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C72K8 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P72K8 is fully compatible with the S3C72K8, both in function and in pin configuration except ROM size. Because of its simple programming requirements, the S3P72K8 is ideal for use as an evaluation chip for the S3C72K8.

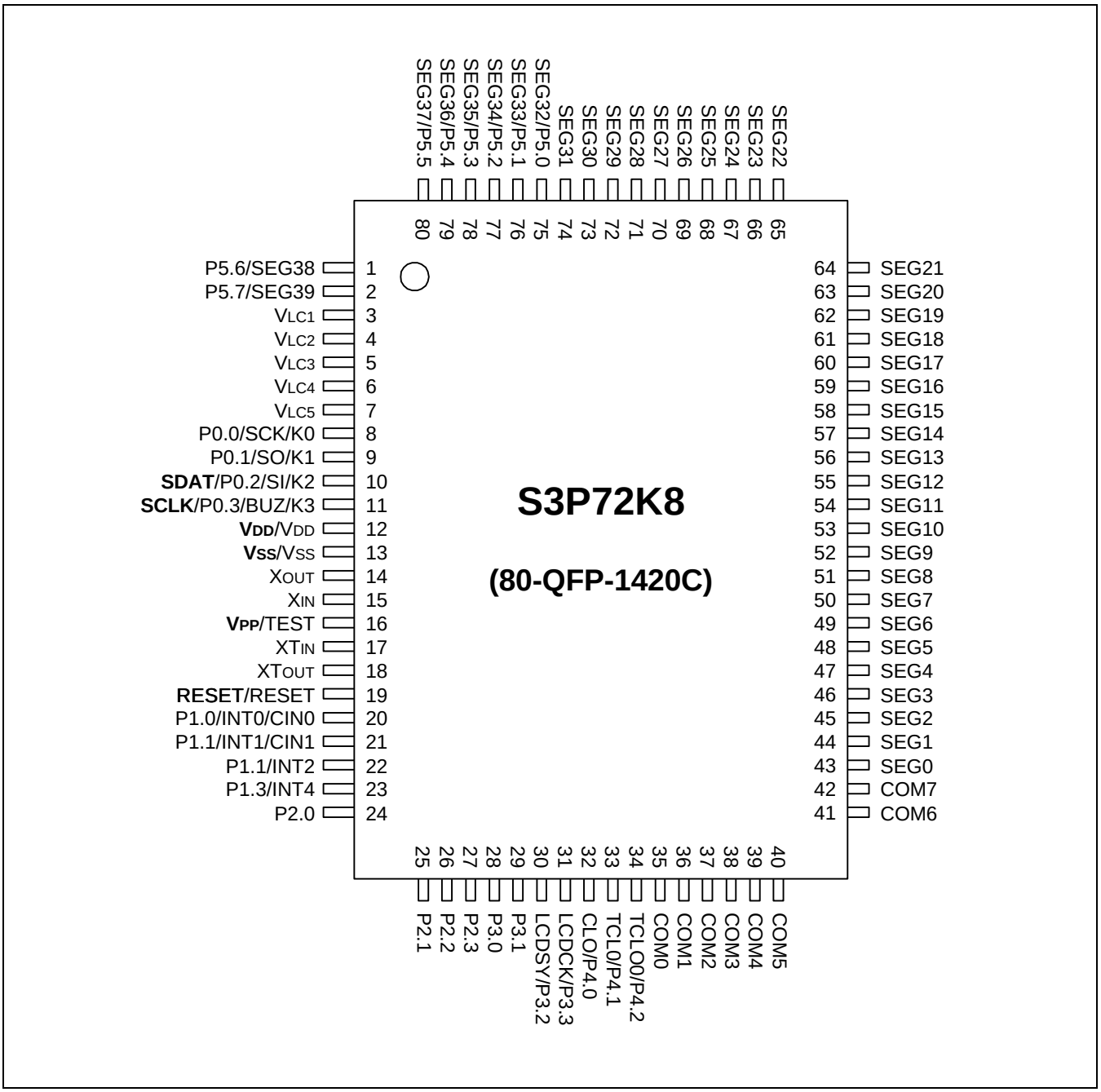


Figure 17-1. S3P72K8 Pin Assignments (80-QFP Package)

Table 17-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P0.2	SDAT	10	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P0.3	SCLK	11	I	Serial clock pin. Input only pin.
TEST	V_{PP}	16	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	19	I	Chip Initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	12/13	I	Logic power supply pin. V_{DD} should be tied to +5 V during programming.

Table 17-2. Comparison of S3P72K8 and S3C72K8 Features

Characteristic	S3P72K8	S3C72K8
Program Memory	8-Kbyte EPROM	8-Kbyte mask ROM
Operating Voltage (V_{DD})	2.0 V to 5.5 V	2.0 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST) = 12.5V	
Pin Configuration	80 QFP	80 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of the S3P72K8, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 17-3 below.

Table 17-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/ MEM	Address (A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

NOTES