AGP In-line Memory Module

(1Mx32 AIMM based on 1Mx32 SGRAM)

Unbuffered SGRAM
Graphics
32-bit Non-ECC/Parity
132-pin AIMM

Revision 1.0

July 2000

Revision History

Revision 1.0 (July 3, 2000)

• Changed ICC5 of M832G0115AP0-C**
• Applied Intel AIMM SPEC1.0. Refer to "Module dimensions" on page 13.

Revision 0.0 (May 10, 2000) - *Target Spec*

• First edition

M832G0115AP0 SGRAM AGP In-Line Memory Module

1Mx32 SGRAM AIMM based on 1Mx32, 2K Refresh, 3.3V Synchronous Graphic RAMs

GENERAL DESCRIPTION

The Samsung M832G0115AP is a 1M bit x 32 Synchronous Graphic RAM based AGP in-line memory module. The Samsung M832G0115AP consists of one 1M x 32 bit Synchronous Graphic RAMs in 100pin QFP packages mounted on a 132pin glass-epoxy substrate. The M832G0115AP is a AGP In-line Memory Module and is intended for mounting into 132-pin edge connector sockets(AGP socket).

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies and burst lengths allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part NO.	Frequency (tCC min)
M832G0115AP0-C7C	133MHz (7.5ns) @CL=2, tRCD/tRP=2CLK
M832G0115AP0-C70	133MHz (7.0ns) @CL=3, tRCD/tRP=3CLK

* M832G0115AP0 : based on PQFP Component

- Burst Mode Operation
- Independent byte operation via DQM0 ~ 3
- Auto & Self Refresh Capability (2048 cycles / 32ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- MRS cycle with address key programs.
  CAS Latency (2, 3)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- Resistor Strapping Options for speed
- PCB : Height 1,400mil, single sided components

PIN CONFIGURATIONS (B Side / A Side)

Pin	B	Pin	A	Pin	B	Pin	A	Pin	B	Pin	A
1	NC	1	NC	23	KEYWAY	23	KEYWAY	45	VCC	45	Vcc
2	NC	2	TYPEDET	24	KEYWAY	24	KEYWAY	46	DQ11	46	A7
3	NC	3	NC	25	KEYWAY	25	KEYWAY	47	VDDQ	47	CS
4	NC	4	NC	26	DQ21	26	CLK0	48	NC	48	NC
5	GND	5	GND	27	DQ20	27	CLK1*	49	GND	49	GND
6	NC	6	NC	28	Vcc	28	Vcc	50	NC	50	A6
7	NC	7	NC	29	DQ19	29	CAS	51	DQ10	51	A1
8	DQ27	8	NC	30	DQ18	30	NC	52	VDDQ	52	VDDQ
9	Vcc	9	Vcc	31	GND	31	GND	53	DQ9	53	A5
10	DQ28	10	DQM3	32	NC	32	NC	54	DQ8	54	A2
11	DQ29	11	NC	33	DQ17	33	RAS	55	GND	55	GND
12	DQ30	12	DQ24	34	VDDQ	34	VDDQ	56	DQM1	56	A4
13	GND	13	GND	35	DQ16	35	A0	57	DQ0	57	A3
14	NC	14	NC	36	DQ15	36	A9	58	VDDQ	58	VDDQ
15	DQ31	15	DQ25	37	GND	37	GND	59	NC	59	NC
16	Vcc	16	Vcc	38	DQ14	38	A11	60	DQ1	60	DQ5
17	DQM2	17	DQ26	39	DQ13	39	A10	61	GND	61	GND
18	NC	18	NC	40	VDDQ	40	VDDQ	62	DQ2	62	DQ6
19	GND	19	GND	41	DQ12	41	A8/AP*	63	DQ3	63	DQ7
20	DQ23	20	WE	42	NC	42	NC	64	VDDQ	64	VDDQ
21	DQ22	21	FSEL	43	GND	43	GND	65	DQ4	65	DQM0
22	KEYWAY	22	KEYWAY	44	NC	44	NC	66	NC	66	NC

MODULE PIN NAMES

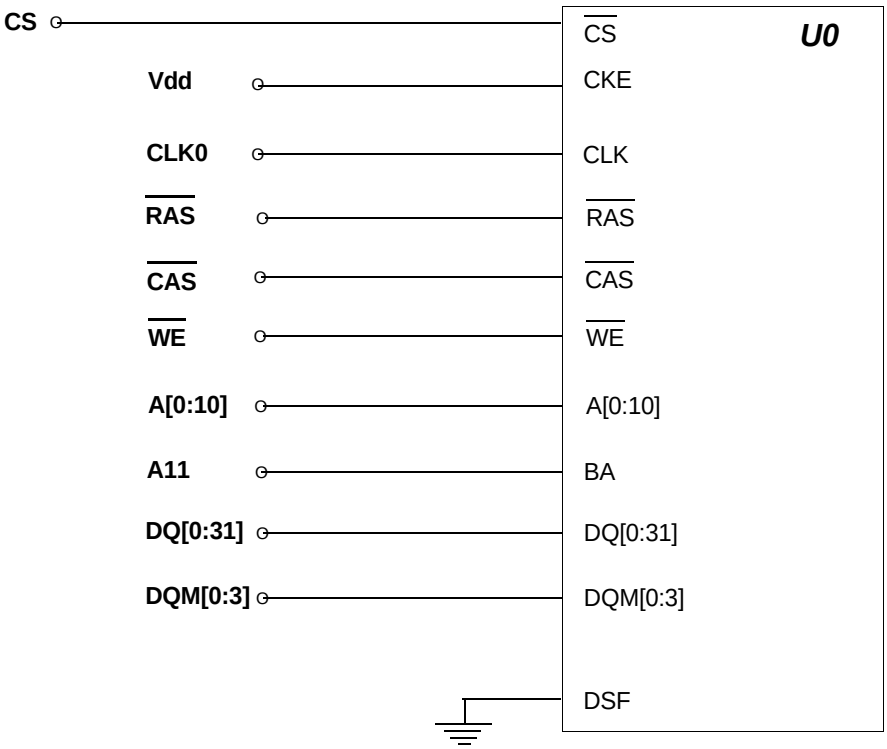
Pin Name	Function
A0~A10	Address Input (multiplexed)
A11	SDRAM Bank Select (BA)
DQ0 ~ DQ31	Data Inputs / Outputs
CLK0,CLK1*	Clock Input
$\overline{CS}$	Chip Select Input
CKE	CLK Enable
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Colume Address Strobe
$\overline{WE}$	Write Enable
DQM	DQ Mask Enable
Vcc	Power Supply
Vddq	Power supply for Data In/Out
GND	Ground(Vss)
NC	No Connection
KEYWAY*	KEYWAY
FSEL*	Memory Frequency Select
TYPEDET*	TYPEDET

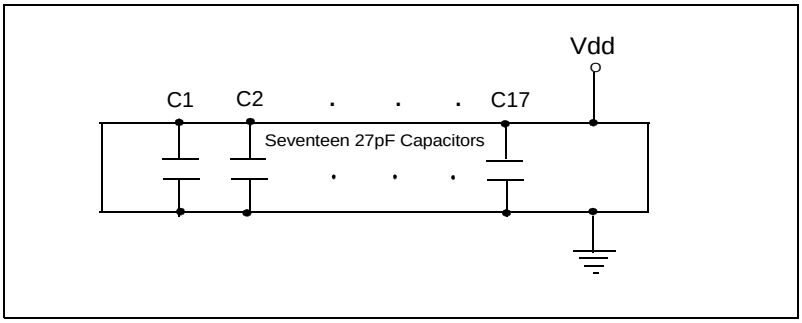
* These pins are not used in this module and should be NC

COMPONENT PIN CONFIGURATION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQMi
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock + t_{SS} prior to new command. Disable input buffers for power down in standby.
A0 ~ A10	*Address*	Row / Column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, Column address : CA_0 ~ CA_7
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and Row precharge.
DQMi	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.(Byte Masking)
DQi	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
DSF	*Define Special Function*	Not used. Must Connected to low
V_{DD}/V_{SS}	*Power Supply /Ground*	Power Supply : +3.3V±0.3V/Ground
V_{DDQ}/V_{SSQ}	*Data Output Power /Ground*	Provide isolated Power/Ground to DQs for improved noise immunity.
N.C	*No Connection*	No connection

FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS(Voltage referenced to V_{SS})

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	5
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3
Output leakage current	I_{LO}	-10	-	10	uA	4
Output Loading Condition	see figure 1					

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DD}.
5. The VDD condition of M832G0115-7C is 3.135V~3.6V.

CAPACITANCE (V_{CC} = 3.3V, T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A10, BA)	C_{IN1}	-	14	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	C_{IN2}	-	14	pF
Input capacitance (CLK0)	C_{IN3}	-	14	pF
Input capacitance ($\overline{CS}$)	C_{IN4}	-	14	pF
Input capacitance (DQM0 ~ DQM3)	C_{IN5}	-	14	pF
Data input/output capacitance (DQ0 ~ DQ31)	C_{OUT}	-	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C, $V_{IH(min)}/V_{IL(max)}$=2.0V/0.8V)

Parameter	Symbol	Test Condition	CAS Latency	Speed		Unit	Note
				-7C	-70		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min), $t_{CC} \geq t_{CC}$(min), I_O = 0mA	3	-	160	mA	2
			2	200	150		
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		2		mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2			
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		30		mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		15			
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		4		mA	
	I_{CC3PS}	CKE ≤ V_{IL}(max), t_{CC} = ∞		4			
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		50		mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		30			
Operating Current (Burst Mode)	I_{CC4}	I_O = 0 mA, Page Burst All bank Activated, t_{CCD} = t_{CCD}(min)	3	-	230	mA	2
			2	290	160		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3	-	200	mA	3
			2	240	190		
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		2		mA	

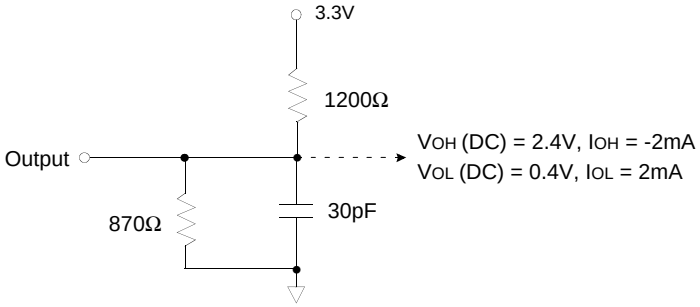
Note : 1. Unless otherwise notes, Input level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}) in LVTTL.

2. Measured with outputs open. Addresses are changed only one time during tcc(min).

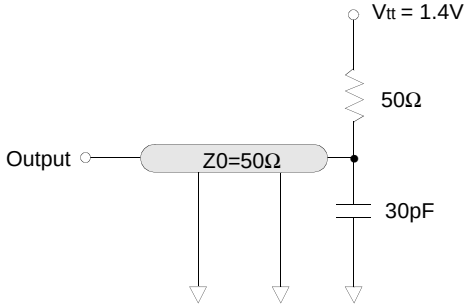
3. Refresh period is 32ms. Addresses are changed only one time during tcc(min).

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70°C)

Parameter	Value
AC input levels	V_{ih}/V_{il} = 2.4V / 0.4V
Input timing measurement reference level	1.4V
Input rise and fall time(See note 3)	t_R/t_F=1ns/ 1ns
Output timing measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

Note : The VDD condition of M832G0115AP-C7C is 3.135V~3.6V.

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version				Unit	Note
			-7C		-70			
CAS Latency		CL	-	2	3	2	CLK	
CLK cycle time		$t_{CC(min)}$	-	7.5	7	10	ns	
Row active to row active delay		$t_{RRD(min)}$	2				CLK	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$		2	3	2	CLK	1
Row precharge time		$t_{RP(min)}$		2	3	2	CLK	1
Row active time		$t_{RAS(min)}$		6	7	5	CLK	1
		$t_{RAS(max)}$	100				us	
Row cycle time		$t_{RC(min)}$	-	8	10	7	CLK	1
Last data in to row precharge		$t_{RDL(min)}$	2				CLK	2
Last data in to new col.address delay		$t_{CDL(min)}$	1				CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1				CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1				CLK	
Mode Register Set cycle time		$t_{MRS(min)}$	1				CLK	
Number of valid output data	CAS Latency=3		2				ea	4
	CAS Latency=2		1					

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer. Refer to the following ns-unit based AC table.

Parameter	Symbol	Version				Unit
		-7C		-70		
Clock latency	t_{CL}	-	2	3	2	CLK
CLK cycle time	$t_{CC(min)}$	-	7.5	7	10	ns
Row active to row active delay	$t_{RRD(min)}$	-	15	14	20	ns
$\overline{RAS}$ to $\overline{CAS}$ delay	$t_{RCD(min)}$	-	15	21	20	ns
Row precharge time	$t_{RP(min)}$	-	15	21	20	ns
Row active time	$t_{RAS(min)}$	-	45	49	50	ns
	$t_{RAS(max)}$	100				us
Row cycle time	$t_{RC(min)}$	-	60	70	70	ns

2. Minimum delay is required to complete write.
3. This parameter means minimum $\overline{CAS}$ to $\overline{CAS}$ delay at block write cycle only.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-7C		-70		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS Latency=3	t_{CC}	-	1000	7	1000	ns	1
	CAS Latency=2		7.5		10			
CLK to valid output delay	CAS Latency=3	t_{SAC}	-	-	-	5.5	ns	1, 2
	CAS Latency=2		-	6.0	-	6.0		
Output data hold time		t_{OH}	2	-	2	-	ns	2
CLK high pulse width	CAS Latency=3	t_{CH}	-		3	-	ns	3
	CAS Latency=2		2					
CLK low pulse width	CAS Latency=3	t_{CL}	-	-	3	-	ns	3
	CAS Latency=2		2					
Input setup time	CAS Latency=3	t_{SS}	-	-	1.75	-	ns	3
	CAS Latency=2		1.5		2.5			
Input hold time		t_{SH}	1	-	1	-	ns	3
CLK to output in Low-Z		t_{SLZ}	1	-	1	-	ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}	-	-	-	5.5	ns	-
	CAS latency=2		-	6.0	-	6.0		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_8/AP	A_{10},A_9 ~ A_0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A_0 ~ A_7)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A_0 ~ A_7)	4
	Auto precharge enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H						V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand Code
A_0 ~ A_{10}, BA : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA : Bank select address.
If "Low" at read, write, Row active and precharge, bank A is selected.
If "High" at read, write, Row active and precharge, bank B is selected.
If A_8 is "High" at Row precharge, BA is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	BA		A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU			W.B.L	TM		CAS Latency			BT	Burst Length		

(Note 1)

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	Reserved
0	1	Vendor Use Only	0	0	1	-	1	Interleave	0	0	1	2	Reserved
1	0		0	1	0	2			0	1	0	4	4
1	1		0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
			1	1	1	Reserved			1	1	1	256(Full)	Reserved

(Note 2)

POWER UP SEQUENCE

SGRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and start clock. Must maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 may be changed.

The device is now ready for normal operation.

Note : 1. RFU (Reserved for Future Use) should stay "0" during MRS cycle.
2. The full column burst(256bit) is available only at Sequential mode of burst type.

BURST SEQUENCE (BURST LENGTH = 4)

Initial address		Sequential				Interleave			
A_1	A_0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial address			Sequential								Interleave							
A_2	A_1	A_0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

MODULE DIMENSIONS