1 PRODUCT OVERVIEW

OVERVIEW

The KS57C2916 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With an up-to-704-dot LCD direct drive capability, and flexible 8-bit timer/counter, the KS57C2916 offers an excellent design solution for a mid-end LCD game.

Up to 8 pins of the 80-pin QFP package can be dedicated to I/O. Six vectored interrupts provide fast response to internal and external events. In addition, the KS57C2916's advanced CMOS technology provides for low power consumption.

OTP

The KS57C2916 microcontroller is also available in OTP (One Time Programmable) version, KS57P2916. KS57P2916 microcontroller has an on-chip 16K-byte one-time-programable EPROM instead of masked ROM. The KS57P2916 is comparable to KS57C2916, both in function and in pin configuration.

FEATURES

Memory

- 256 × 4-bit RAM (excluding LCD display RAM)
- 16,384 × 8-bit ROM

8 I/O Pins

- I/O: 8 pins

LCD Controller/Driver

- 44 segments and 16 common terminals
  (8, 12 and 16 common selectable)
- Internal resistor circuit for LCD bias
- Voltage doubler
- All dot can be switched on/off

8-bit Basic Timer

- 4 interval timer functions
- Watch-dog timer

8-bit Timer/Counter

- Programmable 8-bit timer
- Arbitrary clock output (TCLO0)
- Inverted clock output (TCLO0)

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms
  at 32768 Hz
- Four frequency outputs to BUZ pin and BUZ pin
- Clock source generation for LCD

Interrupts

- Two internal vectored interrupts
- Four external vectored interrupts
- Two quasi-interrupts

Memory-Mapped I/O Structure

- Data memory bank 15

Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main system oscillation stops)
- Sub system clock stop mode

Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal oscillator for subsystem clock
- Main system clock frequency: 4.19 MHz
  (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 µs at 4.19 MHz (main)
- 122 µs at 32.768 kHz (subsystem)

Operating Temperature

- − 40 °C to 85 °C

Operating Voltage Range

- 2.2 V to 3.4 V (0.4 MHz to 4.19 MHz)
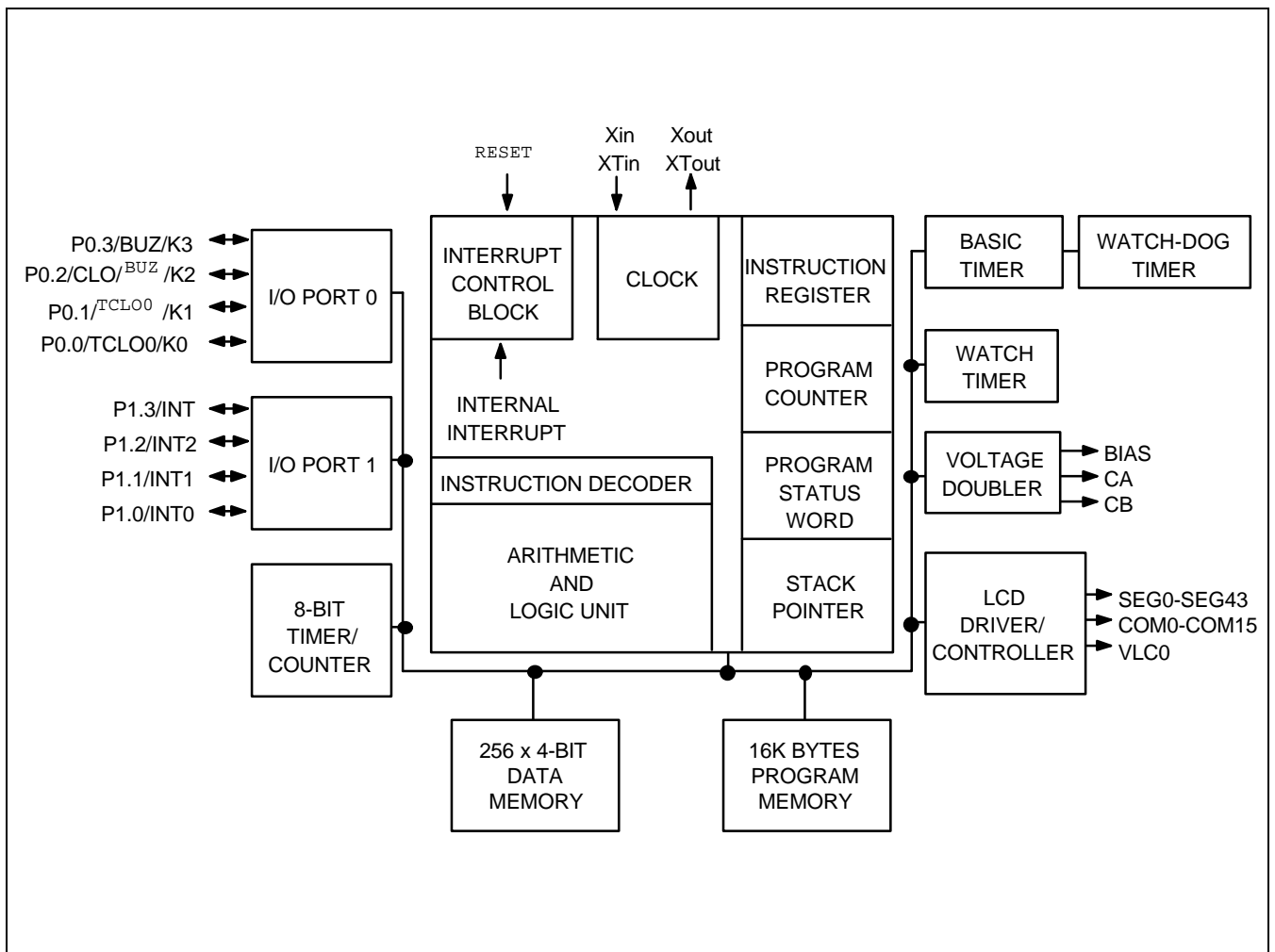
Package Type

- 80-pin QFP or pellet

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BLOCK DIAGRAM

Figure 1-1. KS57C2916 Simplified Block Diagram

PIN ASSIGNMENTS
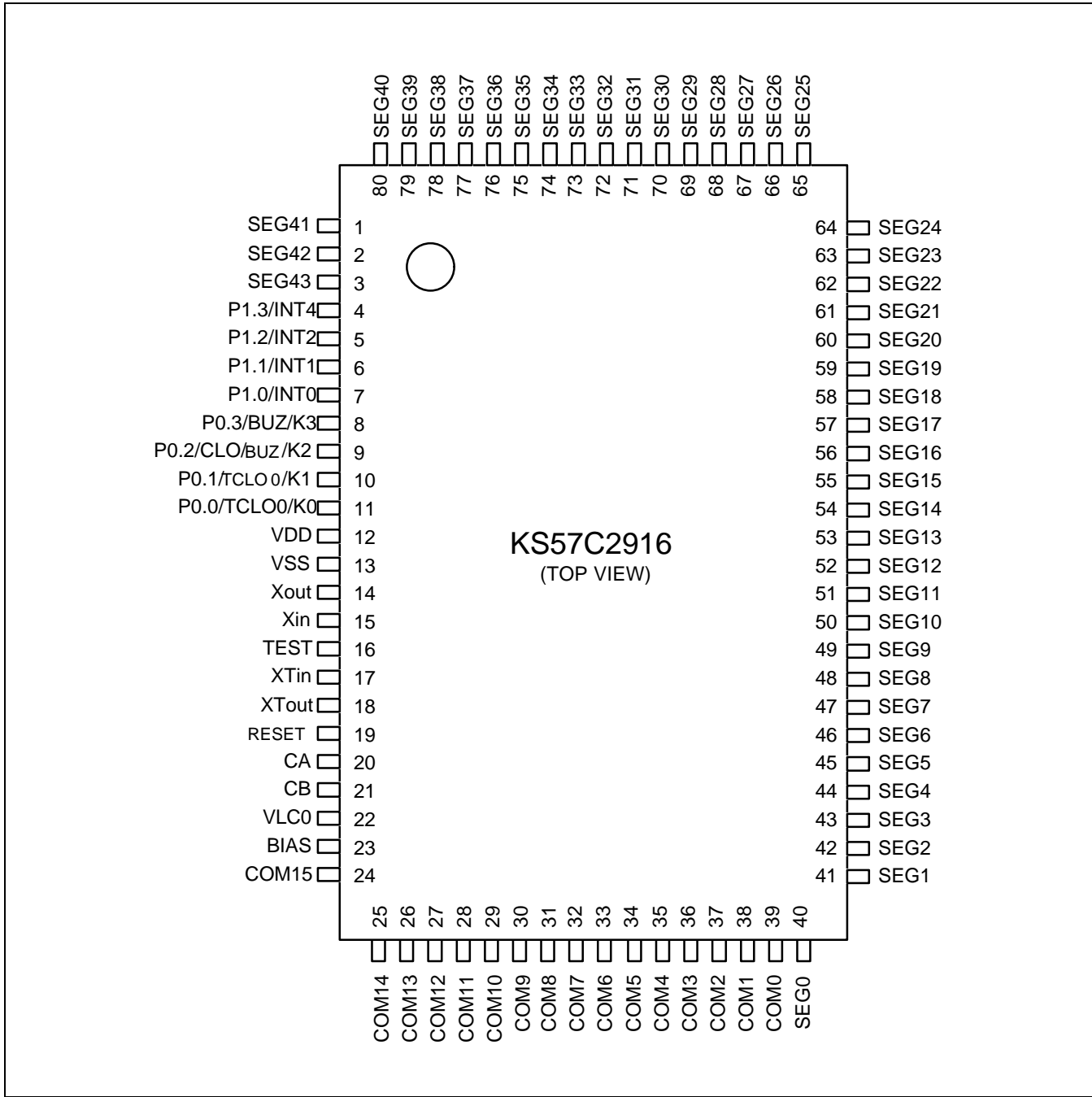
Figure 1-2. KS57C2916 80-QFP Pin Assignment Diagram

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PIN DESCRIPTIONS

Table 1-1. KS57C2916 Pin Descriptions

Pin Name	Pin Type	Description	Circuit Type	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test are possible. Individual pins are software configurable as input or output. Individual pins are software configurable as open-drain or push-pull output. Individual pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	E-1	11 10 9 8	TCLO0/K0 TCLO0/K1 CLO/BUZ/K2 BUZ/K3
P1.0 P1.1 P1.2 P1.3	I/O	Same as port 0.	E-1	7 6 5 4	INT0 INT1 INT2 INT4
INT0, INT1	I/O	External interrupts. The triggering edge for INT0 and INT1 is selectable.		7, 6	P1.0, P1.1
INT2	I/O	Quasi-interrupt with detection of rising or falling edges		5	P1.2
INT4	I/O	External interrupt with detection of rising or falling edges.		4	P1.3
BUZ	I/O	2 kHz, 4 kHz, 8 kHz or 16 kHz frequency output for buzzer sound.		8	P0.3/K3
BUZ	I/O	Inverted BUZ signal		9	P0.2/CLO/K2
CLO	I/O	Clock output		9	P0.2/BUZ/K2
TCLO0	I/O	Inverted Timer/counter 0 clock output		10	P0.1/K1
TCLO0	I/O	Timer/counter 0 clock output		11	P0.0/K0
COM0–COM15	O	LCD common signal output	H-6	39–24	–
SEG0–SEG43	O	LCD segment signal output	H-6	40–80, 1–3	–

Table 1-1. KS57C2916 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Circuit Type	Number	Share Pin
K0–K3	I/O	External interrupt (triggering edge is selectable)	E-1	11–8	P0.0–P0.3
V_{DD}	–	Power supply	–	12	–
V_{SS}	–	Ground	–	13	–
RESET	I	Reset input (active low)	B	19	–
CA, CB	–	Capacitor terminal for voltage doubling	–	20, 21	–
VCL0	–	LCD power supply input	–	22	–
BIAS	O	Doubling voltage level output	–	23	–
X_{in}, X_{out}	–	Crystal, ceramic or RC oscillator pins for system clock	–	15, 14	–
XT_{in}, XT_{out}	–	Crystal oscillator pins for subsystem clock	–	17, 18	–
TEST	I	Test input (must be connected to V_{SS})	–	16	–

NOTE: Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.
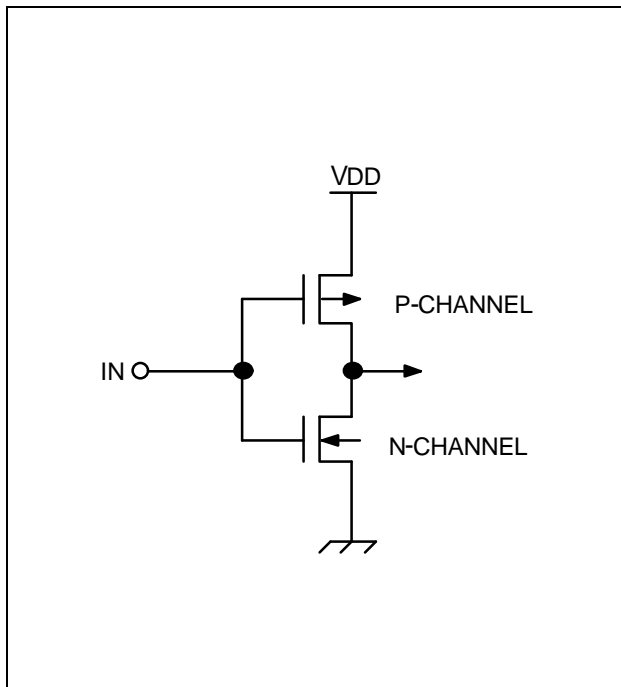
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PIN CIRCUIT DIAGRAMS

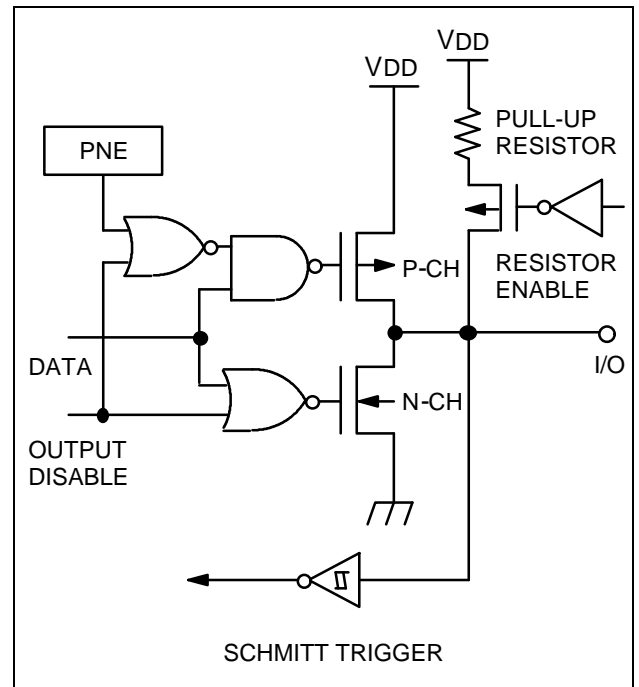**Figure 1-3. Pin Circuit Type A**

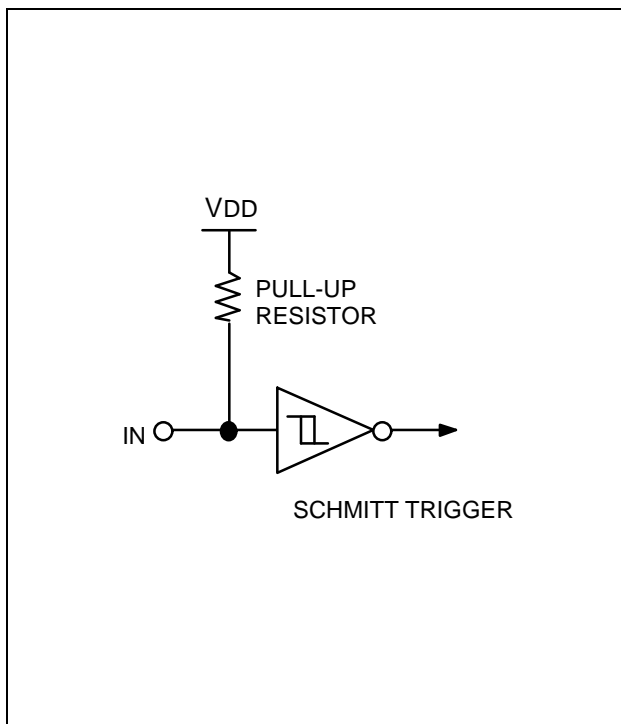**Figure 1-5. Pin Circuit Type E-1**
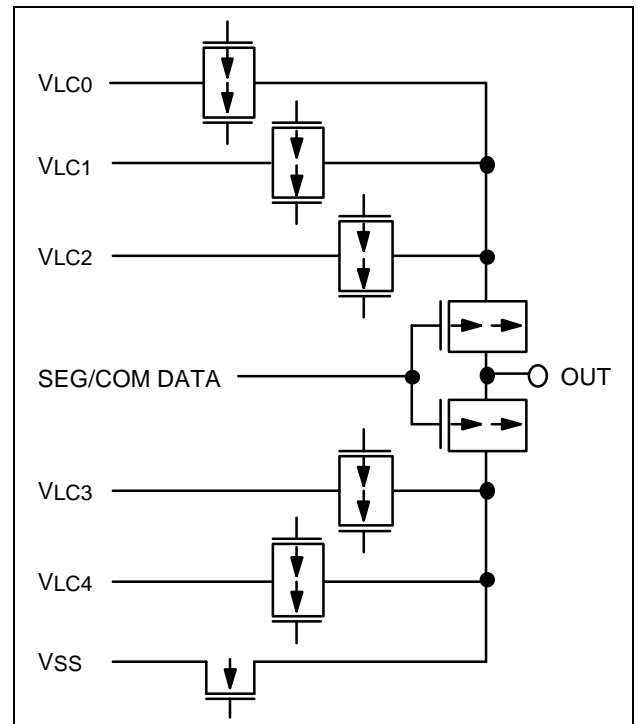

Figure 1-4. Pin Circuit Type B

Figure 1-6. Pin Circuit Type H-6

NOTES

13 ELECTRICAL DATA

OVERVIEW

In this section, information on KS57C2916 electrical characteristics is presented as tables and graphics.
The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings

— D.C. electrical characteristics

— Main system clock oscillator characteristics

— Subsystem clock oscillator characteristics

— I/O capacitance

— A.C. electrical characteristics

— Operating voltage range

Miscellaneous Timing Waveforms

— A.C timing measurement point

— Clock timing measurement at X_{in}

— Clock timing measurement at XT_{in}

— TCL timing

— Input timing for RESET

— Input timing for external interrupts

— Serial data transfer timing

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode

— Stop mode release timing when initiated by RESET

— Stop mode release timing when initiated by an interrupt request

Table 13-1. Absolute Maximum Ratings

(T_A = 25 $^{\circ}$C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 4.5	V
Input Voltage	V_I	Ports 0, 1	– 0.3 to VDD + 0.3	V
Output Voltage	V_O	–	– 0.3 to VDD + 0.3	V
Output Current High	I_{OH}	One I/O pin active	– 15	mA
		All I/O pins active	– 30	
Output Current Low	I_{OL}	One I/O pin active	+ 30 (Peak value)	mA
			+ 15[(note)]	
		Total for pins 0, 1	+ 100 (Peak value)	
			+ 60[(note)]	
Operating Temperature	T_A	–	– 40 to + 85	$^{\circ}$C
Storage Temperature	T_{stg}	–	– 65 to + 150	$^{\circ}$C

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 13-2. D.C. Electrical Characteristics

(T_A = – 40 $^{\circ}$C to + 85 $^{\circ}$C, V_{DD} = 2.2 V to 3.4 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	Ports 0, 1, and RESET	$0.8V_{DD}$	–	V_{DD}	V
	V_{IH2}	X_{in}, X_{out}, and XT_{in}	$V_{DD} - 0.1$		V_{DD}	
Input Low Voltage	V_{IL1}	Ports 0, 1, and RESET	–	–	$0.2V_{DD}$	V
	V_{IL2}	X_{in}, X_{out}, and XT_{in}			0.1	
Output High Voltage	V_{OH}	V_{DD} = 2.2 V to 3.4 V I_{OH} = – 1 mA Ports 0, 1	$V_{DD} - 1.0$	–	–	V
Output Low Voltage	V_{OL}	V_{DD} = 2.2 V to 3.4 V I_{OL} = 5 mA Ports 0, 1	–	–	1.0	V

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Table 13-2. D.C. Electrical Characteristics (Continued)

$(T_A = -40\ ^{\circ}C$ to $+85\ ^{\circ}C$, $V_{DD} = 2.2$ V to 3.4 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Leakage Current	I_{LIH1}	$V_I = V_{DD}$ All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	$V_I = V_{DD}$ X_{in}, X_{out} and XT_{in}			20	
Input Low Leakage Current	I_{LIL1}	$V_I = 0$ V All input pins except RESET X_{in}, X_{out} and XT_{in}	–	–	– 3	µA
	I_{LIL2}	$V_I = 0$ V RESET, X_{in}, X_{out} and XT_{in}			– 20	
Output High Leakage Current	I_{LOH}	$V_O = V_{DD}$ All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	$V_O = 0$ V All output pins	–	–	– 3	µA
Pull-Up Resistor	R_{L1}	$V_I = 0$ V; $V_{DD} = 3$V Ports 0, 1	50	100	200	kΩ
	R_{L2}	$V_I = 0$ V; $V_{DD} = 3$V; RESET	200	450	800	
LCD Voltage Dividing Resistor [1]	R_{LCD1}	Ta = + 25 °C	50	100	150	kΩ
	R_{LCD2}	Ta = + 25 °C	25	50	75	
$\lvert V_{DD}\text{-}COMi \rvert$ Voltage Drop (i = 0–15)	V_{DC}	$V_{LCD} = 3.0$ V – 15 µA per common pin	–	–	120	mV
$\lvert V_{LCD}\text{-}SEGx \rvert$ Voltage Drop (x = 0–43)	V_{DS}	$V_{LCD} = 3.0$ V – 15 µA per common pin	–	–	120	
Middle Output Voltage [2]	V_{LC0}	$V_{LC0} = 5.0$ V	V_{LC0}-0.2	V_{LC0}	V_{LC0}+0.2	V
	V_{LC1}		$0.8V_{LC0}$-0.2	$0.8V_{LC0}$	$0.8V_{LC0}$+0.2	
	V_{LC2}		$0.6V_{LC0}$-0.2	$0.6V_{LC0}$	$0.6V_{LC0}$+0.2	
	V_{LC3}		$0.4V_{LC0}$-0.2	$0.4V_{LC0}$	$0.4V_{LC0}$+0.2	
	V_{LC4}		$0.2V_{LC0}$-0.2	$0.2V_{LC0}$	$0.2V_{LC0}$+0.2	

NOTES:
1. RLCD1 is LCD voltage dividing resistor when LCON.2 = "0", and RLCD2 when LCON.2 = "1".
2. It is middle output voltage when 1/16 duty and 1/5 bias.

Table 13-2. D.C. Electrical Characteristics (Concluded)
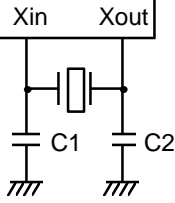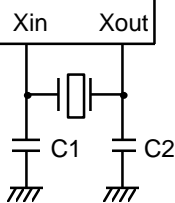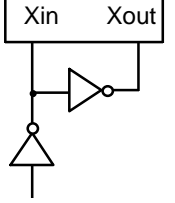
$(T_A = -40\,°C \text{ to } +85\,°C, V_{DD} = 2.2\ V \text{ to } 3.4\ V)$
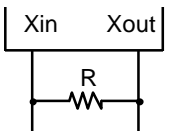
Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current [1]	I_{DD1}	V_{DD} = 3V ± 10% 4.19 MHz (PCON=3H) crystal oscillator C1 = C2 = 22 pF		–	1.3	3.0	mA
	I_{DD2}	Idle mode; V_{DD} = 3 V ± 10% 4.19 MHz (PCON=3H) crystal oscillator C1 = C2 = 22 pF			0.4	1.0	
	I_{DD3} [2]	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	15	30	µA
	I_{DD4} [2]	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator			5	15	
	I_{DD5}	Stop mode; V_{DD} = 3 V ± 10%	SCMOD=0000B, XTin=0V		0.5	3	
		Stop mode; V_{DD} = 3 V ± 10%	SCMOD=0100B		0.2	2	

NOTES:

1. Current in the following circuits are not included; on-chip pull-up resistors, internal LCD voltage dividing resistors, voltage doubler, and output port drive currents.
2. Data includes power consumption for subsystem clock oscillation.
3. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.

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Table 13-3. Main System Clock Oscillator Characteristics

(T_A = $-40\ ^\circ C$ to $+85\ ^\circ C$, V_{DD} = 2.2 V to 3.4 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator	Xin Xout C1 C2	Oscillation frequency (1)	–	0.4	–	4.19	MHz
		Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range; V_{DD} = 3.0 V	–	–	4	ms
Crystal Oscillator	Xin Xout C1 C2	Oscillation frequency (1)	–	0.4	–	4.19	MHz
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	10	ms
External Clock	Xin Xout	X_{in} input frequency (1)	–	0.4	–	4.19	MHz
		X_{in} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns
RC Oscillator	Xin Xout R	Frequency	V_{DD} = 3 V	0.4	–	1.5	MHz

NOTES:

1. Oscillation frequency and X_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when stop mode is terminated.

Table 13-4. Recommended Oscillator Constants

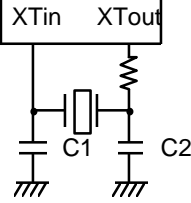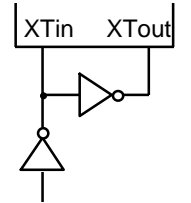(T_A = − 40 °C to + 85 °C, V_{DD} = 2.2 V to 3.4 V)

Manufacturer	Series Number [1]	Frequency Range	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
			C1	C2	MIN	MAX	
TDK	FCR ðÿM5	3.58 MHz–4.2 MHz	33	33	2.2	3.4	Leaded Type
	FCR ðÿMC5	3.58 MHz–4.2 MHz	(2)	(2)	2.2	3.4	On-chip C Leaded Type
	CCR ðÿMC3	3.58 MHz–4.2 MHz	(3)	(3)	2.2	3.4	On-chip C SMD Type

NOTES:
1. Please specify normal oscillator frequency.
2. On-chip C: 30pF built in.
3. On-chip C: 38pF built in.

Table 13-5. Subsystem Clock Oscillator Characteristics

(T_A = − 40 °C to + 85 °C, V_{DD} = 2.2 V to 3.4 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency [1]	–	32	32.768	35	kHz
		Stabilization time [2]	V_{DD} = 2.2 V to 3.4 V	–	1.0	3	s
External Clock		XT_{in} input frequency [1]	–	32	–	100	kHz
		XT_{in} input high and low level width (t_{XTL}, t_{XTH})	–	5	–	15	μs

NOTES:
1. Oscillation frequency and XT_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs.

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Table 13-6. Input/Output Capacitance

($T_A = 25\ ^\circ$C, $V_{DD} = 0$ V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF

Table 13-7. Voltage Doubler Output

($T_A = -40\ ^\circ$C to $+ 85\ ^\circ$C, $V_{DD} = 2.2$ V to 3.4 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Voltage Doubler Output	Vbias	$V_{DD} = 2.2$ V to 3.4 V	–	2 V_{DD}	–	V

Table 13-8. A.C. Electrical Characteristics

($T_A = -40\ ^\circ$C to $+ 85\ ^\circ$C, $V_{DD} = 2.2$ V to 3.4 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (note)	t_{CY}	$V_{DD} = 2.2$ V to 3.4 V	0.95	–	64	µs
		With subsystem clock (fxt)	114	122	125	
Interrupt Input High, Low Width	f_{INTH}, f_{INTL}	INT0–INT2, INT4 K0–K3	10	–	–	
RESET Input Low Width	t_{RSL}	Input	10	–	–	

NOTE: Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock (fx) source.
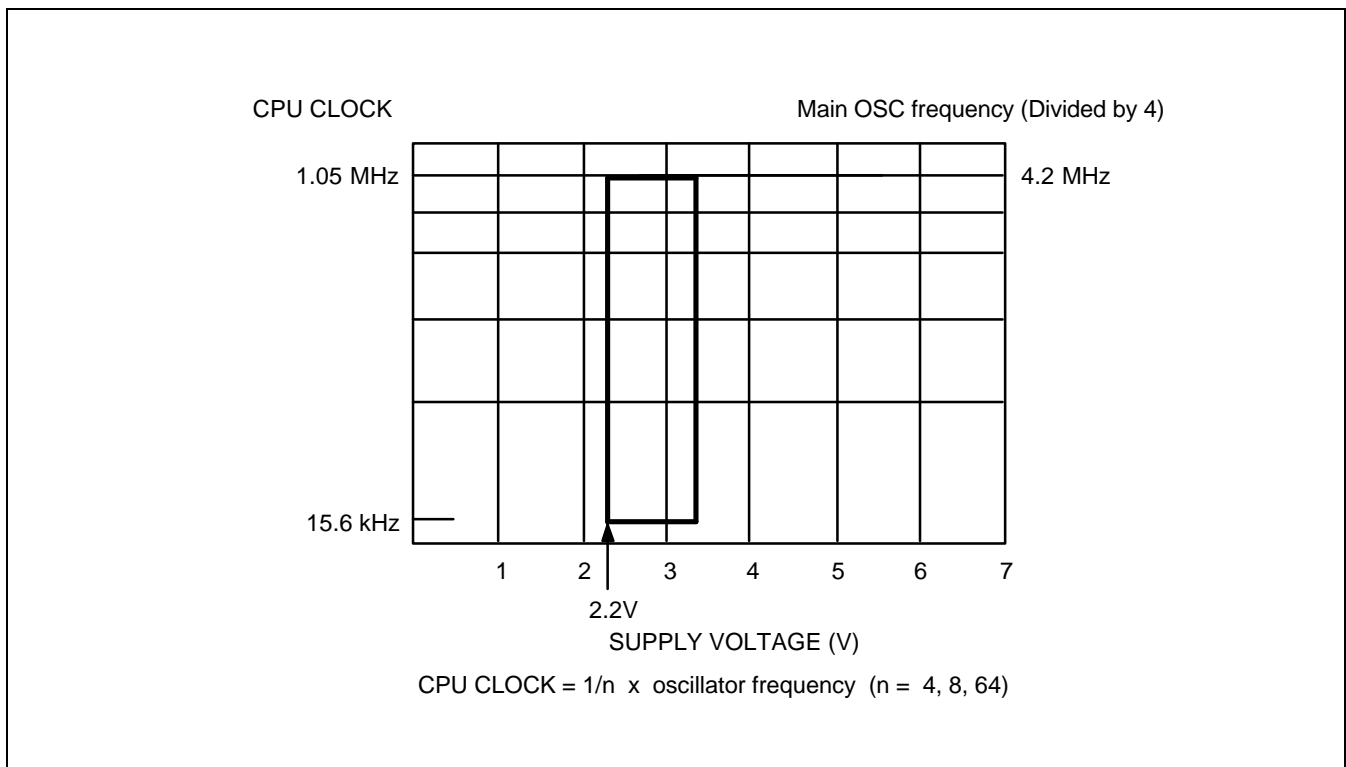
CPU CLOCK   Main OSC frequency (Divided by 4)

1.05 MHz   4.2 MHz

15.6 kHz

          1   2   3   4   5   6   7

                2.2V

                SUPPLY VOLTAGE (V)

CPU CLOCK = 1/n x oscillator frequency (n = 4, 8, 64)

Figure 13-1. Standard Operating Voltage Range

Table 13-9. RAM Data Retention Supply Voltage in Stop Mode

$(T_A = -40 \,^{\circ}C$ to $+85 \,^{\circ}C)$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	2.2	–	3.4	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.2 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time [1]	t_{WAIT}	Released by RESET	–	$2^{17}/fx$	–	ms
		Released by interrupt	–	(2)	–	

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

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TIMING WAVEFORMS
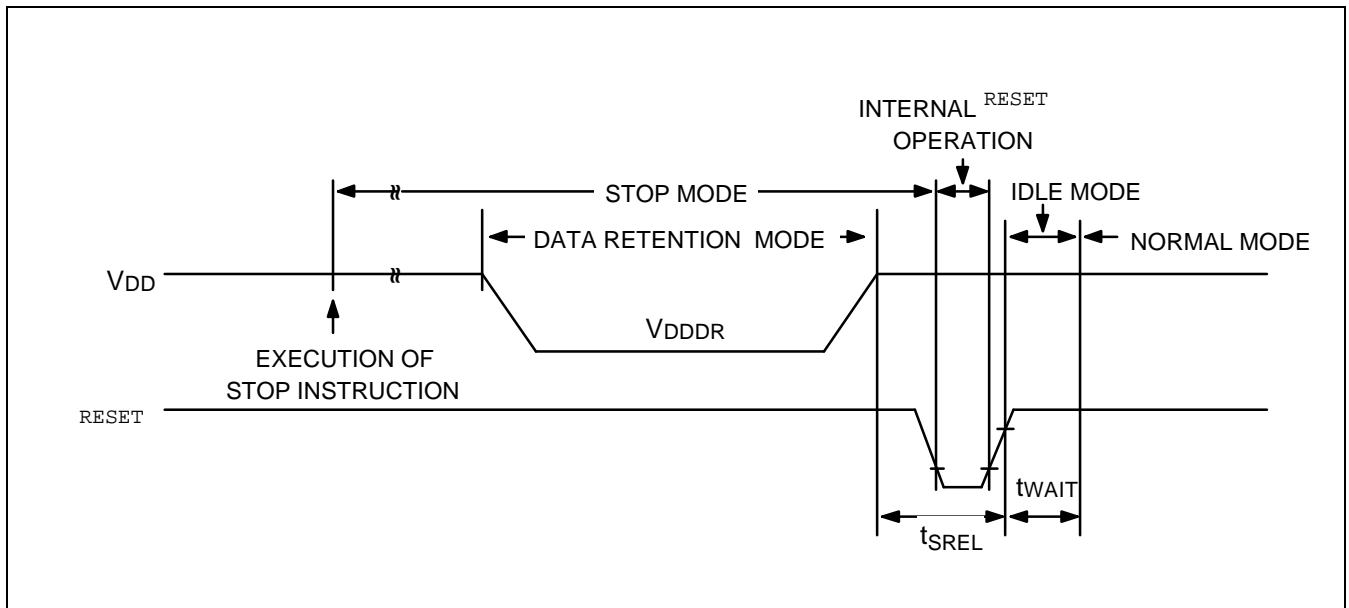
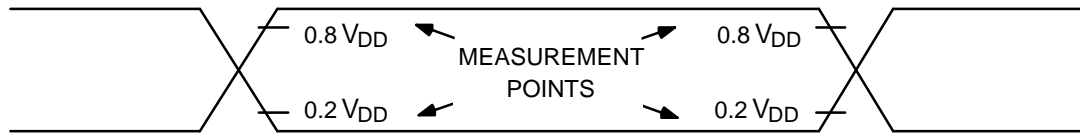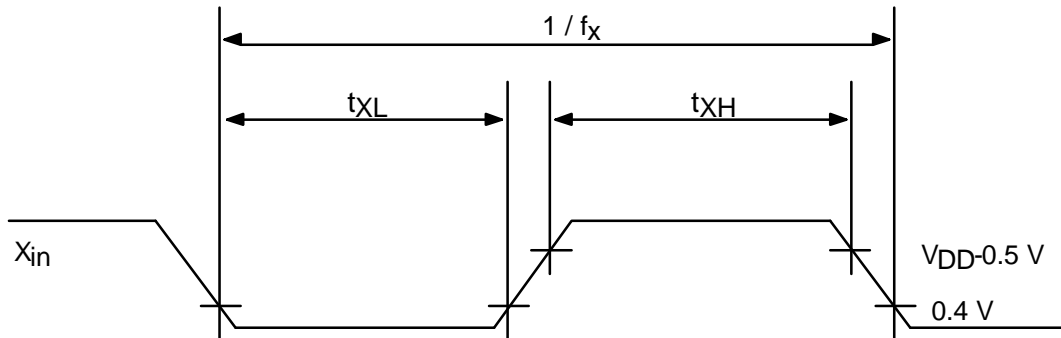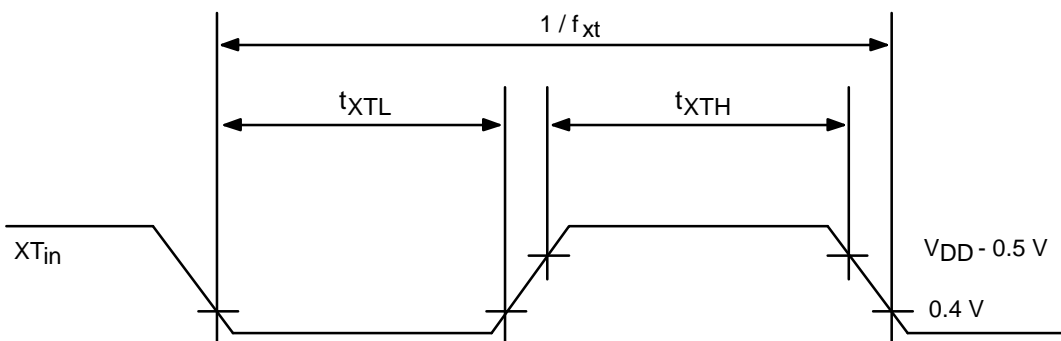**Figure 13-2. Stop Mode Release Timing When Initiated by RESET**
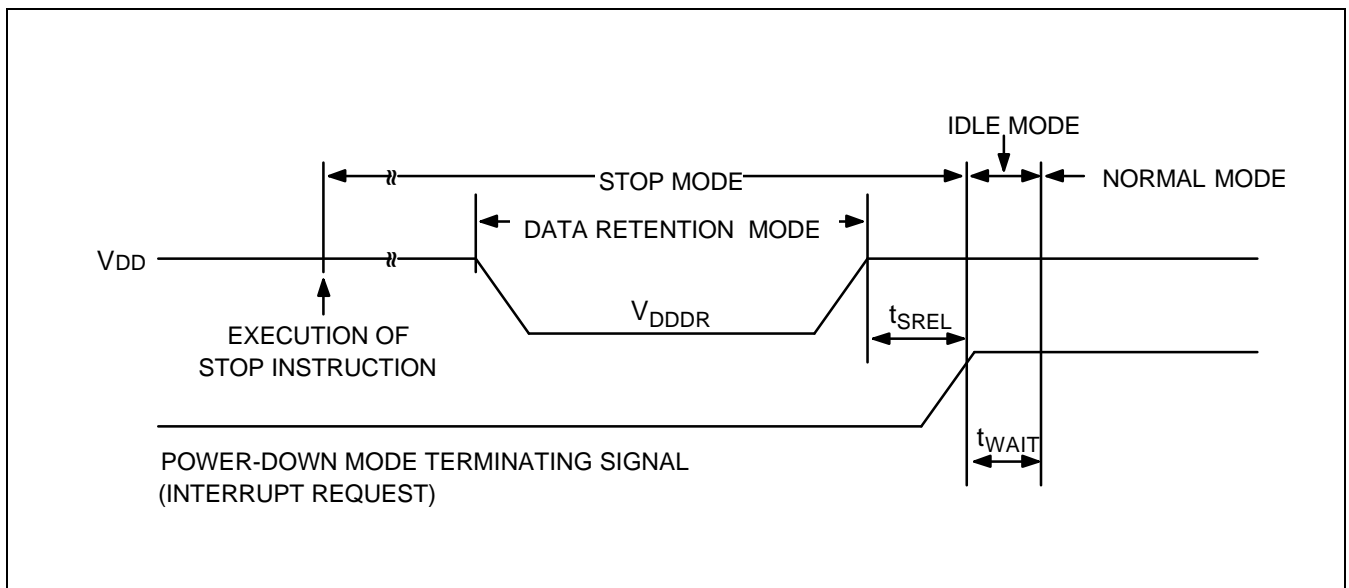
Figure 13-3. Stop Mode Release Timing When Initiated by Interrupt Request

Figure 13-4. A.C. Timing Measurement Points (Except for X$_{in}$ and XT$_{in}$)

Figure 13-5. Clock Timing Measurement at X$_{in}$
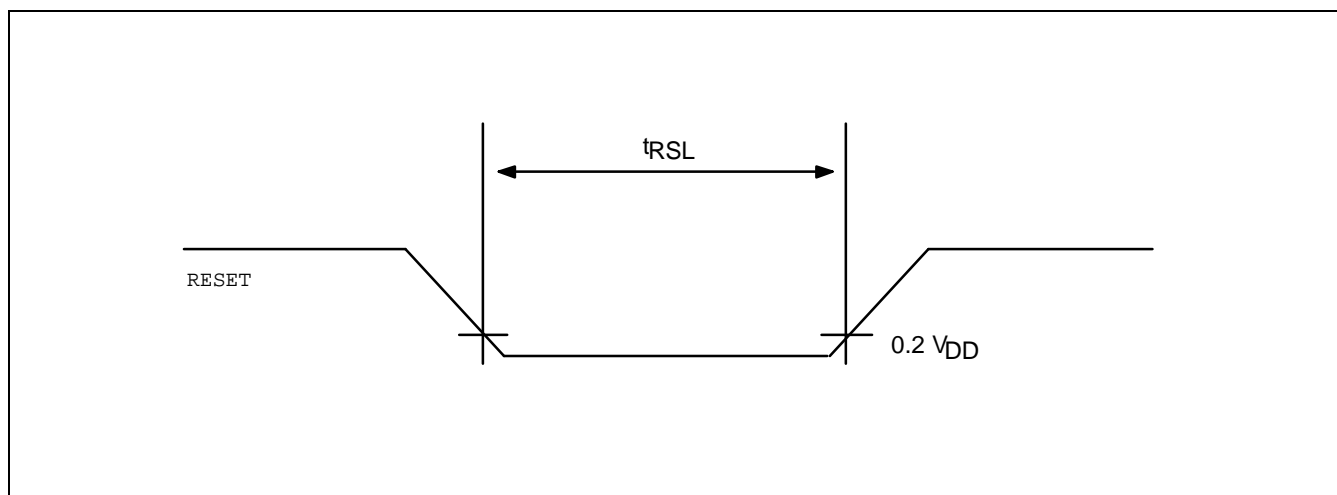

Figure 13-6. Clock Timing Measurement at XT$_{in}$

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Figure 13-7. Input Timing for RESET Signal
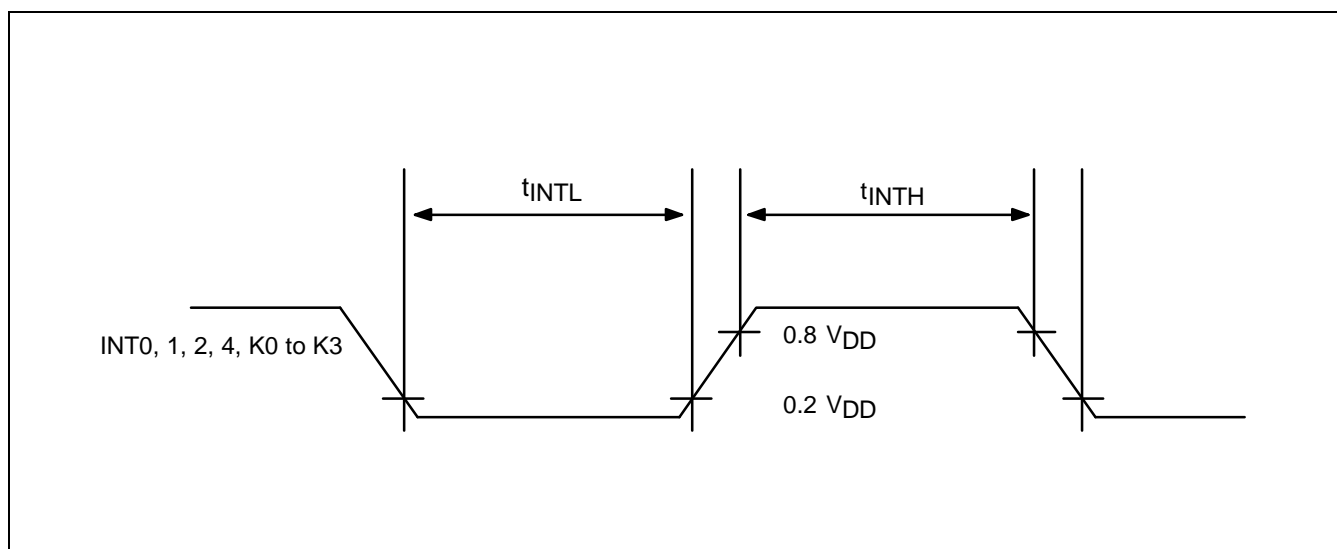
Figure 13-8. Input Timing for External Interrupts

NOTES

CHARACTERISTIC CURVES

NOTE

The characteristic values shown in the following graphs are based on actual test measurements.

They do not, however, represent guaranteed operating values.
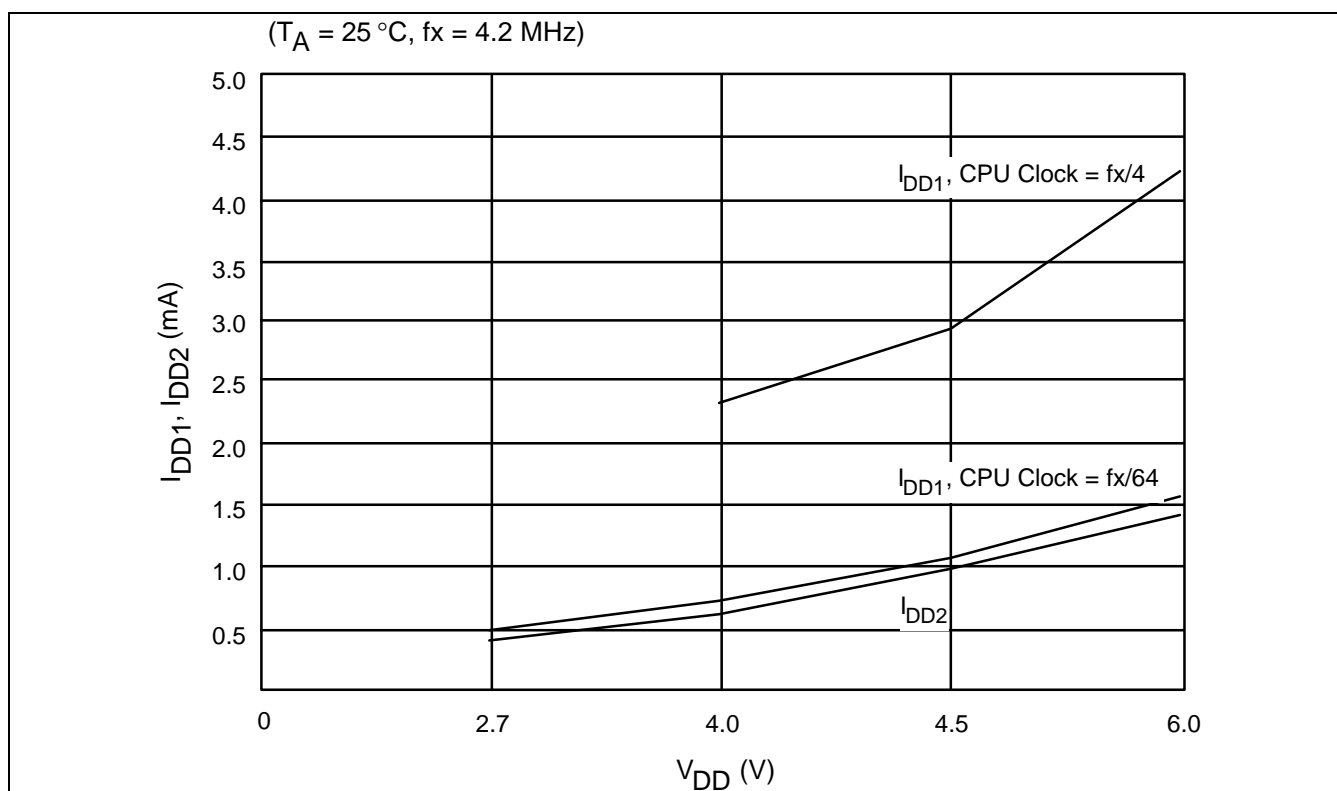
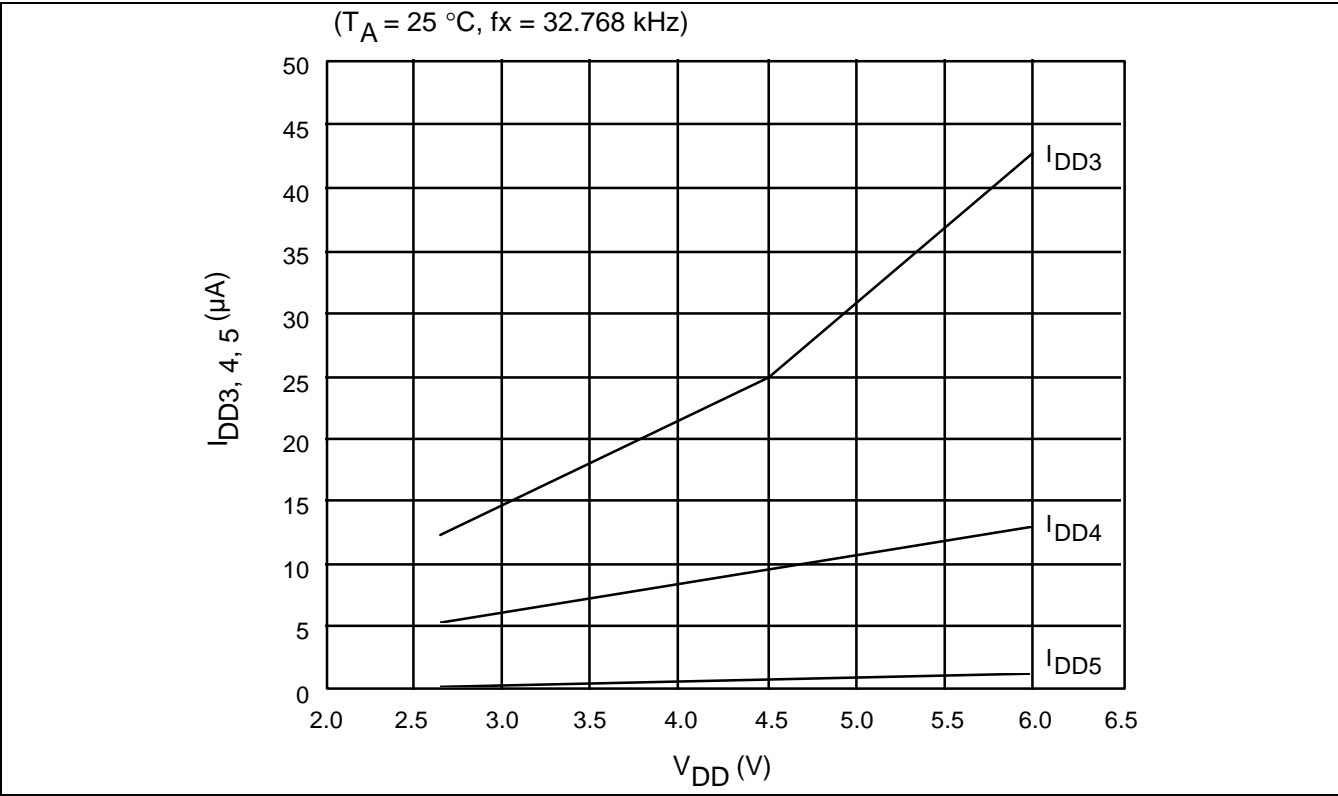

Figure 13-11. I_{DD1}, I_{DD2} VS. V_{DD}

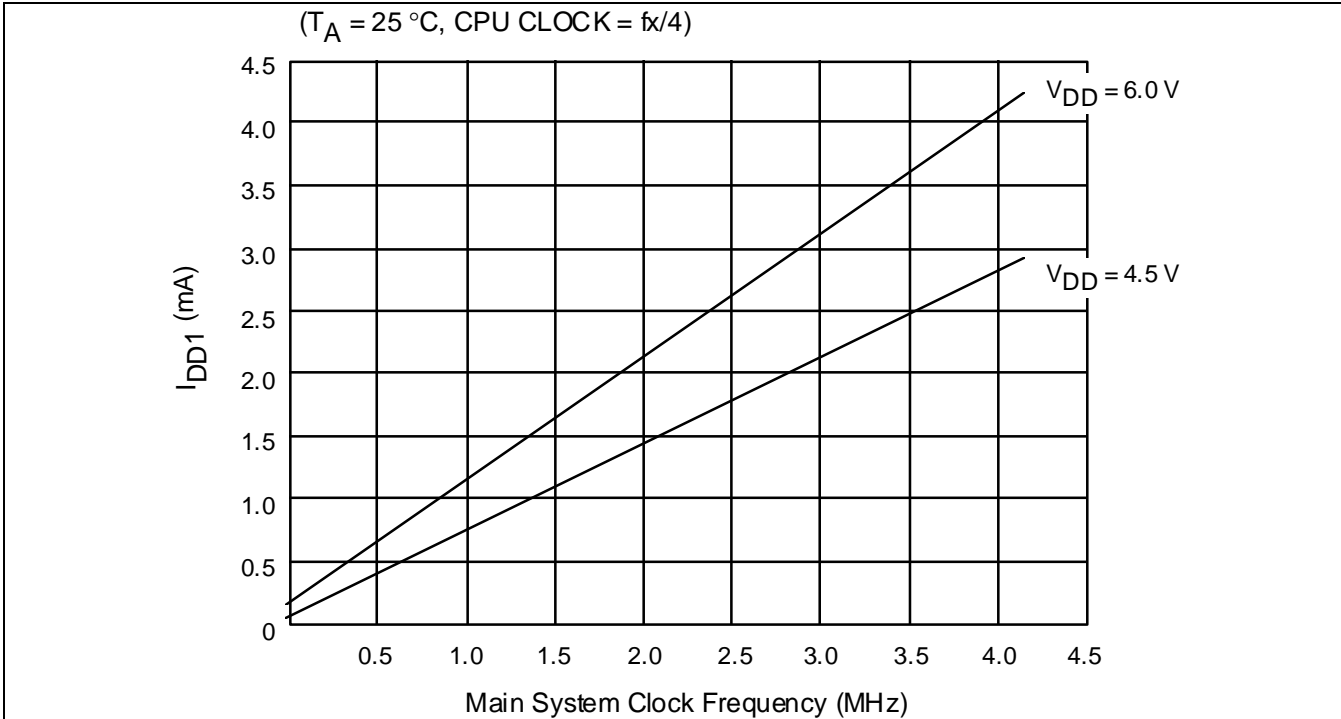**Figure 13-12. I_{DD3}, I_{DD4}, I_{DD5} VS. V_{DD}**

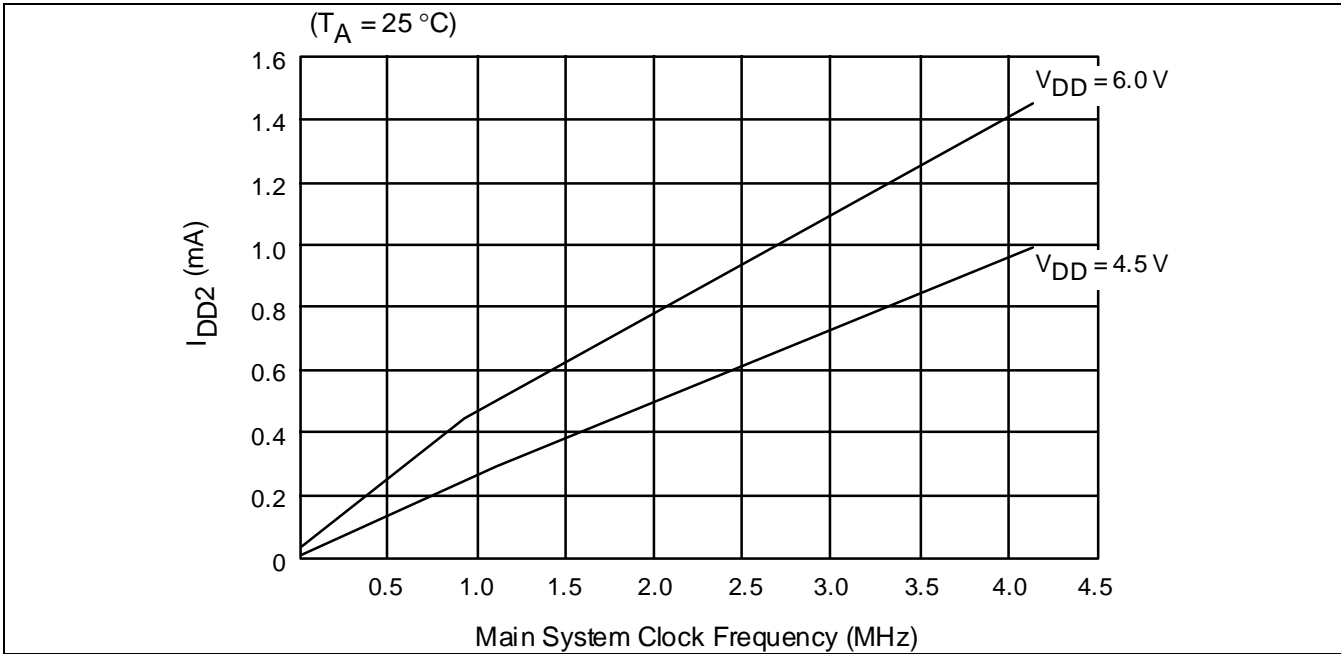**Figure 13-13. I_{DD1} VS. Main System Clock Frequency**

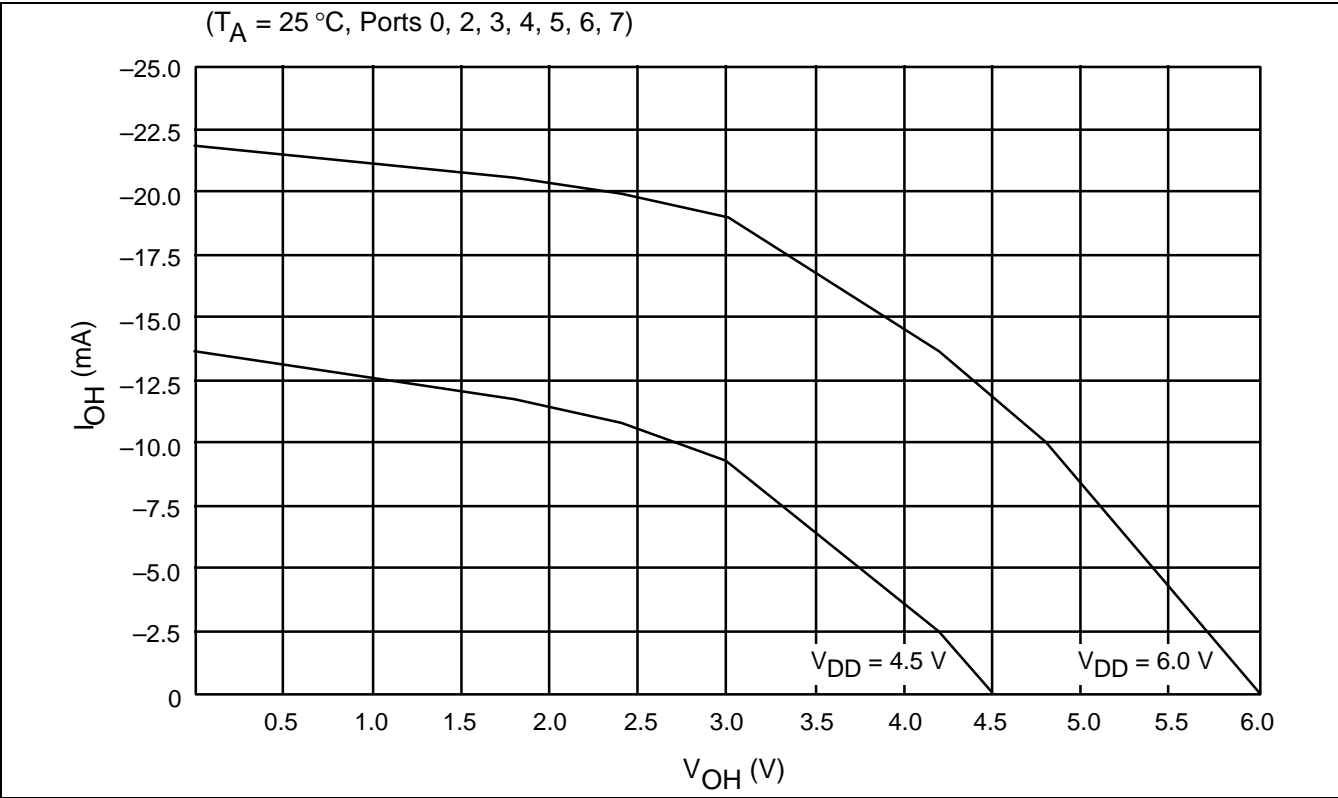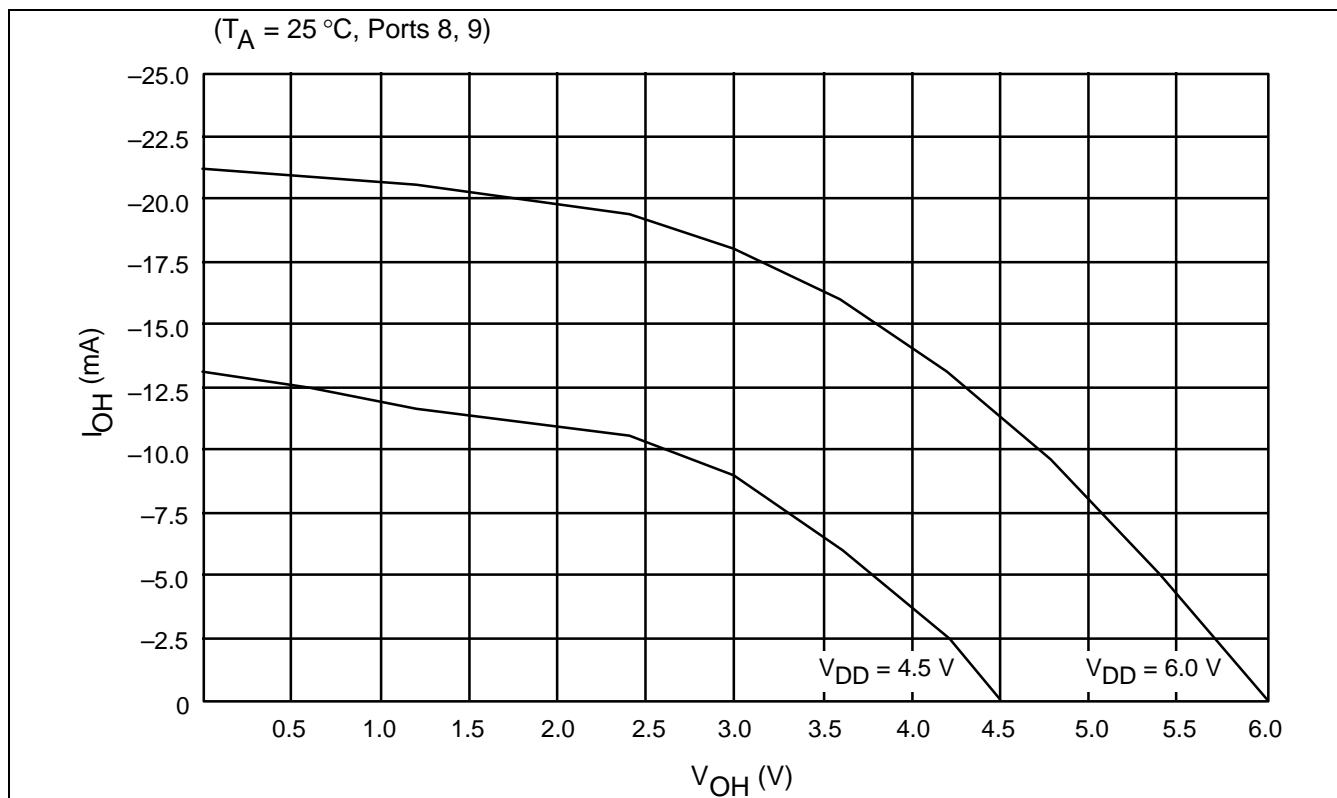**Figure 13-13. I_{DD2} VS. Main System Clock Frequency**

Figure 13–15. I_{OH} VS. V_{OH} (P0, 2, 3, 4, 5, 6, 7)

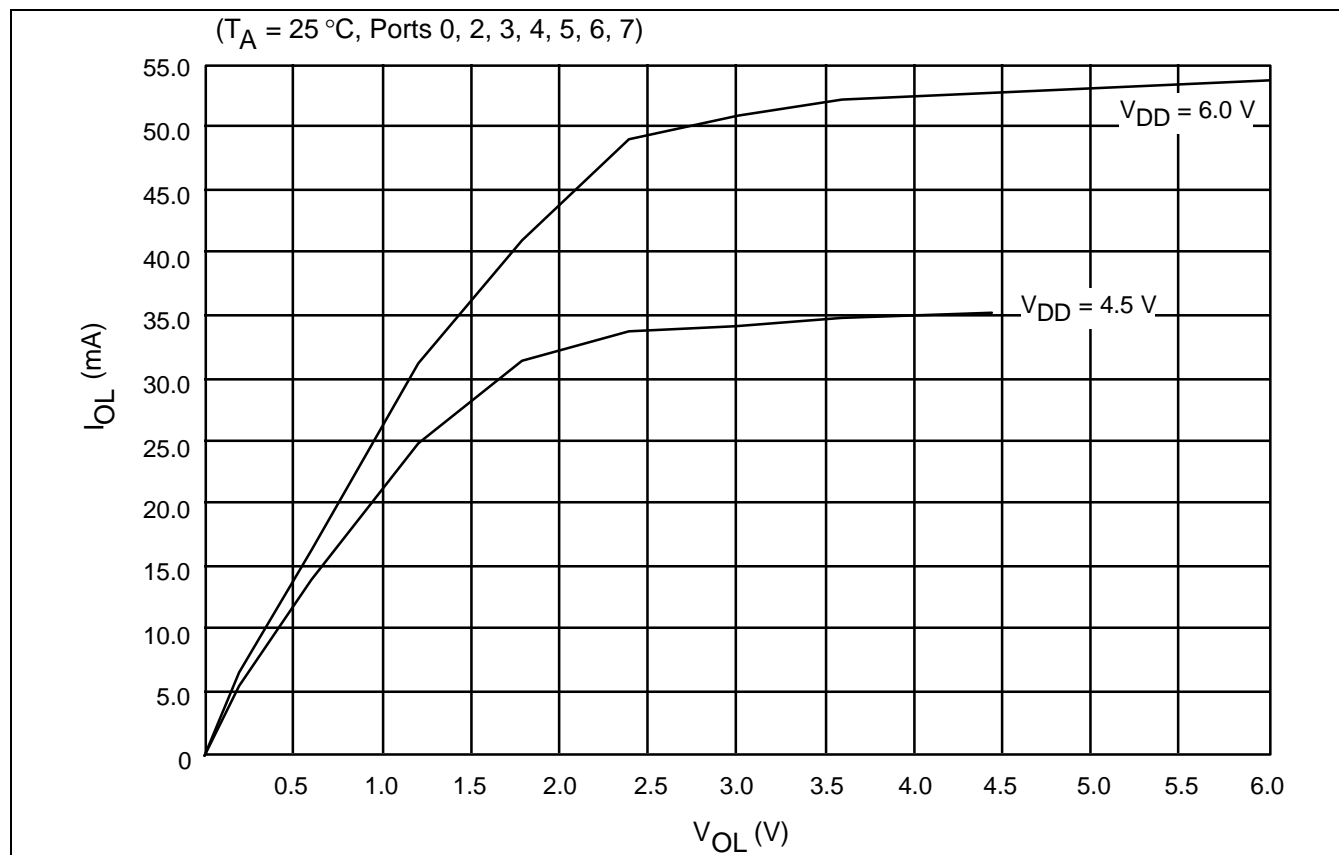**Figure 13–16. I$_{OH}$ VS. V$_{OH}$ (P8, 9)**

$(T_A = 25 °C, \text{Ports } 0, 2, 3, 4, 5, 6, 7)$

Figure 13–17. I_{OL} VS. V_{OL} (P0, 2, 3, 4, 5, 6, 7)

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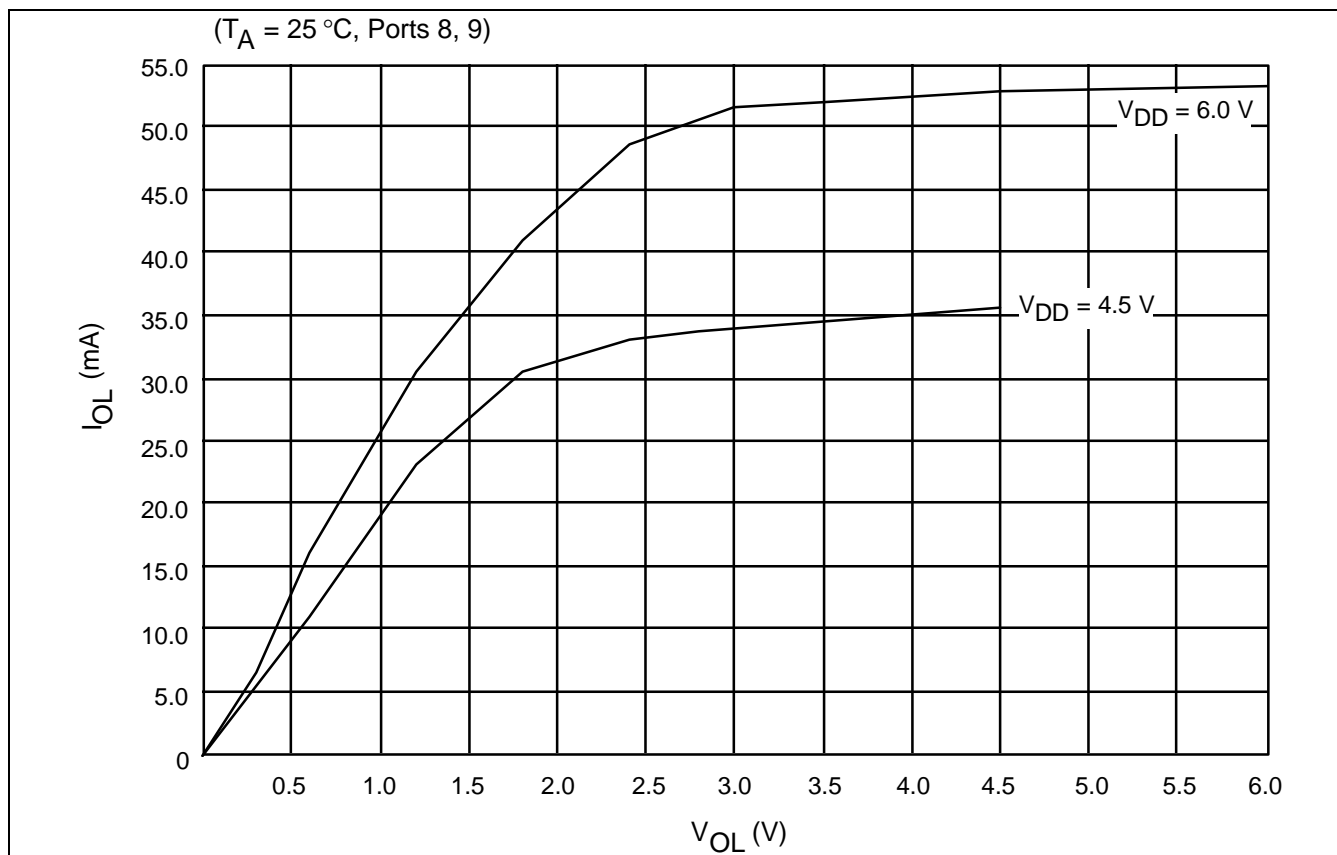
Figure 13–18. I$_{OL}$ VS. V$_{OL}$ (P8, 9)

NOTES

14 MECHANICAL DATA

OVERVIEW

This section contains the following information about the device package:

— Package dimensions in millimetersD

— Pad diagram

— Pad/pin coordinate data table

NOTES
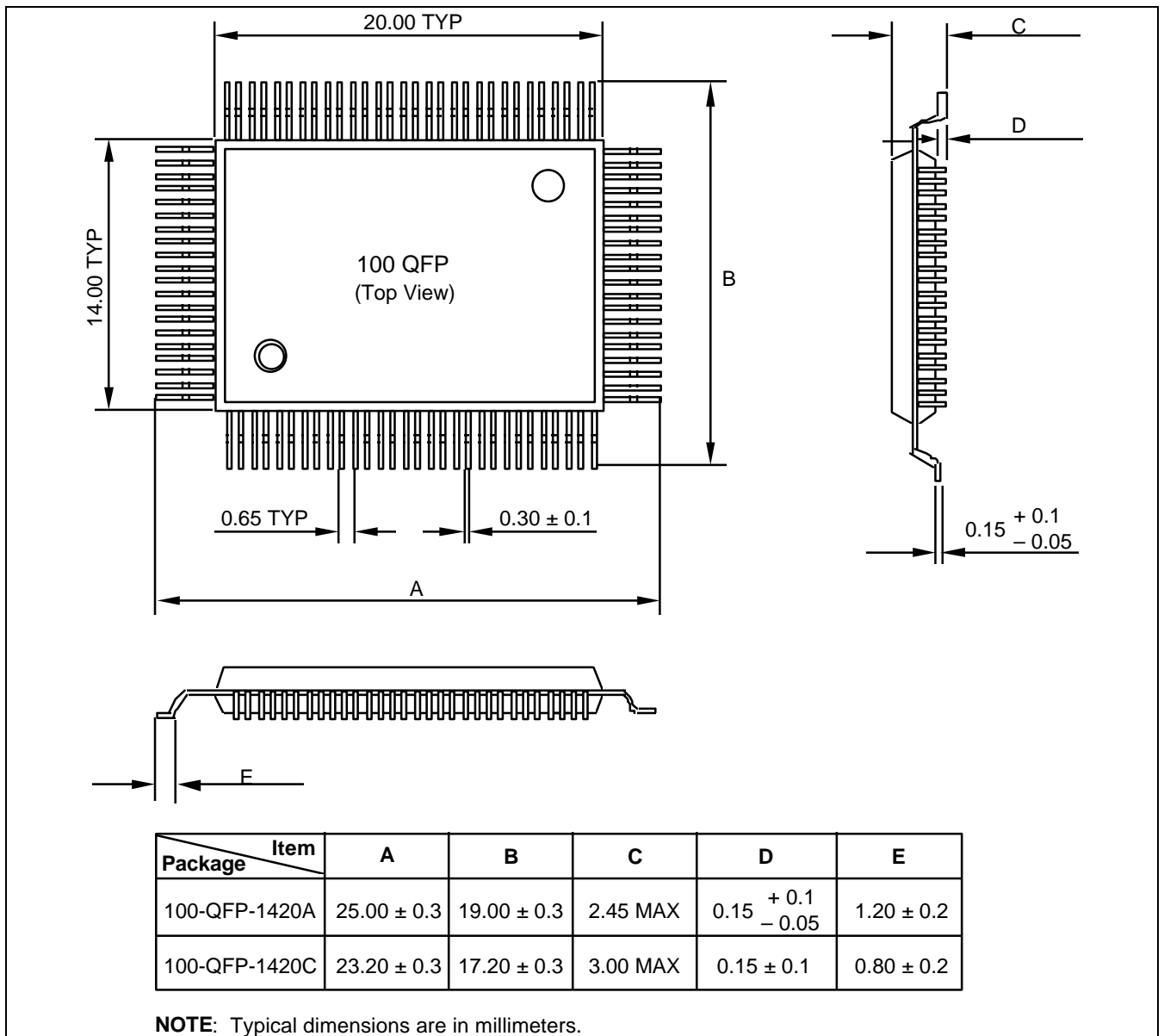
Figure 14-1. 100-QFP Package Dimensions

Package \ Item	A	B	C	D	E
100-QFP-1420A	25.00 ± 0.3	19.00 ± 0.3	2.45 MAX	$0.15 \begin{smallmatrix} +0.1 \\ -0.05 \end{smallmatrix}$	1.20 ± 0.2
100-QFP-1420C	23.20 ± 0.3	17.20 ± 0.3	3.00 MAX	0.15 ± 0.1	0.80 ± 0.2

NOTE: Typical dimensions are in millimeters.

15 **KS57P2916 OTP**

OVERVIEW

The KS57P2916 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS57C2916 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The KS57P2916 is fully compatible with the KS57C2916, both in function and in pin configuration. Because of its simple programming requirements, the KS57P2916 is ideal for use as an evaluation chip for the KS57C2916.
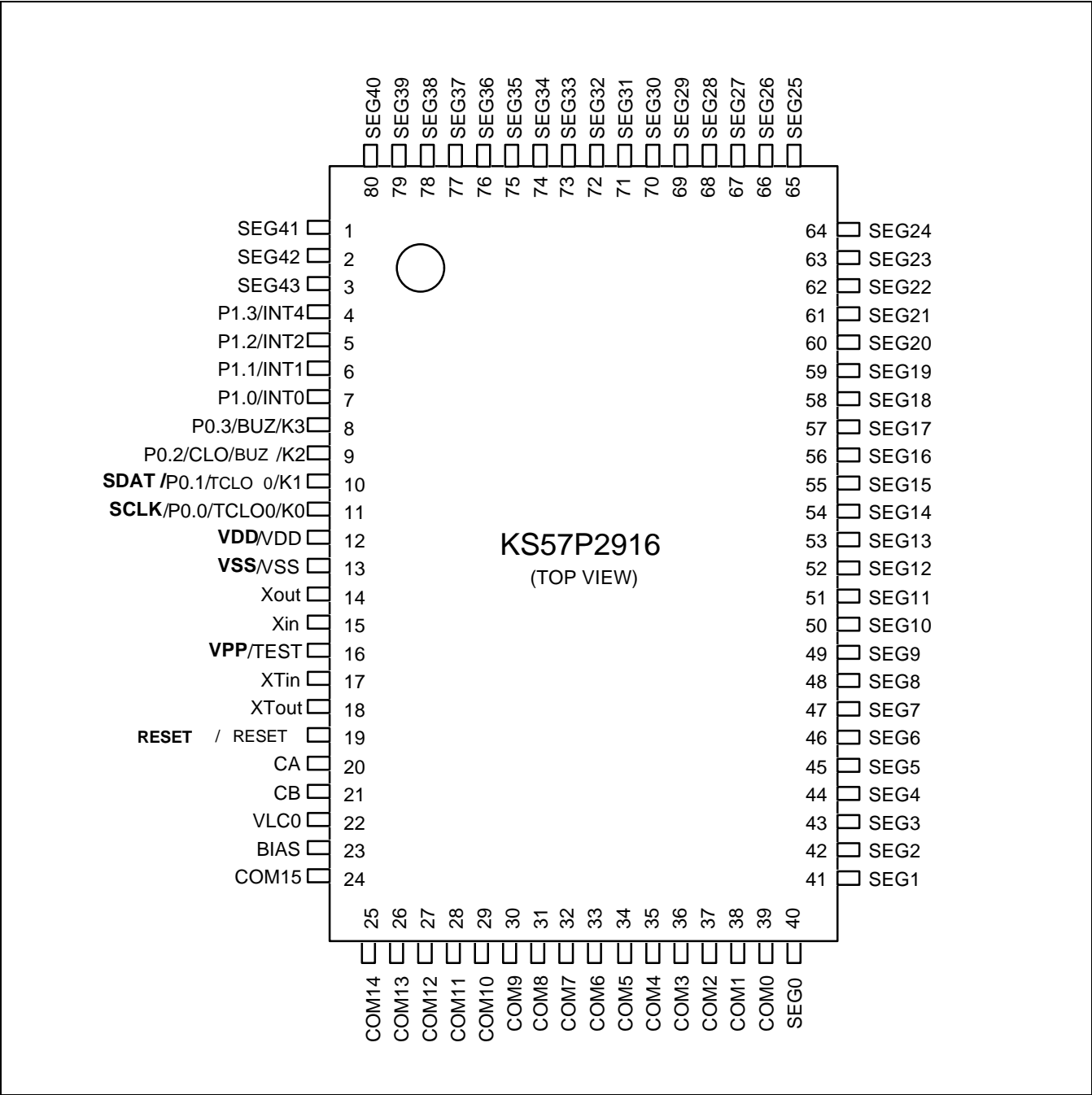
Figure 15-1. KS57P2916 Pin Assignments (80-QFP Package)

Table 15-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P0.1	SDAT	10	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P0.0	SCLK	11	I/O	Serial clock pin. Input only pin.
TEST	V_{PP}(TEST)	16	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	19	I	Chip initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	12/13	I	Logic power supply pin. VDD should be tied to +5 V during programming.

Table 15-2. Comparison of KS57P2916 and KS57C2916 Features

Characteristic	KS57P2916	KS57C2916
Program Memory	16 Kbyte EPROM	16 Kbyte mask ROM
Operating Voltage (V_{DD})	2.2 V to 3.4 V	2.2 V to 3.4 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP}(TEST)=12.5V	
Pin Configuration	80 QFP	80 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP}(TEST) pin of the KS57P2916, the EPROM programming mode is entered.

The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 15–3 below.

Table 15-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/MEM	Address (A15–A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

**NOTE**:   "0" means Low level; "1" means High level.

Table 15-4. D.C. Electrical Characteristics

(T_A = − 40 °C to + 85 °C, V_{DD} = 2.2 V to 3.4 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	IDD1	V_{DD} = 3V ± 10% 4.19 MHz (PCON=3H) crystal oscillator C1 = C2 = 22 pF		−	1.3	3.0	mA
	IDD2	Idle mode; V_{DD} = 3 V ± 10% 4.19 MHz (PCON=3H) crystal oscillator C1 = C2 = 22 pF			0.4	1.0	
	IDD3 (2)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		−	15	30	µA
	IDD4 (2)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator			5	15	
	IDD5	Stop mode; V_{DD} = 3 V ± 10%	SCMOD=0000B, XTin=0V		0.5	3	
		Stop mode; V_{DD} = 3 V ± 10%	SCMOD=0100B		0.2	2	

NOTES:

1. Data includes power consumption for subsystem clock oscillation.
2. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.
3. Current in the following circuits are not included; on-chip pull-up resistors, internal LCD voltage dividing resistors, voltage doubler, and output port drive currents.
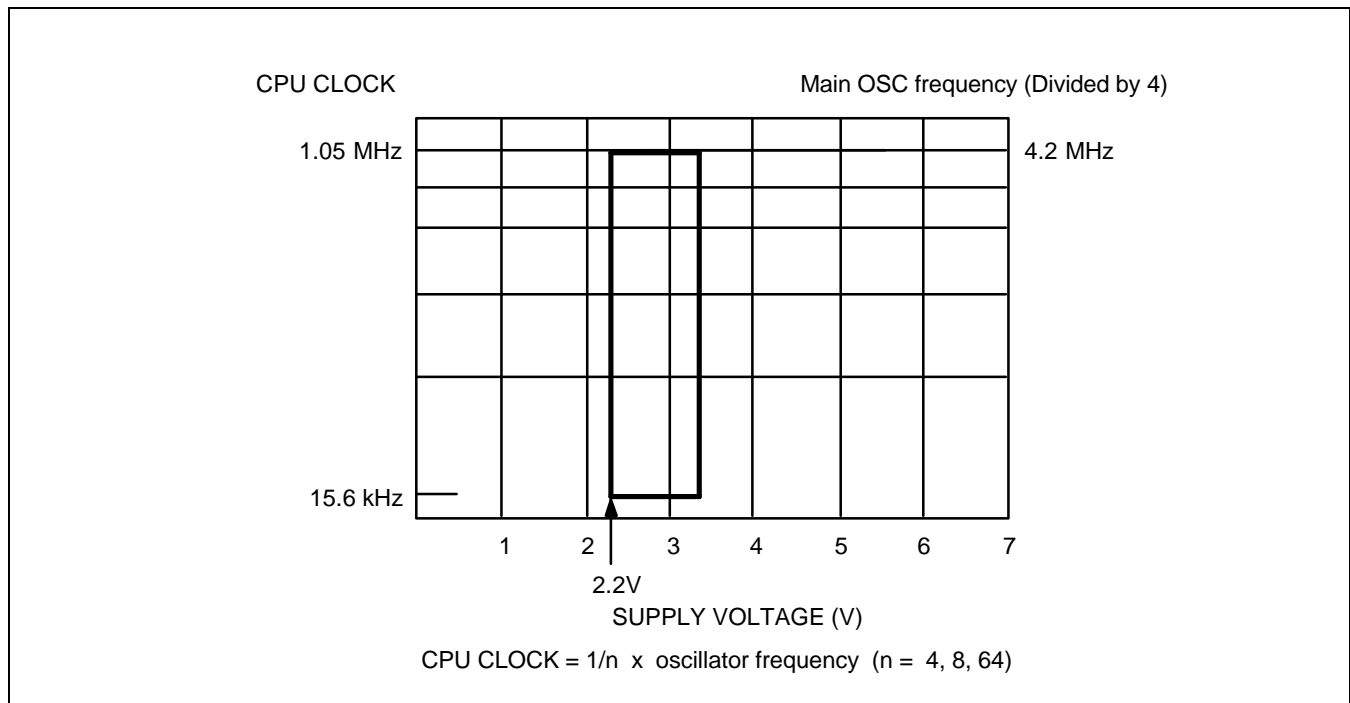
Figure 15-2. Standard Operating Voltage Range

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