1 PRODUCT OVERVIEW

OVERVIEW

The KS57C0616 single-chip CMOS microcontroller has been designed for high-performance using SAM 47 (Samsung Arrangeable Microcontrollers). SAM 47, Samsung's newest 4-bit CPU core is notable for its low energy consumption and low operating voltage.

Up to 36 pins of the available 42-SDIP and 44-QFP packages can be dedicated to I/O, and six vectored interrupts provide fast response to internal and external events.

In addition, the advanced CMOS technology of KS57C0616 provides for low power consumption and a wide operating voltage range.

OTP

The KS57C0616 microcontroller is also available in OTP (One Time Programmable) version, KS57P0616. The KS57P0616 microcontroller has an on-chip 16-Kbyte one-time-programmable EPROM instead of masked ROM. The main features of KS57P0616 and KS57C0616 is same except ROM type.

FEATURES SUMMARY

Memory

- 1 K × 4-bit RAM
- 16 K × 8-bit ROM

36 I/O Pins

- Input only: 4 pins
- I/O: 24 pins
- N-channel open-drain I/O: 8 pins

Memory-Mapped I/O Structure

- Data memory bank 15

8-Bit Basic Timer

- Programmable interval timer
- Watchdog timer

Two 8-Bit Timer/Counters

- Programmable 8-bit timer
- External event counter function
- Arbitrary clock frequency output

Watch Timer

- Real-time and interval time measurement
- Four frequency outputs to the BUZ pin

Bit Sequential Carrier

- Supports 8-bit serial data transfer in arbitrary format

Interrupts

- 3 external interrupt vectors
- 3 internal interrupt vectors
- 2 quasi-interrupts

Power-Down Modes

- Idle: Only CPU clock stops
- Stop: System clock stops

Oscillation Sources

- Crystal, or ceramic for main system clock
- Main system clock frequency: 0.4–6.0 MHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, and 15.3 μs at 4.19 MHz
- 1.12, 2.23, 17.88 μs at 3.58 MHz
- 0.67, 1.33, 10.7 μs at 6.0 MHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V

Package Types

- 42 SDIP, 44 QFP

BLOCK DIAGRAM

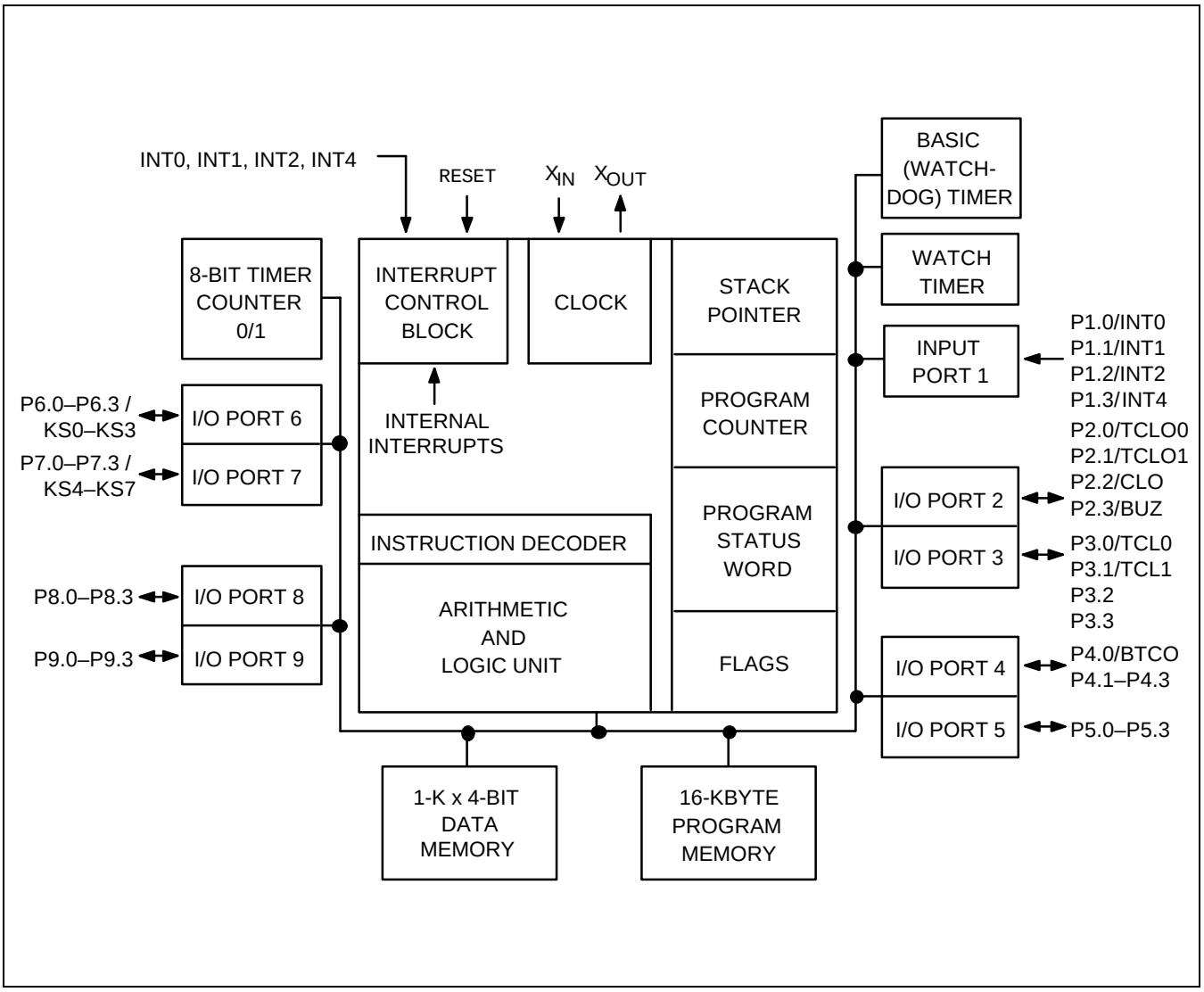


Figure 1-1. KS57C0616 Simplified Block Diagram

PIN ASSIGNMENTS

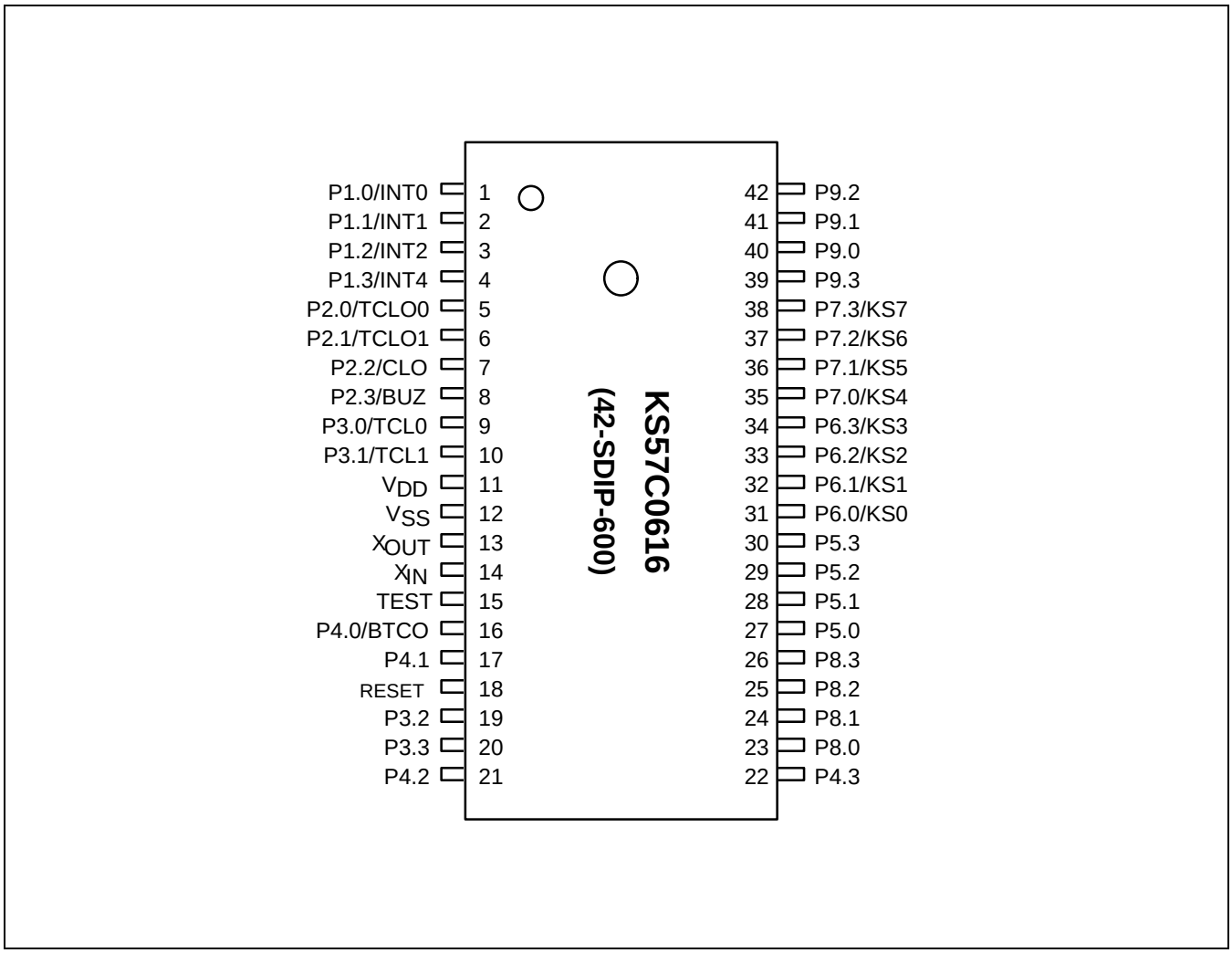


Figure 1-2. KS57C0616 Pin Assignment Diagrams (42-SDIP-600)

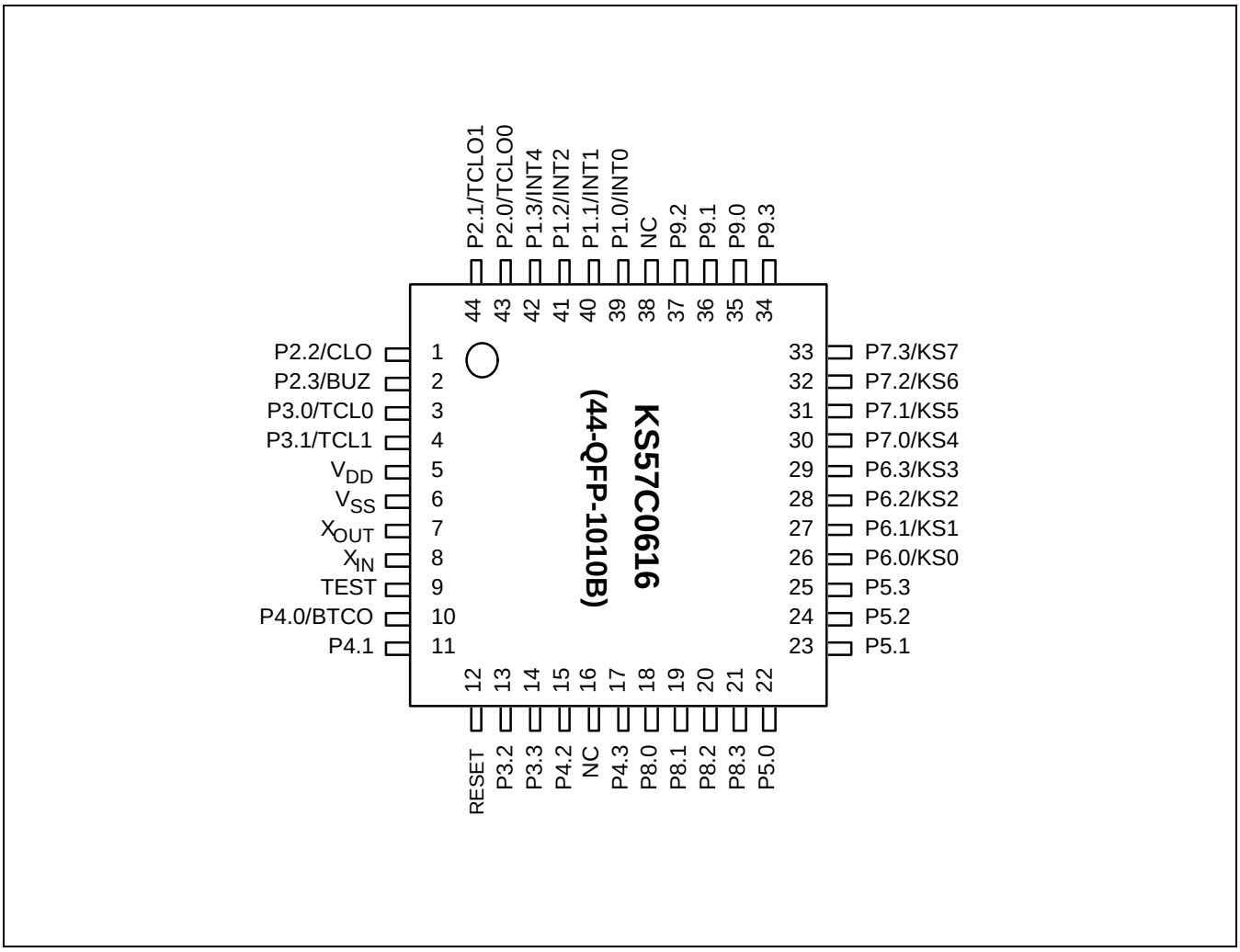


Figure 1-3. KS57C0616 Pin Assignment Diagrams (44-QFP-1010B)

PIN DESCRIPTIONS

Table 1-1. KS57C0616 Pin Descriptions

Pin Name	Pin Type	Description	Pin Number	Share Pin	Circuit Type
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. Each pull-up resistors are assignable by software.	1 (39) 2 (40) 3 (41) 4 (42)	INT0 INT1 INT2 INT4	A-4
P2.0 P2.1 P2.2 P2.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output.	5 (43) 6 (44) 7 (1) 8 (2)	TCLO0 TCLO1 CLO BUZ	D-2
P3.0 P3.1 P3.2 P3.3		4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. Ports 2 and 3 can be paired to enable 8-bit data transfer.	9 (3) 10 (4) 19 (13) 20 (14)	TCL0 TCL1	D-4
P4.0 P4.1 P4.2 P4.3 P5.0–P5.3	I/O	4-bit I/O ports. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. N-channel open-drain or push-pull output can be selected by software (1-bit unit). Ports 4 and 5 can be paired to enable 8-bit data transfer.	16 (10) 17 (11) 21 (15) 22 (17) 27–30 (22–25)	BTCO	E-2
P6.0–P6.3 P7.0–P7.3	I/O	4-bit I/O ports. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. Ports 6 and 7 can be paired to enable 8-bit data transfer.	31–34 (26–29), 35–38 (30–33)	KS0–KS3 KS4–KS7	D-4
P8.0–P8.3 P9.0–P9.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. Ports 8 and 9 can be paired to enable 8-bit data transfer.	23–26 (18–21), 40–42, 39 (35–37, 34)	–	D-2

Table 1-1. KS57C0616 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Pin Number	Share Pin	Circuit Type
INT0 INT1	I	External interrupt input. The triggering edge for INT0 and INT1 is selectable.	1 (39) 2 (40)	P1.0 P1.1	A-3
INT2	I	Quasi-interrupt input with detection of rising edge	3 (41)	P1.2	A-3
INT4	I	External interrupt with detection of rising and falling edge.	4 (42)	P1.3	A-3
TCLO0	I/O	Timer/counter 0 clock output	5 (43)	P2.0	D-2
TCLO1	I/O	Timer/counter 1 clock output	6 (44)	P2.1	D-2
CLO	I/O	Clock output	7 (1)	P2.2	D-2
BUZ	I/O	2, 4, 8, or 16 kHz frequency output for buzzer sound with 4.19 MHz system clock	8 (2)	P2.3	D-2
TCL0	I/O	External clock input for timer/counter 0	9 (3)	P3.0	D-4
TCL1	I/O	External clock input for timer/counter 1	10 (4)	P3.1	D-4
BTCO	I/O	Basic timer clock output	16 (10)	P4.0	E-2
KS0–KS3 KS4–KS7	I/O	Quasi-interrupt inputs with falling edge detection	31–34 (26–29) 35–38 (30–33)	P6.0–P6.3 P7.0–P7.3	D-4
V_{DD}	–	Power supply	11 (5)	–	–
V_{SS}	–	Ground	12 (6)	–	–
RESET	–	RESET signal	18 (12)	–	B
X_{IN} X_{OUT}	–	Crystal, or ceramic oscillator signal for main system clock. (For external clock input, use X_{IN} and input X_{IN}'s reverse phase to X_{OUT})	14 (8) 13 (7)	–	–
TEST	–	Test signal input	15 (9)	–	–
NC	–	No connection	(16, 38)	–	–

NOTE: Parentheses indicate pin number for 44 QFP package.

PIN CIRCUIT DIAGRAMS

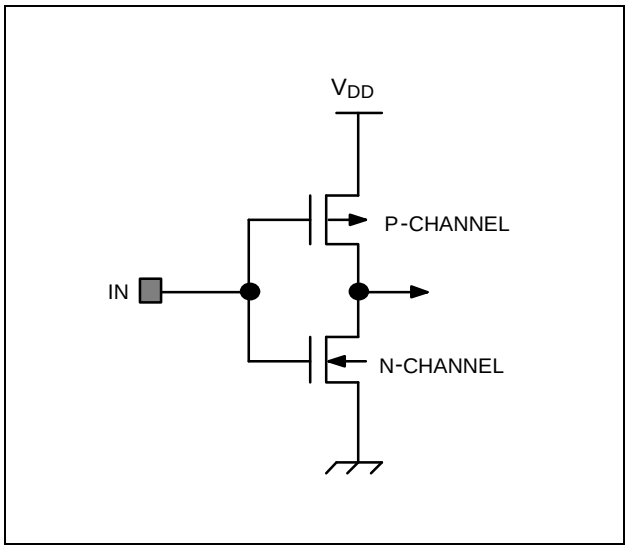


Figure 1-4. Pin Circuit Type A

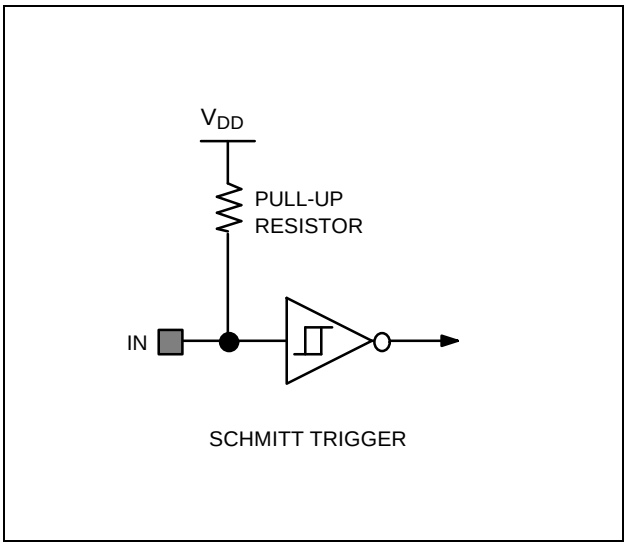


Figure 1-6. Pin Circuit Type B

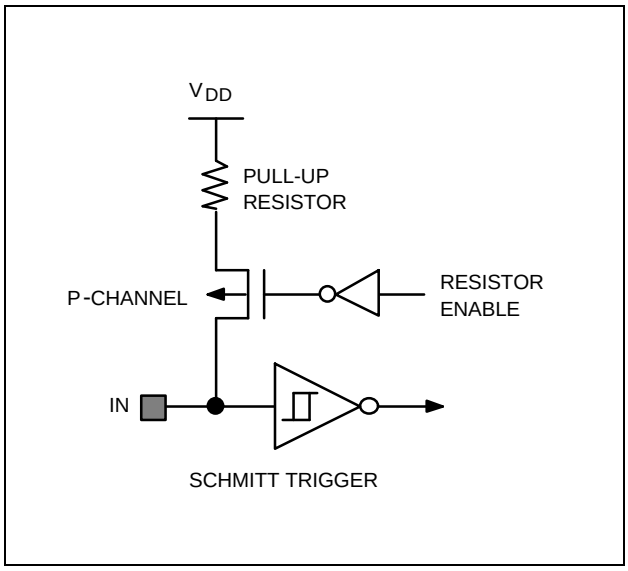


Figure 1-5. Pin Circuit Type A-3

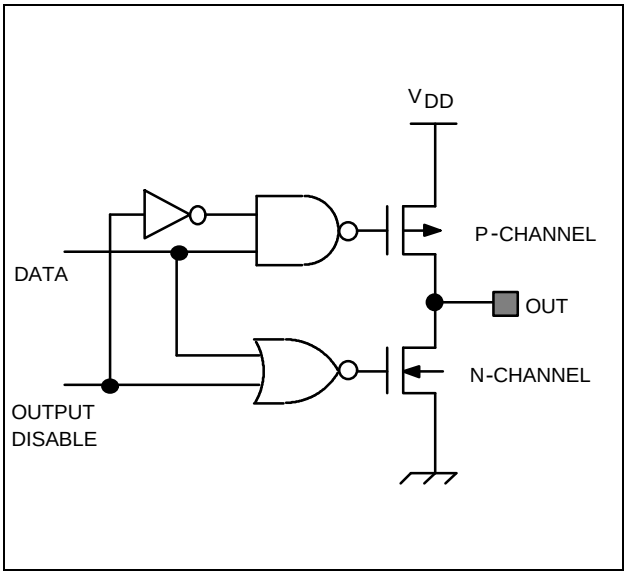


Figure 1-7. Pin Circuit Type C

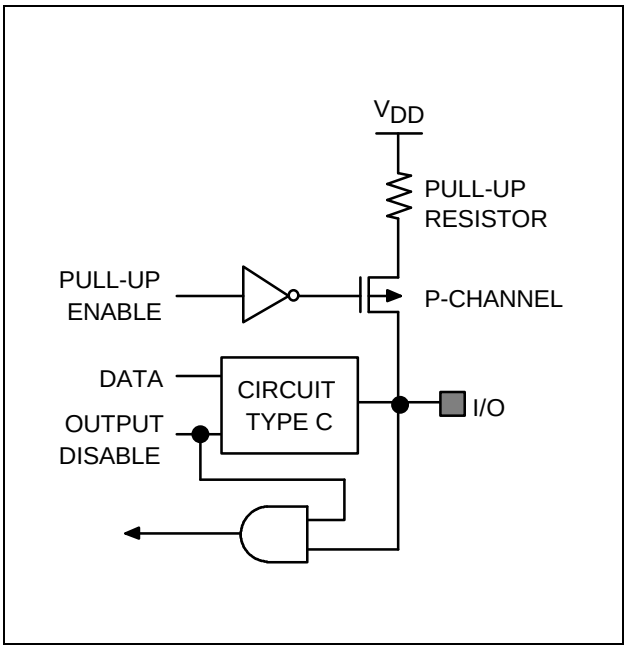


Figure 1-8. Pin Circuit Type D-2

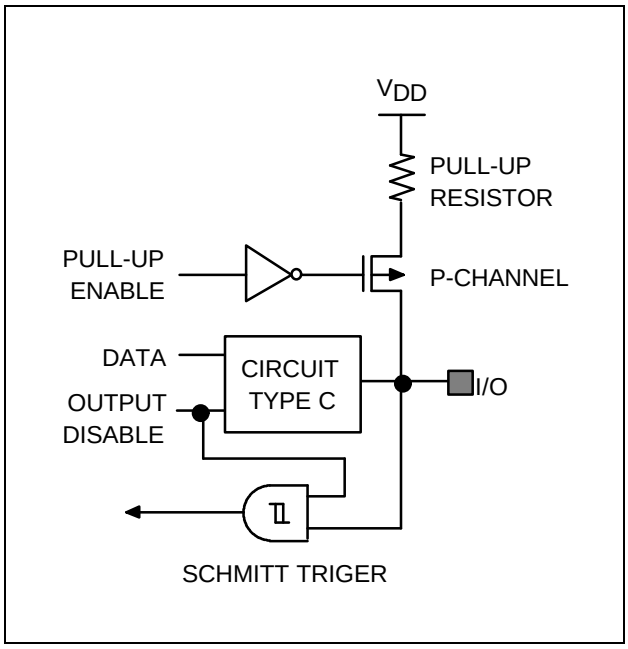


Figure 1-9. Pin Circuit Type D-4

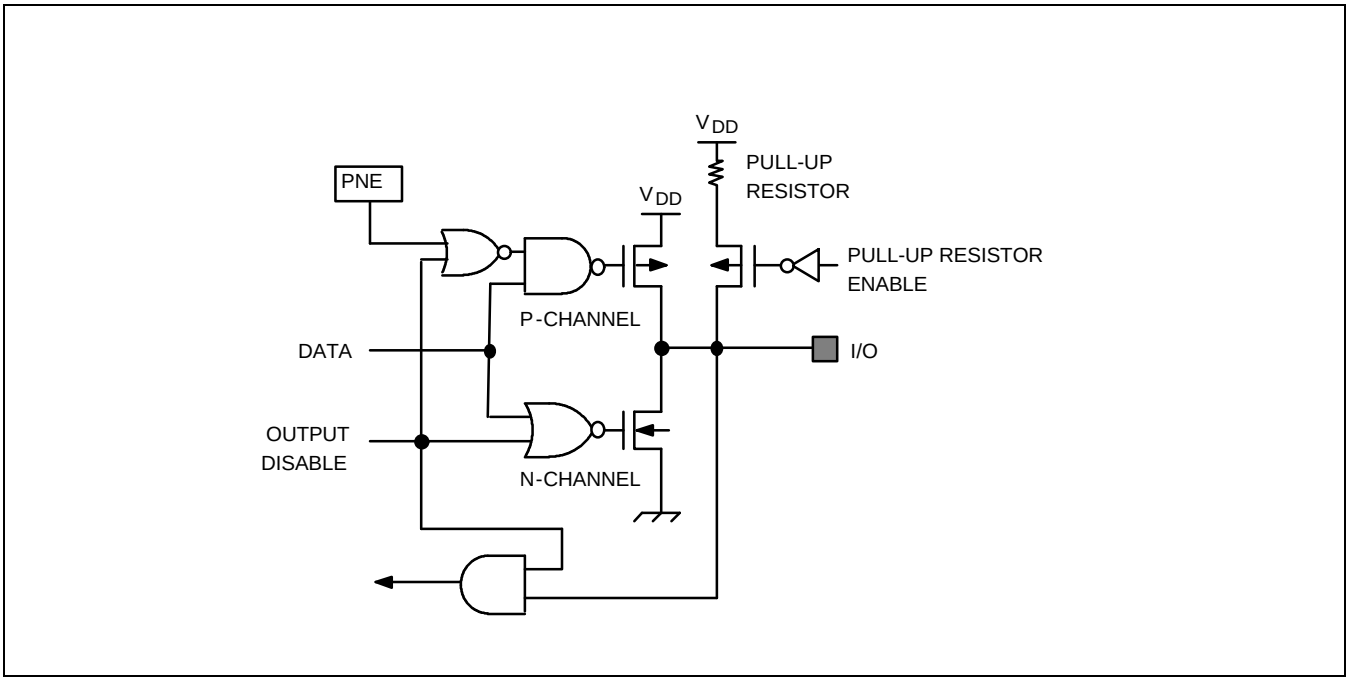


Figure 1-10. Pin Circuit Type E-2

NOTES

12 ELECTRICAL DATA

OVERVIEW

In this chapter, information on KS57C0616 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— System clock oscillator characteristics
— I/O capacitance
— A.C. electrical characteristics
— Operating voltage range

Miscellaneous Timing Waveforms

— A.C timing measurement point
— Clock timing measurement at X_{IN} and X_{OUT}
— TCL timing
— Input timing for RESET
— Input timing for external interrupts

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Table 12-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_{I1}	All I/O ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	– 15	mA
		All I/O ports active	– 35	
Output Current Low	I_{OL}	One I/O port active	+ 30 (Peak value) + 15 (note)	mA
		All I/O ports active	+ 100 (Peak value) + 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

NOTE: The values for output current low (I_{OL}) are calculated as peak value $\times \sqrt{\text{Duty}}$.

Table 12-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	VIH1	All input pins except those specified below for V_{IH2}–V_{IH3}	0.7 V_{DD}	–	V_{DD}	V
	VIH2	Ports 1, 3, 6, 7, and RESET	0.8 V_{DD}		V_{DD}	
	VIH3	X_{IN} and X_{OUT}	V_{DD} – 0.1		V_{DD}	
Input low voltage	VIL1	All input pins except those specified below for V_{IL2}–V_{IL3}	–	–	0.3 V_{DD}	V
	VIL2	Ports 1, 3, 6, 7, and RESET			0.2 V_{DD}	
	VIL3	X_{IN} and X_{OUT}			0.1	

Table 12-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output high voltage	V_{OH}	I_{OH} = – 1 mA Ports except 1	V_{DD} – 1.0	–	–	V
Output low voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA, Ports 4 and 5 only	–	–	2	V
		V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA	–	–	0.4	
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V I_{OL}= 4 mA, all out ports except 4, 5	–	–	2	V
		V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA	–	–	0.4	
Input high leakage current	I_{LIH1}	$V_I = V_{DD}$ All input pins except those specified below	–	–	3	µA
	I_{LIH2}	$V_I = V_{DD}$ X_{IN} and X_{OUT}			20	
Input low leakage current	I_{LIL1}	V_I = 0 V All input pins except below and RESET	–	–	– 3	µA
	I_{LIL2}	V_I = 0 V X_{IN} and X_{OUT} only			– 20	
Output high leakage current	I_{LOH}	$V_O = V_{DD}$ All out pins	–	–	3	µA
Output low leakage current	I_{LOL}	V_O = 0 V All out pins	–	–	– 3	µA
Pull-up resistor	R_{L1}	V_{DD} = 5 V; V_I = 0 V except RESET	25	50	100	kΩ
		V_{DD} = 3 V	50	100	200	
	R_{L2}	V_{DD} = 5 V; V_I = 0 V; RESET	100	250	400	
		V_{DD} = 3 V	200	500	800	

Table 12-2. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

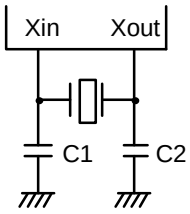
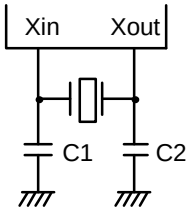
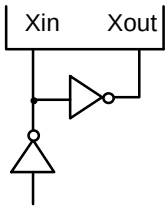
Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply current (1)	I_{DD1}	Run mode; V_{DD} = 5 V ± 10%	6.0 MHz	–	2.6	8.0	mA
		crystal oscillator; C1 = C2 = 22 pF	3.58 MHz		1.7	4.0	
		V_{DD} = 3 V ± 10%	6.0 MHz		1.2	4.0	
			3.58 MHz		0.7	2.3	
	I_{DD2}	Idle mode; V_{DD} = 5 V ± 10%	6.0 MHz	–	0.7	2.5	mA
		crystal oscillator; C1 = C2 = 22 pF	3.58 MHz		0.6	1.8	
		V_{DD} = 3 V ± 10%	6.0 MHz		0.2	1.5	
			3.58 MHz		0.2	1.0	
	I_{DD3}	Stop mode; V_{DD} = 5 V ± 10%		–	0.2	3.0	µA
		Stop mode; V_{DD} = 3 V ± 10%			0.1	2.0	

NOTES:

1. D.C. electrical values for Supply Current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up registers.
2. For D.C. electrical values, the power control register (PCON) must be set to 0011B.

Table 12-3. Main System Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	4.2	
		Stabilization time (2)	V_{DD} = 3 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	4.2	
		Stabilization time (2)	V_{DD} = 3 V	–	–	10	ms
External Clock		X_{IN} input frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	4.2	
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1,250	ns

NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 12-4. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF

Table 12-5. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	0.95			
TCL0, TCL1 Input Frequency	f_{TI0}, f_{TI1}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5 V			1	
TCL0, TCL1 Input High, Low Width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 1.8 V to 5.5 V	1.8			
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0, INT1, INT2, INT4, KS0–KS7	10	–	–	µs
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

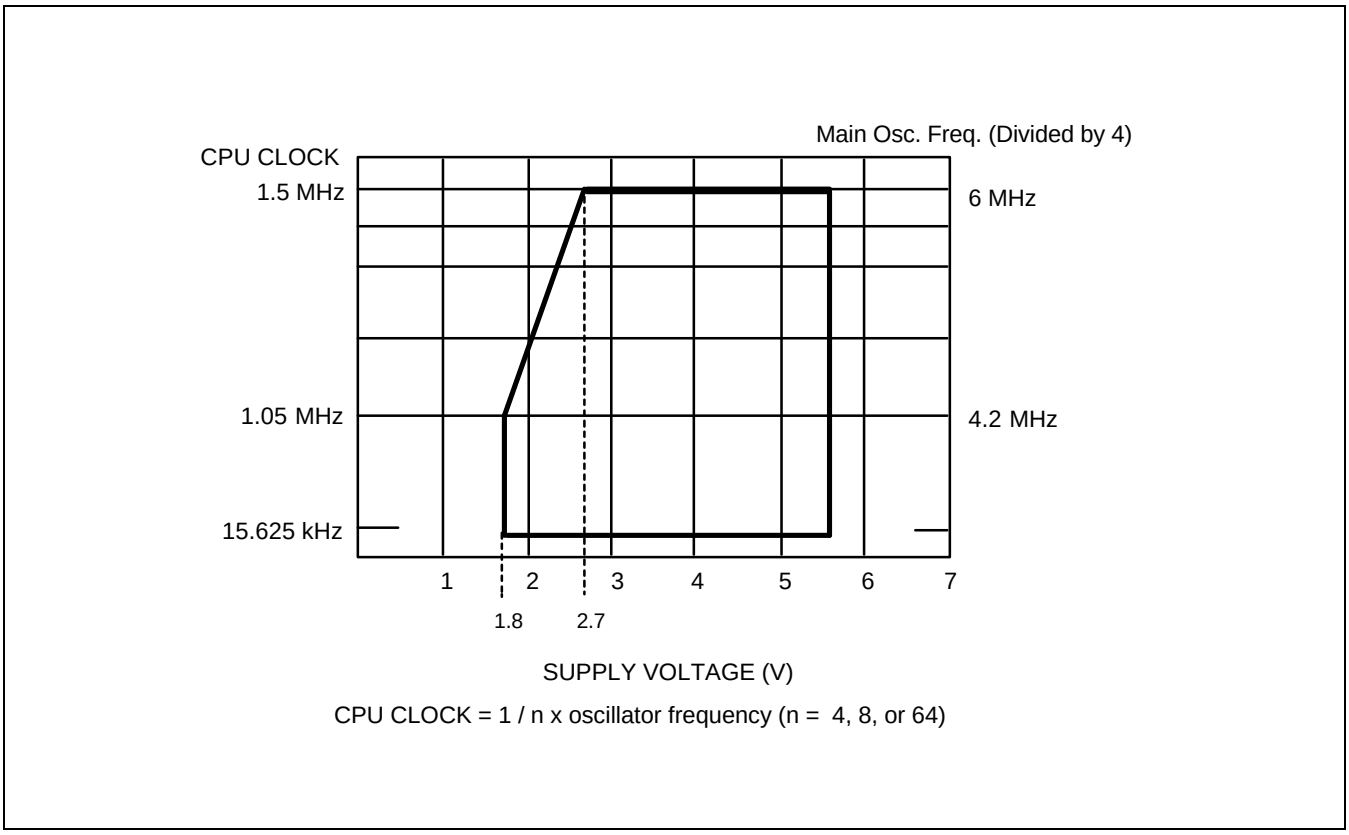


Figure 12-1. Standard Operating Voltage Range

Table 12-6. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17}/fx	–	ms
		Released by interrupt		(2)		

NOTES:

1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

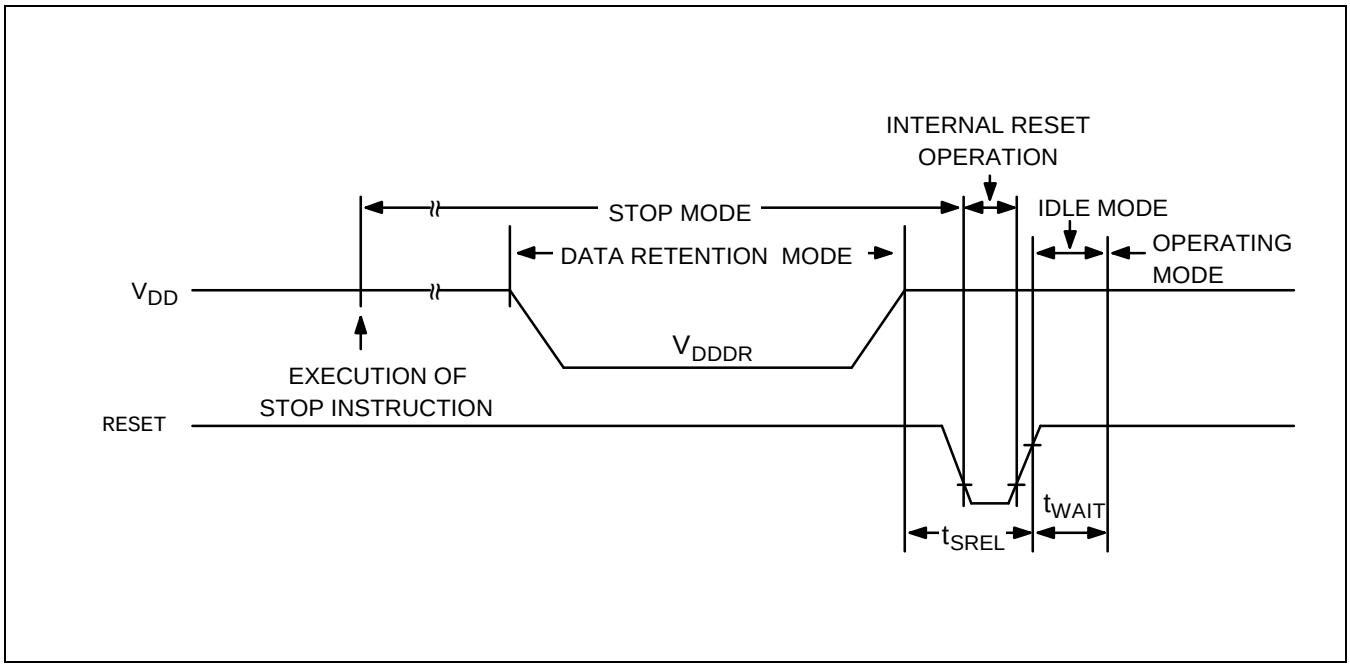


Figure 12-2. Stop Mode Release Timing when Initiated by RESET

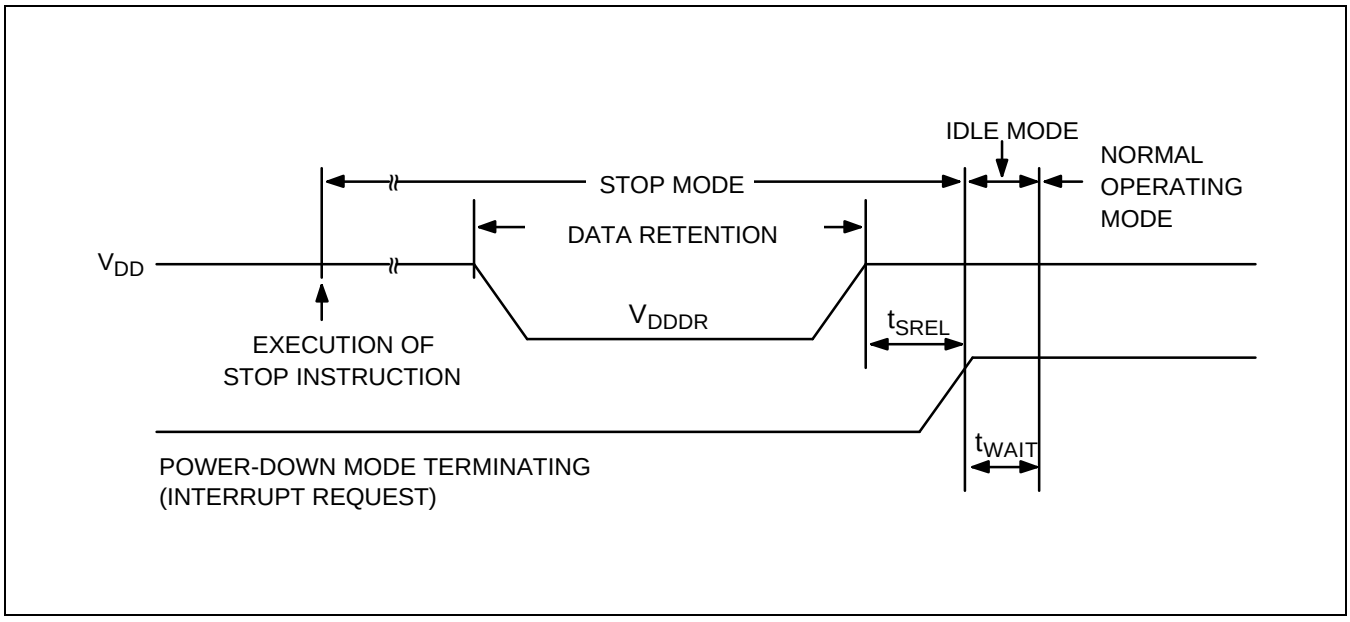


Figure 12-3. Stop Mode Release Timing when Initiated by Interrupt Request

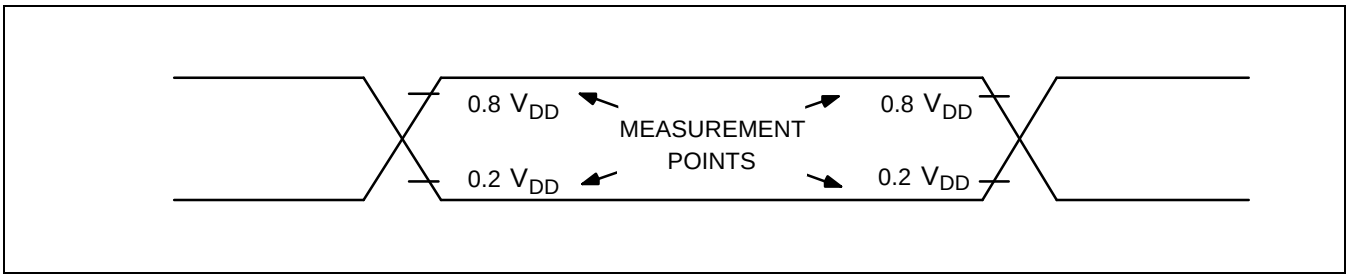


Figure 12-4. A.C. Timing Measurement Points (Except for X_{IN})

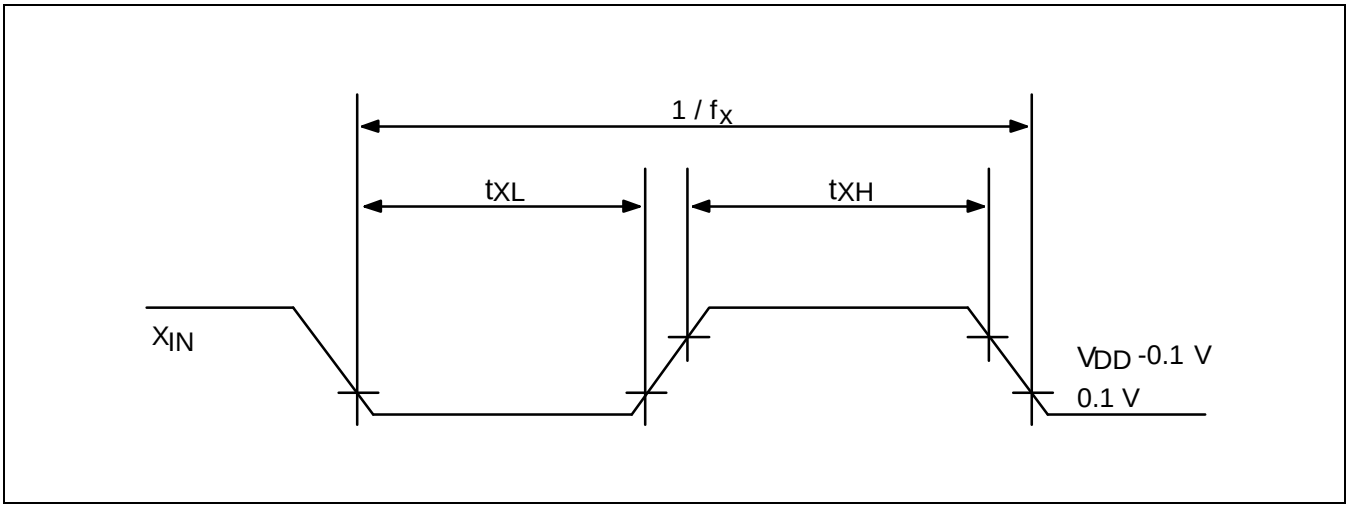


Figure 12-5. Clock Timing Measurement at X_{IN}

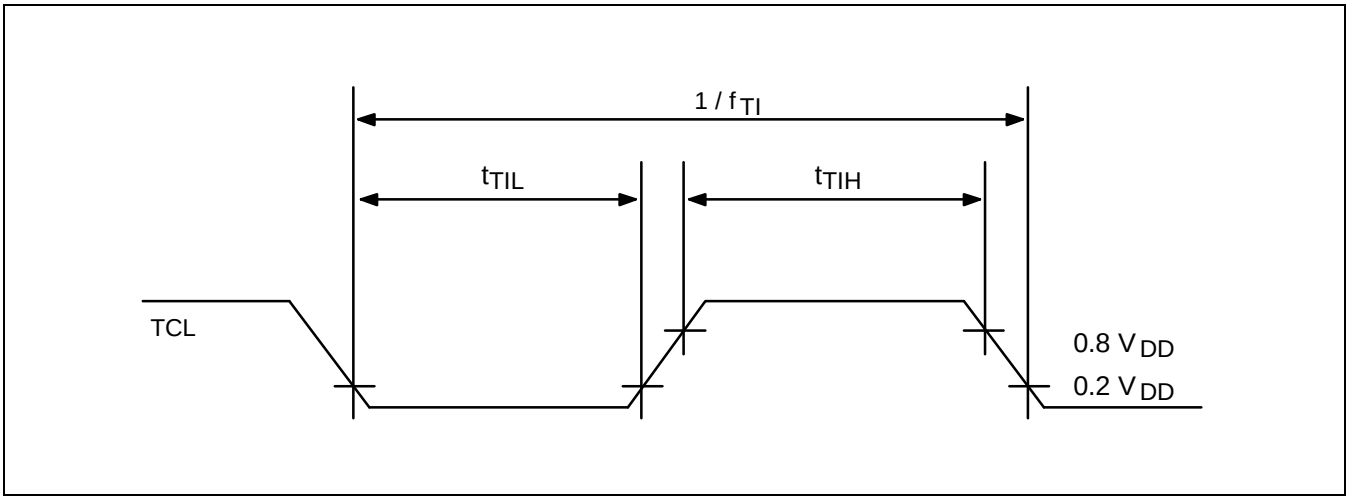


Figure 12-6. TCL Timing

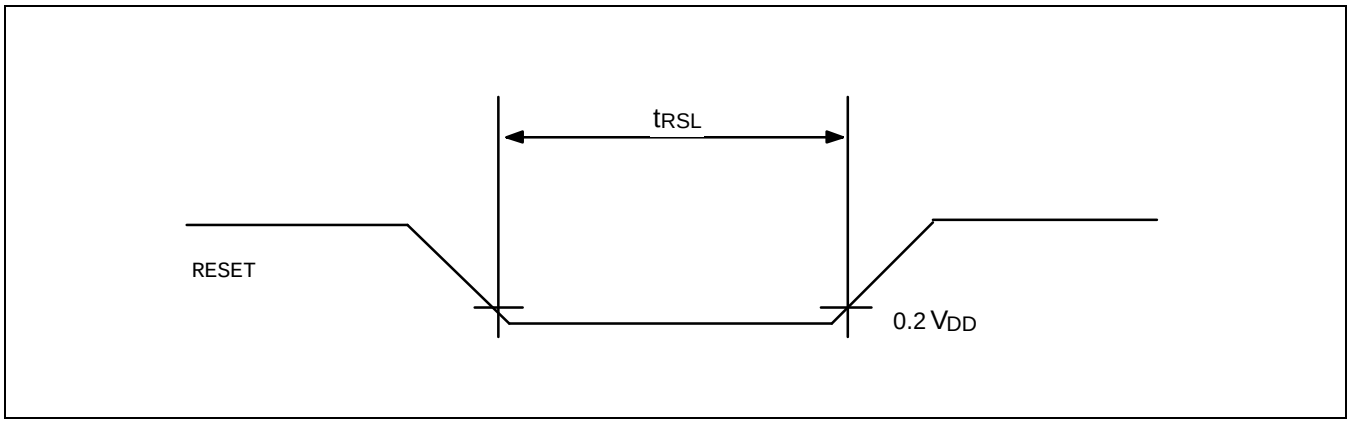


Figure 12-7. Input Timing for RESET Signal

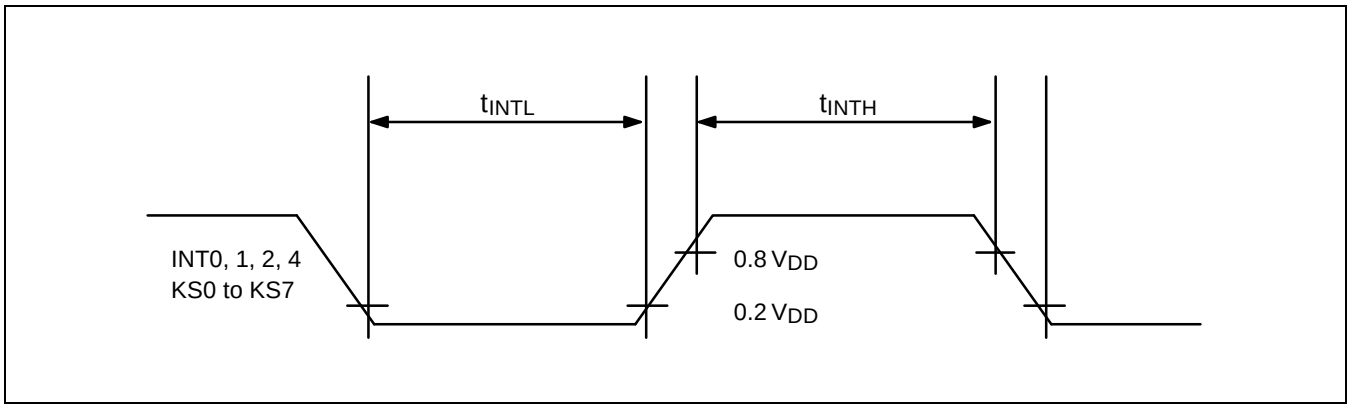


Figure 12-8. Input Timing for External Interrupts and Quasi-Interrupts

13 MECHANICAL DATA

OVERVIEW

The KS57C0616 microcontroller is currently available in 42-pin SDIP and 44-pin QFP package.

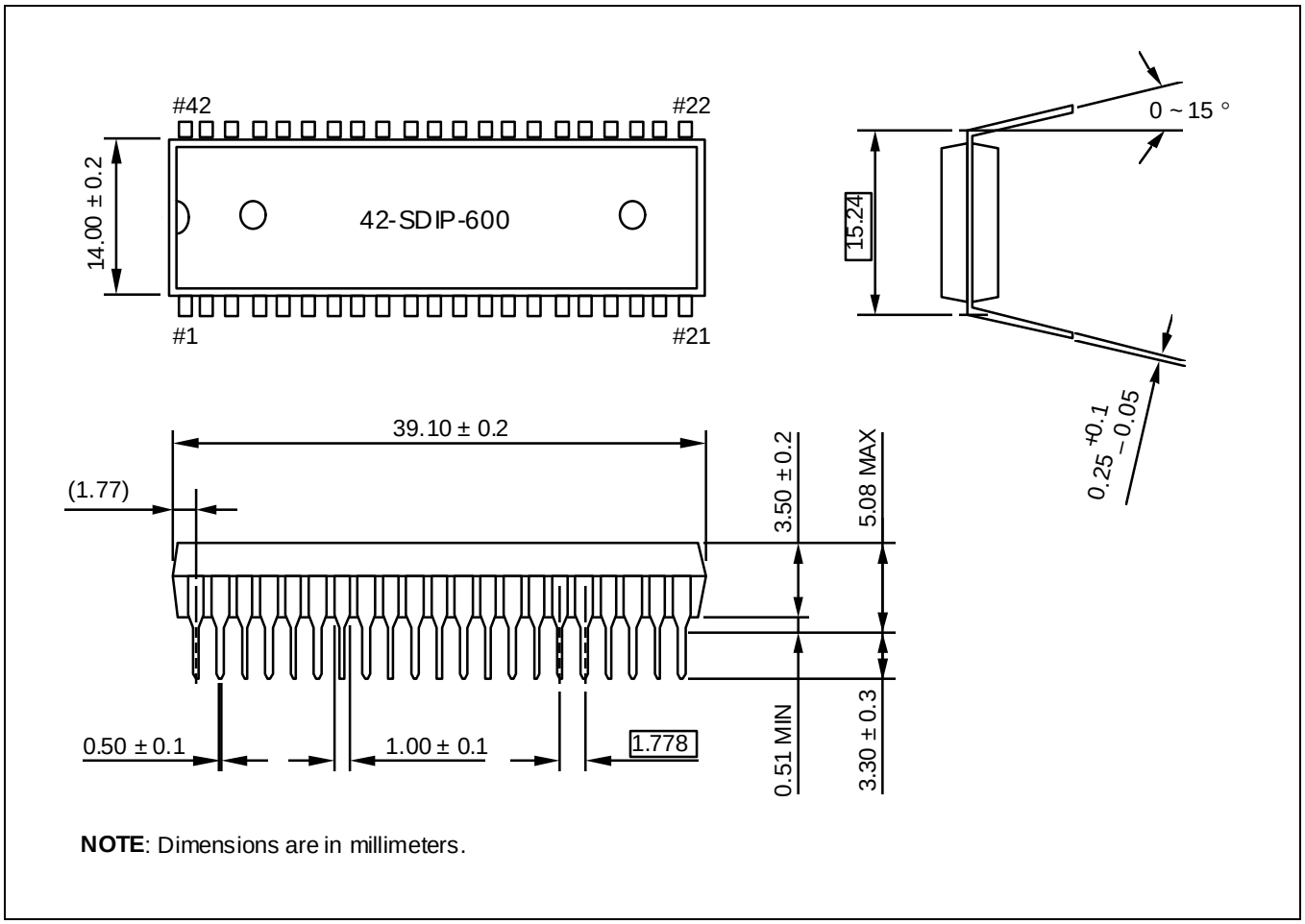


Figure 13-1. 42-Pin SDIP Package Dunebsuibs

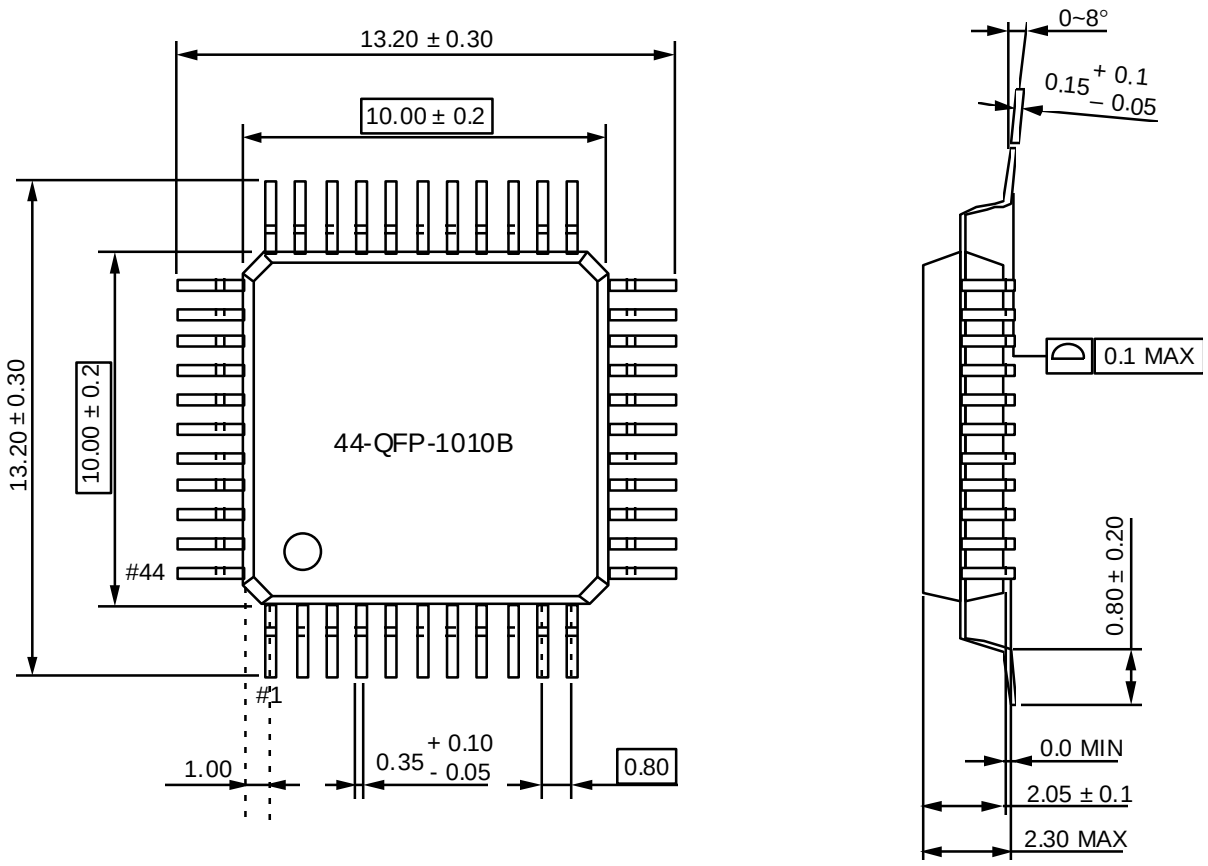


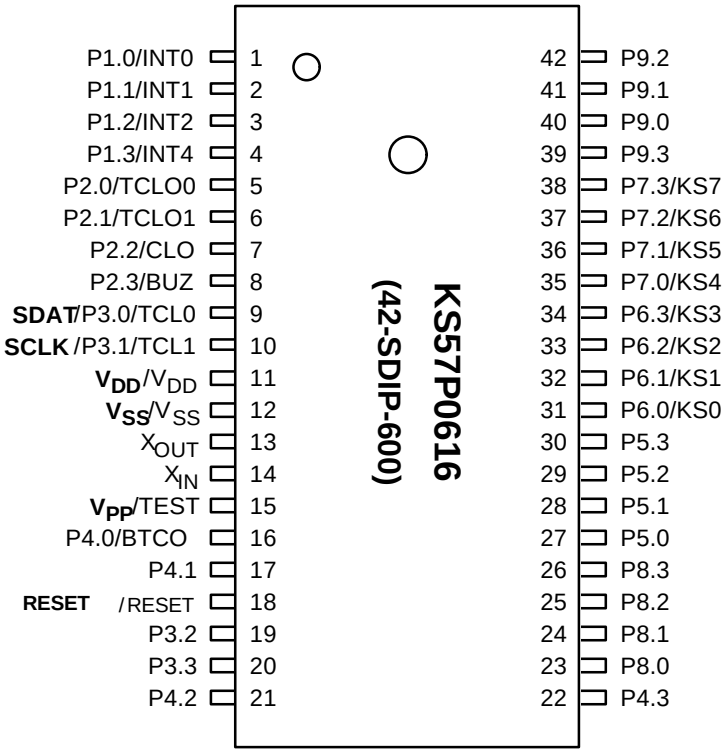
Figure 13-2. 44-Pin QFP Package Dimensions

14 KS57P0616 OTP

OVERVIEW

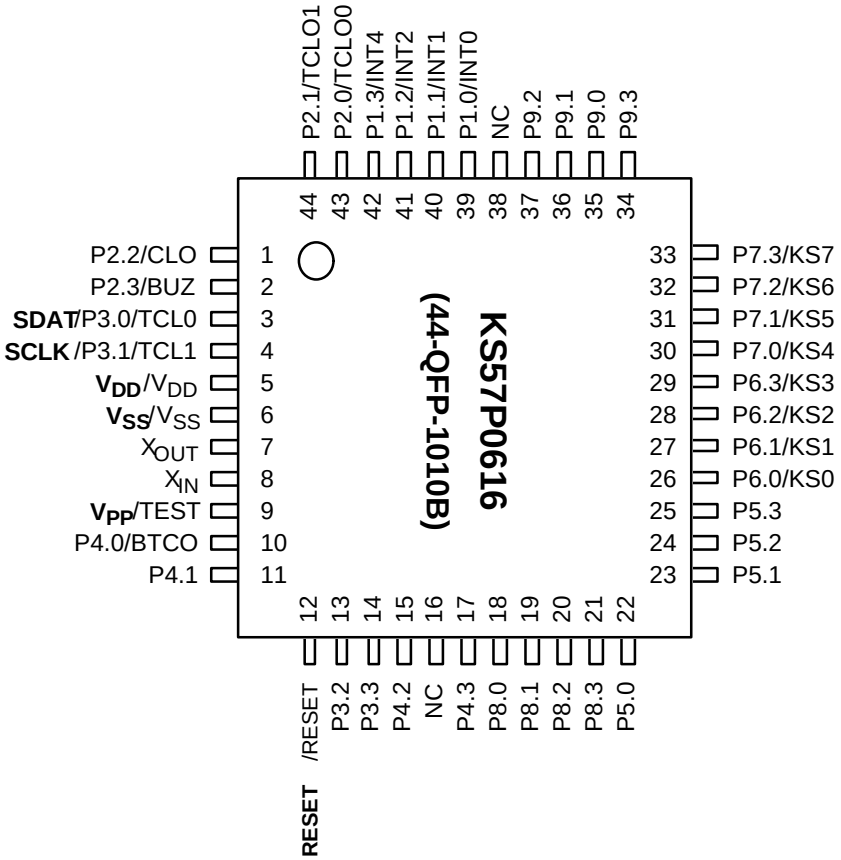
The KS57P0616 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS57C0616 microcontroller. It has an on-chip EPROM instead of masked ROM. The EPROM is accessed by a serial data format.

The KS57P0616 is fully compatible with the KS57C0616, both in function and in pin configuration. Because of its simple programming requirements, the KS57P0616 is ideal for use as an evaluation chip for the KS57C0616.



NOTE: The bolds indicate an OTP pin name.

Figure 14-1. KS57P0616 Pin Assignments (42-SDIP)



NOTE: The bolds indicate an OTP pin name.

Figure 14-2. KS57P0616 Pin Assignments (44-QFP)

Table 14-1. KS57P0616 Pin Descriptions Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	**Pin Name**	**Pin No.**	**I/O**	**Function**
P3.0	SDAT	9 (3)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P3.1	SCLK	10 (4)	I/O	Serial clock pin. Input only pin.
TEST	V_{PP} (TEST)	15 (9)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	18 (12)	I	Chip initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	11/12 (5/6)	I	Logic power supply pin. V_{DD} should be tied to + 5 V during programming.

NOTE: Parentheses indicate pin numbers of 44-QFP package.

Table 14-2. Comparison of KS57P0616 and KS57C0616 Features

Characteristic	KS57P0616	KS57C0616
Program Memory	16-Kbyte EPROM	16-Kbyte mask ROM
Operating Voltage (V_{DD})	1.8 V to 5.5 V	1.8 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST) = 12.5 V	–
Pin Configuration	42 SDIP/44 QFP	42 SDIP/44 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of the KS57P0616, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 14-3 below.

Table 14-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/MEM	Address (A15–A0)	R/w	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

Table 14-4. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_{I1}	All I/O ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	– 15	mA
		All I/O ports active	– 35	
Output Current Low	I_{OL}	One I/O port active	+ 30 (Peak value) + 15 (note)	mA
		All I/O ports active	+ 100 (Peak value) + 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

NOTE: The values for output current low (I_{OL}) are calculated as peak value $\times \sqrt{\text{Duty}}$.

Table 14-5. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH1}	All input pins except those specified below for V_{IH2}–V_{IH3}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 1, 3, 6, 7, and RESET	0.8 V_{DD}		V_{DD}	
	V_{IH3}	X_{IN} and X_{OUT}	V_{DD} – 0.1		V_{DD}	
Input low voltage	V_{IL1}	All input pins except those specified below for V_{IL2}–V_{IL3}	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 1, 3, 6, 7, and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN} and X_{OUT}			0.1	

Table 14-5. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output high voltage	V_{OH}	I_{OH} = – 1 mA Ports except 1	V_{DD} – 1.0	–	–	V
Output low voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA, Ports 4 and 5 only	–	–	2	V
		V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA	–	–	0.4	
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V I_{OL}= 4 mA, all out ports except 4, 5	–	–	2	V
		V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA	–	–	0.4	
Input high leakage current	I_{LIH1}	$V_I = V_{DD}$ All input pins except those specified below	–	–	3	µA
	I_{LIH2}	$V_I = V_{DD}$ X_{IN} and X_{OUT}			20	
Input low leakage current	I_{LIL1}	V_I = 0 V All input pins except below and RESET	–	–	– 3	µA
	I_{LIL2}	V_I = 0 V X_{IN} and X_{OUT} only			– 20	
Output high leakage current	I_{LOH}	$V_O = V_{DD}$ All out pins	–	–	3	µA
Output low leakage current	I_{LOL}	V_O = 0 V All out pins	–	–	– 3	µA
Pull-up resistor	R_{L1}	V_{DD} = 5 V; V_I = 0 V except RESET	25	50	100	kΩ
		V_{DD} = 3 V	50	100	200	
	R_{L2}	V_{DD} = 5 V; V_I = 0 V; RESET	100	250	400	
		V_{DD} = 3 V	200	500	800	

Table 14-5. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

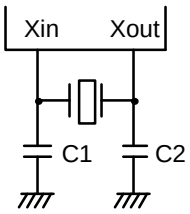
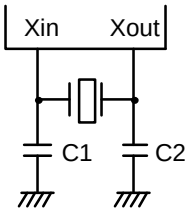
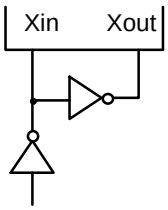
Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply current (1)	I_{DD1}	Run mode; V_{DD} = 5 V ± 10%	6.0 MHz	–	2.6	8.0	mA
		crystal oscillator; C1 = C2 = 22 pF	3.58 MHz		1.7	4.0	
		V_{DD} = 3 V ± 10%	6.0 MHz		1.2	4.0	
			3.58 MHz		0.7	2.3	
	I_{DD2}	Idle mode; V_{DD} = 5 V ± 10%	6.0 MHz	–	0.7	2.5	mA
		crystal oscillator; C1 = C2 = 22 pF	3.58 MHz		0.6	1.8	
		V_{DD} = 3 V ± 10%	6.0 MHz		0.2	1.5	
			3.58 MHz		0.2	1.0	
	I_{DD3}	Stop mode; V_{DD} = 5 V ± 10%		–	0.2	3.0	µA
		Stop mode; V_{DD} = 3 V ± 10%			0.1	2.0	

NOTES:

1. D.C. electrical values for Supply Current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up registers.
2. For D.C. electrical values, the power control register (PCON) must be set to 0011B.

Table 14-6. Main System Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3.0	
		Stabilization time (2)	V_{DD} = 3 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3.0	
		Stabilization time (2)	V_{DD} = 3 V	–	–	10	ms
External Clock		X_{IN} input frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3.0	
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1,250	ns

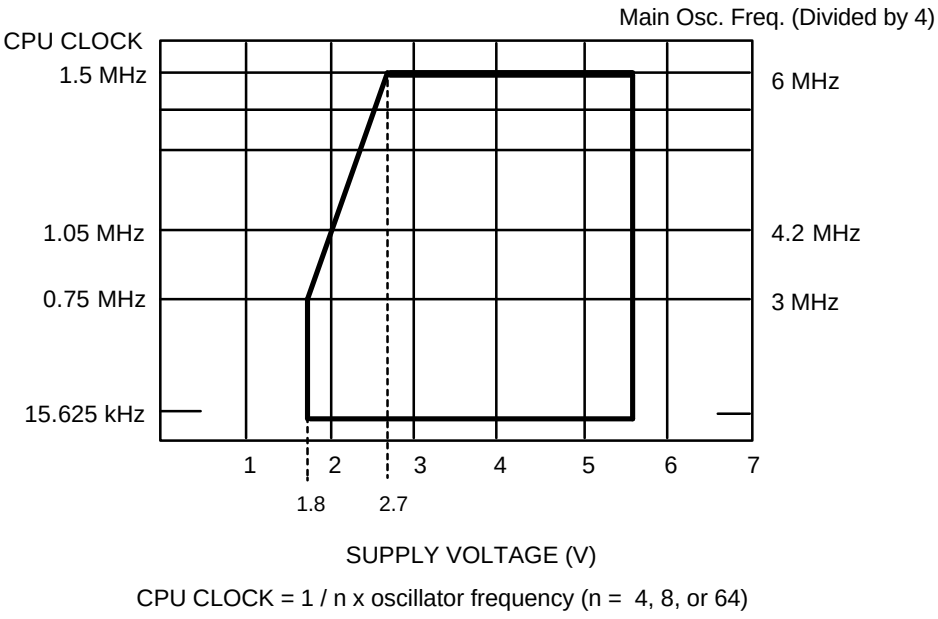
NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 14-7. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF



CPU CLOCK = 1 / n x oscillator frequency (n = 4, 8, or 64)

Figure 14-3. Standard Operating Voltage Range

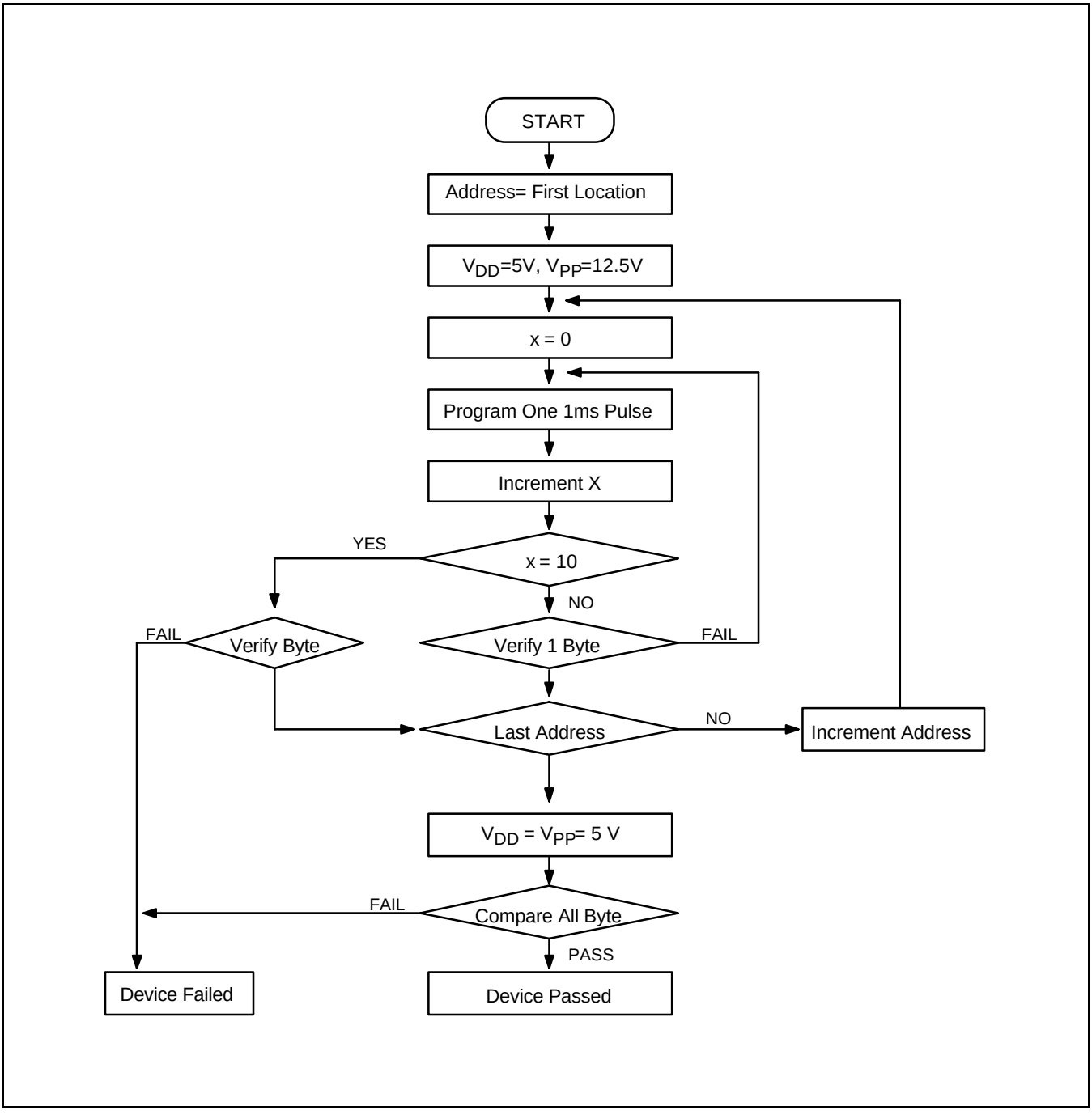


Figure 14-4. OTP Programming Algorithm

NOTES