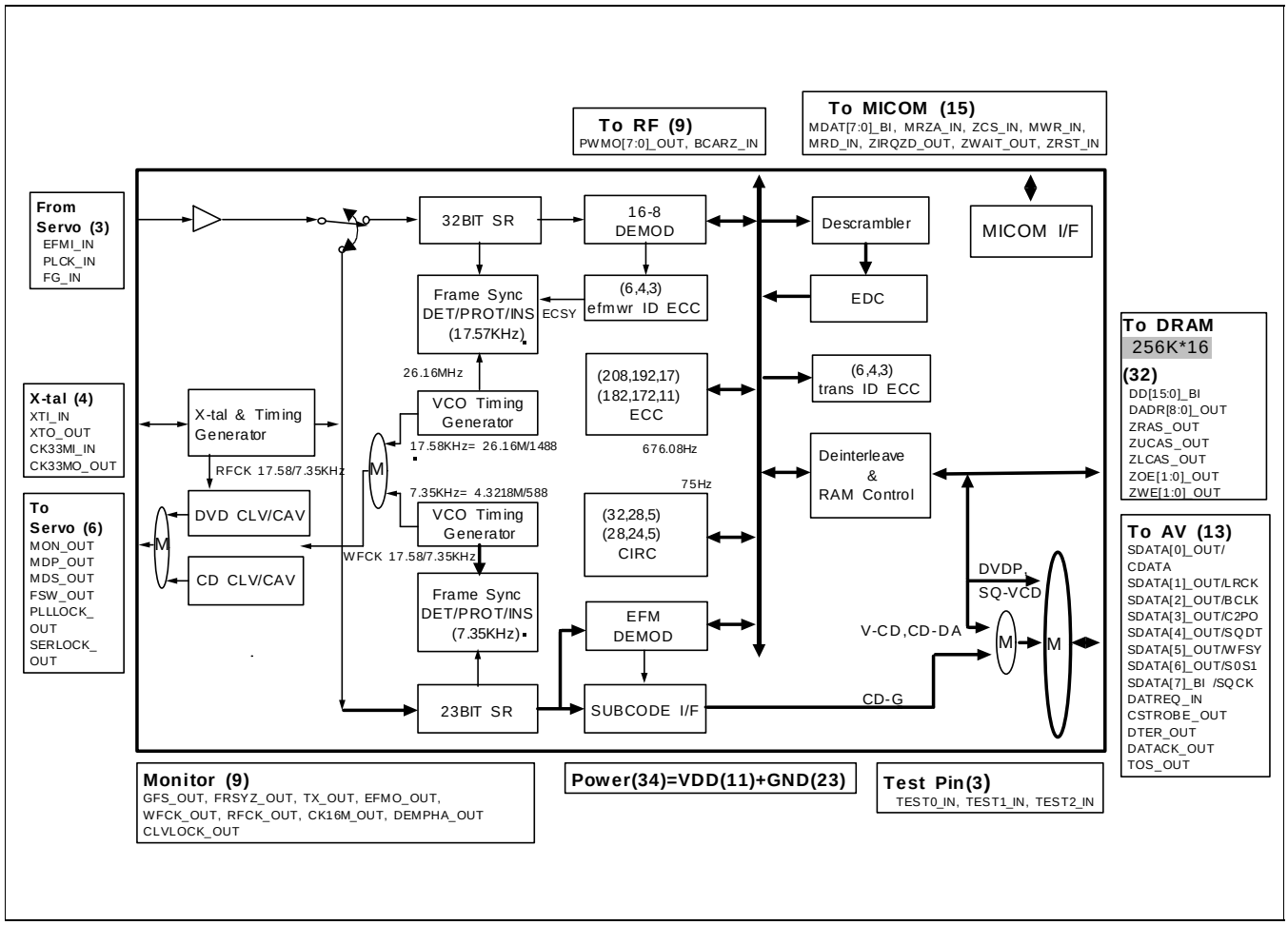
INTRODUCTION

The KS1453 is a Data Process IC which acts as a buffer control for outputting the demodulated data by Hand Shake. It also executes error corrections of the Sliced output of the RF signal from the disc (EFM signals). It is compatible with a 1× DVDP/DVD-ROM and a 4× (CLV standard) CD Data Processing. Its other functions include ECC Error Correction, CD/DVD repeat playback, Descramble, EDC Error Detection, DSI Data Detection, A/V Decoder Interface, CD/VCD Playback, BCA Decoding, Disc Motor Control, EFM Demodulation and Synchronization Detection, Protection, Insertion and ID Data Error Correction.

FEATURES

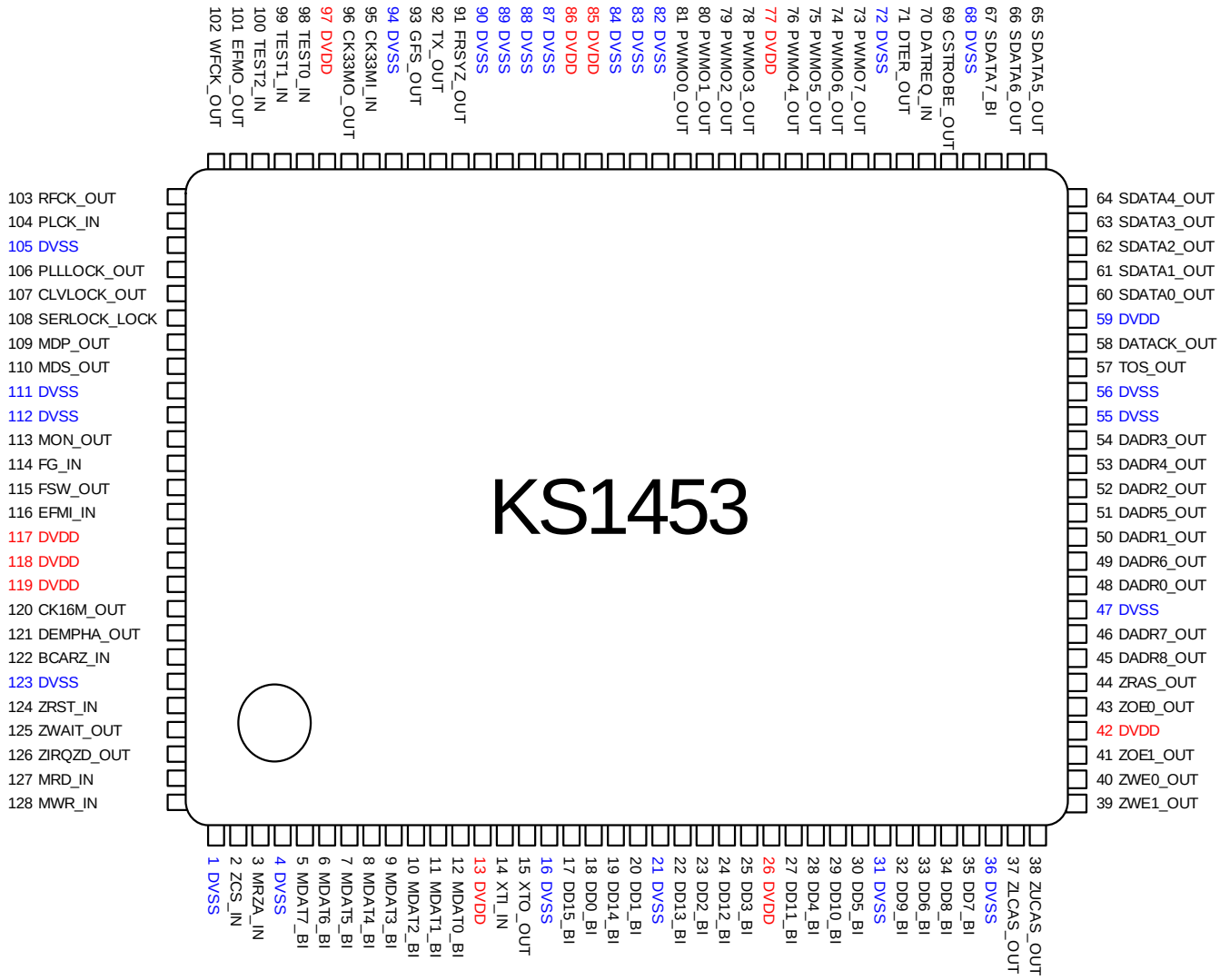
- External PLCK input
- EFM/EFM Plus Demodulator
- Sync Protection/Insertion
- CIRC/RS-PC Error Correction (4/16 Erasure Correction)
- Cross/Row Deinterleave
- 4~16 Mbits DRAM Interface (External component for Error Correction/Track Buffer)
- Descramble
- ID Error Correction
- Main Data Error Detection (EDC)
- Error Flag Monitoring
- MICOM Interface
- Micom Direct Memory Access Function (DVD/CD)
- DSI Detection and DSI Data Output
- A/V Decoder Parallel Interface
- Built-in CD-DA Decoder
- Subcode Data Serial Output
- Spindle Servo Control Signal Generation
- DVD Playback
- CD/VCD Playback (1×, 2× 4×)
- BCA Decoding function
- CLV/CAV function
- CD/VCD Repeat Correction Function
- 5 V Single Power Supply
- 128-QFP
- Application Mode: CD_Player, CD_ROM, Video-CD, DVDP Player

BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN DIAGRAM


KS1453
1 DVSS
2 ZCS_IN
3 MRZA_IN
4 DVSS
5 MDAT7_BI
6 MDAT6_BI
7 MDAT5_BI
8 MDAT4_BI
9 MDAT3_BI
10 MDAT2_BI
11 MDAT1_BI
12 MDAT0_BI
13 DVDD
14 XTI_IN
15 XTO_OUT
16 DVSS
17 DD15_BI
18 DD0_BI
19 DD14_BI
20 DD1_BI
21 DVSS
22 DD13_BI
23 DD2_BI
24 DD12_BI
25 DD3_BI
26 DVDD
27 DD11_BI
28 DD4_BI
29 DD10_BI
30 DD5_BI
31 DVSS
32 DD9_BI
33 DD6_BI
34 DD8_BI
35 DD7_BI
36 DVSS
37 ZLCAS_OUT
38 ZUCAS_OUT
39 ZWE1_OUT
40 ZWE0_OUT
41 ZOE1_OUT
42 DVDD
43 ZOE0_OUT
44 ZRAS_OUT
45 DADR8_OUT
46 DADR7_OUT
47 DVSS
48 DADR0_OUT
49 DADR6_OUT
50 DADR1_OUT
51 DADR5_OUT
52 DADR2_OUT
53 DADR4_OUT
54 DADR3_OUT
55 DVSS
56 DVSS
57 TOS_OUT
58 DATACK_OUT
59 DVDD
60 SDATA0_OUT
61 SDATA1_OUT
62 SDATA2_OUT
63 SDATA3_OUT
64 SDATA4_OUT
65 SDATA5_OUT
66 SDATA6_OUT
67 SDATA7_BI
68 DVSS
69 CSTROBE_OUT
70 DATREQ_IN
71 DTER_OUT
72 DVSS
73 PWMO7_OUT
74 PWMO6_OUT
75 PWMO5_OUT
76 PWMO4_OUT
77 DVDD
78 PWMO3_OUT
79 PWMO2_OUT
80 PWMO1_OUT
81 PWMO0_OUT
82 DVSS
83 DVSS
84 DVSS
85 DVDD
86 DVDD
87 DVSS
88 DVSS
89 DVSS
90 DVSS
91 FRSYZ_OUT
92 TX_OUT
93 GFS_OUT
94 DVSS
95 CK33MI_IN
96 CK33MO_OUT
97 DVDD
98 TEST0_IN
99 TEST1_IN
100 TEST2_IN
101 EFMO_OUT
102 WFCK_OUT
103 RFCK_OUT
104 PLCK_IN
105 DVSS
106 PLLLOCK_OUT
107 CLVLOCK_OUT
108 SERLOCK_LOCK
109 MDP_OUT
110 MDS_OUT
111 DVSS
112 DVSS
113 MON_OUT
114 FG_IN
115 FSW_OUT
116 EFMI_IN
117 DVDD
118 DVDD
119 DVDD
120 CK16M_OUT
121 DEMPHA_OUT
122 BCARZ_IN
123 DVSS
124 ZRST_IN
125 ZWAIT_OUT
126 ZIRQZD_OUT
127 MRD_IN
128 MWR_IN

PIN DESCRIPTION

No.	Pin Name	Description	I/O	Notes
1	DVSS	Digital GND (0 V)		
2	ZCS_IN	Chip Select (Active Low)	I	MICOM
3	MRZA_IN	Micom Register Select (L ® REGISTER H → DATA)	I	MICOM
4	DVSS	Digital GND (0 V)		
5	MDAT7_BI	MICOM Data Bus	B	MICOM
6	MDAT6_BI	MICOM Data Bus	B	MICOM
7	MDAT5_BI	MICOM Data Bus	B	MICOM
8	MDAT4_BI	MICOM Data Bus	B	MICOM
9	MDAT3_BI	MICOM Data Bus	B	MICOM
10	MDAT2_BI	MICOM Data Bus	B	MICOM
11	MDAT1_BI	MICOM Data Bus	B	MICOM
12	MDAT0_BI	MICOM Data Bus	B	MICOM
13	DVDD	Digital Power (+5V)		
14	XTI_IN	System Clock Input for 26.16 MHz	I	XTAL
15	XTO_OUT	System Clock Output for 26.16 MHz	O	XTAL
16	DVSS	Digital GND (0 V)		
17	DD15_BI	DRAM Data Bus	B	DRAM
18	DD0_BI	DRAM Data Bus	B	DRAM
19	DD14_BI	DRAM Data Bus	B	DRAM
20	DD1_BI	DRAM Data Bus	B	DRAM
21	DVSS	Digital GND (0 V)		
22	DD13_BI	DRAM Data Bus	B	DRAM
23	DD2_BI	DRAM Data Bus	B	DRAM
24	DD12_BI	DRAM Data Bus	B	DRAM
25	DD3_BI	DRAM Data Bus	B	DRAM
26	DVDD	Digital Power (+5 V)		
27	DD11_BI	Digital Data Bus	B	DRAM
28	DD4_BI	Digital Data Bus	B	DRAM
29	DD10_BI	Digital Data Bus	B	DRAM
30	DD5_BI	Digital Data Bus	B	DRAM
31	DVSS	Digital GND (0 V)		
32	DD9_BI	DRAM Data Bus	B	DRAM
33	DD6_BI	DRAM Data Bus	B	DRAM
34	DD8_BI	DRAM Data Bus	B	DRAM
35	DD7_BI	DRAM Data Bus	B	DRAM
36	DVSS	Digital GND (0 V)		
37	ZLCAS_OUT	DRAM Low Column Address Strobe	O	DRAM
38	ZUCAS_OUT	DRAM Upper Column Address Strobe	O	DRAM
39	ZWE1_OUT	DRAM Write Enable 1 (8M ONLY)	O	DRAM
40	ZWE0_OUT	DRAM Write Enable 0 (4M, 8M, 16M)	O	DRAM
41	ZOE1_OUT	DRAM Output Enable 1 (16M MODE DADR9)	O	DRAM
42	DVDD	Digital Power (+5 V)		
43	ZOE0_OUT	DRAM Output Enable 0	O	DRAM
44	ZRAS_OUT	DRAM Row Address Strobe	O	DRAM
45	DADR8_OUT	DRAM Address Bus	O	DRAM

No.	Pin Name	Description	I/O	Notes
46	DADR7_OUT	DRAM Address Bus	O	DRAM
47	DVSS	Digital GND (0 V)		
48	DADR0_OUT	DRAM Address Bus	O	DRAM
49	DADR6_OUT	DRAM Address Bus	O	DRAM
50	DADR1_OUT	DRAM Address Bus	O	DRAM
51	DADR5_OUT	DRAM Address Bus	O	DRAM
52	DADR2_OUT	DRAM Address Bus	O	DRAM
53	DADR4_OUT	DRAM Address Bus	O	DRAM
54	DADR3_OUT	DRAM Address Bus	O	DRAM
55	DVSS	Digital GND (0 V)		
56	DVSS	Digital GND (0 V)		
57	TOS_OUT	Top of Sector	O	AV Decoder
58	DATACK_OUT	Data Acknowledge Signal Output	O	AV Decoder
59	DVDD	DIGITAL Power (+5 V)		
60	SDATA0_OUT	DVD Data/CD Data Bit Stream (CDATA)	O	AV Decoder
61	SDATA1_OUT	DVD Data/CD Data L/R Clock (LRCK)	O	AV Decoder
62	SDATA2_OUT	DVD Data/CD Data Bit Clock (BLCK)	O	AV Decoder
63	SDATA3_OUT	DVD Data/CD Data Error Flag (C2PO)	O	AV Decoder
64	SDATA4_OUT	DVD Data/Subcode Serial Data (SQDT)	O	AV Decoder
65	SDATA5_OUT	DVD Data/Subcode Frame Sync (WFSY)	O	AV Decoder
66	SDATA6_OUT	DVD Data/Subcode Block Sync (S0S1)	O	AV Decoder
67	SDATA7_BI	DVD Data/Subcode Serial Clock (SQCK)	B	AV Decoder
68	DVSS	Digital GND (0 V)		
69	CSTROBE_OUT	Data Strobe (Clock) Output	O	AV Decoder
70	DATREQ_IN	Data Request from A/V Decoder or ROM Decoder	I	AV Decoder
71	DTER_OUT	DVD Data Error Output	O	AV Decoder
72	DVSS	Digital GND (0 V)		
73	PWMO7_OUT	PWM Output Signal	O	RF
74	PWMO6_OUT	PWM Output Signal	O	RF
75	PWMO5_OUT	PWM Output Signal	O	RF
76	PWMO4_OUT	PWM Output Signal	O	RF
77	DVDD	Digital Power (+5 V)		
78	PWMO3_OUT	PWM Output Signal	O	RF
79	PWMO2_OUT	PWM Output Signal	O	RF
80	PWMO1_OUT	PWM Output Signal	O	RF
81	PWMO0_OUT	PWM Output Signal	O	RF
82	DVSS	Digital GND (0 V)		
83	DVSS	Digital GND (0 V)		
84	DVSS	Digital GND (0 V)		
85	DVDD	DIGITAL Power (+5 V)		
86	DVDD	DIGITAL Power (+5 V)		
87	DVSS	Digital GND (0 V)		
88	DVSS	Digital GND (0 V)		
89	DVSS	Digital GND (0 V)		
90	DVSS	Digital GND (0 V)		
91	FRSYZ_OUT	Frame Sync Out	O	Monitor
92	TX_OUT	Digital Out	O	Monitor

No.	Pin Name	Description	I/O	Notes
93	GFS_OUT	Good Frame Sync Detection State Output (OK at H)	O	Monitor
94	DVSS	Digital GND (0 V)		
95	CK33MI_IN	System Clock Input for 33.8688 MHz	I	X-tal
96	CK33MO_OUT	System Clock Output for 33.8688 MHz	O	X-tal
97	DVDD	Digital Power (+5 V)		
98	TEST0_IN	Test Mode Selection Terminal	I	
99	TEST1_IN	Test Mode Selection Terminal	I	
100	TEST2_IN	Test Mode Selection Terminal	I	
101	EFMO_OUT	EFM Out	O	Monitor
102	WFCK_OUT	Write Frame Pulse	O	Monitor
103	RFCK_OUT	Reference Frame Pulse	O	Monitor
104	PLCK_IN	Phase Locked Clock	I	Servo
105	DVSS	Digital GND (0 V)		
106	PLLLOCK_OUT	Lock Signal for PLL	O	Servo
107	CLVLOCK_OUT	Lock Signal for CLV	O	Monitor
108	SERLOCK_OUT	Lock Signal for SERVO	O	Servo
109	MDP_OUT	Spindle Motor Phase Control Signal (3-STATE)	O	Servo
110	MDS_OUT	Spindle Motor Speed Control Signal (3-STATE)	O	Servo
111	DVSS	Digital GND (0 V)		
112	DVSS	Digital GND (0 V)		
113	MON_OUT	Spindle Motor Output Filter Switching Output	O	Servo
114	FG_IN	Reference Signal for CAV	I	Servo
115	FSW_OUT	Spindle Motor Output Filter Switching Output (3-STATE)	O	Servo
116	EFMI_IN	EFM/EFM+ Signal Input	I	Servo
117	DVDD	Digital Power (+5 V)		
118	DVDD	Digital Power (+5 V)		
119	DVDD	Digital Power (+5 V)		
120	CK16M_OUT	CK33Ms 2 Division Clock / 16.9344 MHz	O	Monitor
121	DEMPHA_OUT	"HIGH", when on Deemphasis	O	Monitor
122	BCARZ_IN	BCA Input Signal	I	RF
123	DVSS	Digital GND (0 V)		
124	ZRST_IN	Hardware Reset (Active Low)	I	MICOM
125	ZWAIT_OUT	Micom Read / Write Access Wait (Wait at L)	O	MICOM
126	ZIRQZD_OUT	Interrupt Request to Micom	O	MICOM
127	MRD_IN	Micom Read Strobe (Active Low)	I	MICOM
128	MWR_IN	Micom Write Strobe (Active Low)	I	MICOM

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(VDD = 5.0 V ± 5%, VSS = 0 V, Ta = 0 ~ +70°C)

Item			Conditions	Min	Max	Unit	Applicable Terminal
Input Voltage	Input Voltage "H" Level	V_{IH}	–	0.7 V_{DD}	–	V	①
	Input Voltage "L" Level	V_{IL}	–	–	0.3 V_{DD}	V	
Output Voltage	Output Voltage "H" Level	V_{OH}	I_{OH} = -2, -4 mA	2.4	V_{DD}	V	②
	Output Voltage "L" Level	V_{OL}	I_{OL} = 2, 4 mA	0	0.4	V	
Input Current	Input Current "H" Level	I_{IH1}	V_{IN} = V_{DD}	-10	+10	μA	③
	Input Current "L" Level	I_{IL1}	V_{IN} = V_{SS}	-10	+10	μA	
Input Current	Input Current "H" Level	I_{IH2}	V_{IN} = V_{DD}	10	100	μA	④
	Input Current "L" Level	I_{IL2}	V_{IN} = V_{SS}	-100	-10	μA	⑤
Input LEAK Current		I_{LI}	V_I = 0 ~ 5. 25 V	-10	+10	μA	①

NOTES:

①: All CMOS input terminal, BIDIR PADs input mode terminal

②: All Output Signals

③: All CMOS input terminal, BIDIR PADs input mode terminal

④: All inputs having Pull-down

⑤: All inputs having Pull-up

ABSOLUTE MAXIMUM RATINGS

No.	Item	Symbol	Spec.	Unit
1	DC input voltage	Vin	-0.3 ~ VDD + 0.3	V
2	DC supply voltage	V_{DD}max	-0.3 to +7.0	V
3	DC input current	Iin	$\pm$10	mA
4	Storage Temperature	Tstg	-40 ~ 125	°C

RECOMMENDED OPERATION CONDITIONS

No.	Item	Symbol	Spec.	Unit
1	Operating Temperatures	Topr	0 ~ 70	°C
2	DC supplied voltage	V_{DD}	4.75 ~ 5.25	V

BLOCK CHARACTERISTICS

ECC FEATURE

- Uses Euclid's Algorithm
- Uses the same circuit as DVD, BCA, and CD

1) In the case of DVD (primitive polynomial: $x^8 + x^4 + x^3 + x^2 + 1$)

:Error Correcting Capability for DVD Data.

→ PI (182, 172, 11) CODE: 5 error correction/10 errata correction

→ PO (208, 192, 17) CODE: 8 error correction/16 errata correction

:Error Correction Capability for BCA Data.

→ BCA (52, 48, 5) CODE: 2 error correction

- 33.8688 MHz Clock: 1X operation (PI + PO + PI)/1 EFM BLOCK Satisfaction - Basic Operation.

2) In the case of CD (primitive polynomial: $x^8 + x^4 + x^3 + x^2 + 1$)

C1 (32, 28, 5) CODE: 2 errata corrected

C2 (28, 24, 4) CODE: 4 errata corrected

- In the case of video - CD, repeat correction is executed (C1 → C2 → C1 → C2)

MEMORY CONTROL FEATURE

- The CD Data Processor and DVD Data Processor share an external 4M or 8M DRAM.
- Has EFM Data Write, ECC Data R/W, Descrambler R/W and Transfer Read Addressing features.
- Over/Under Memory Control (VBR Control)

1) In the case of DVD

- User a 33.8688MHz Crystal Clock
- Continual storage by input order, unrelated to Data type (PO Deinterleave)
- 13 ECC Block Areas in the 4MBit DRAM (Performs EFM, ECC, Descrambler, Transfer)
- BCA Area secured (208 Bytes)
- Micom User Area secured (can use Blocks 1 ~ 8 in units of ECC Blocks)
- Can Write in units of Sectors in EFM Data Write
- Can transmit in units of Sectors when transmitting Data
- Block Copy Feature (can specify number of Sectors)
- MICOM Direct Access on DRAM

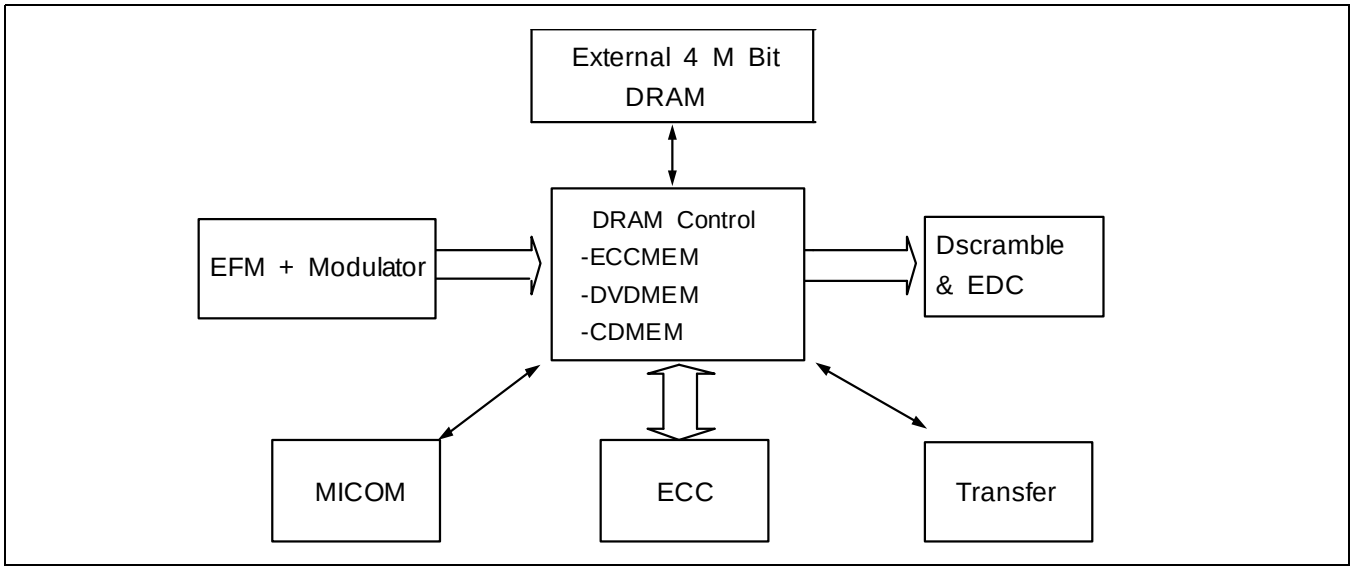


Figure 1. Block Diagram Of Memory Controller

2) In the case of CD

- CD-DA, CD-ROM, V-CD: Uses 33.8688MHz Crystal Clock
- VIDEO-CD: Repeat Correction Possible
- Uses 8 Kilobytes Memory Area
- EFM, ECC, Transfer function
- EFM: WFCK Standard
- ECC, Transfer: RFCK Standard
- Micom Direct Access on DRAM

3) Descrambler & EDC & Transfer Feature

- Control of Descramble On/Off from Micom
- ECD Flag output to Micom
- Choice between 2048 Bytes or 2064 Bytes for output
- Adjustable transmission sector number
- Maximum transmission rate 5.4 Mbyte/s
- Parallel synchronous I/F application
- Active 'L/H" selection possible for REQUEST, TOS, ACK, DATCLK, and EDCFLG

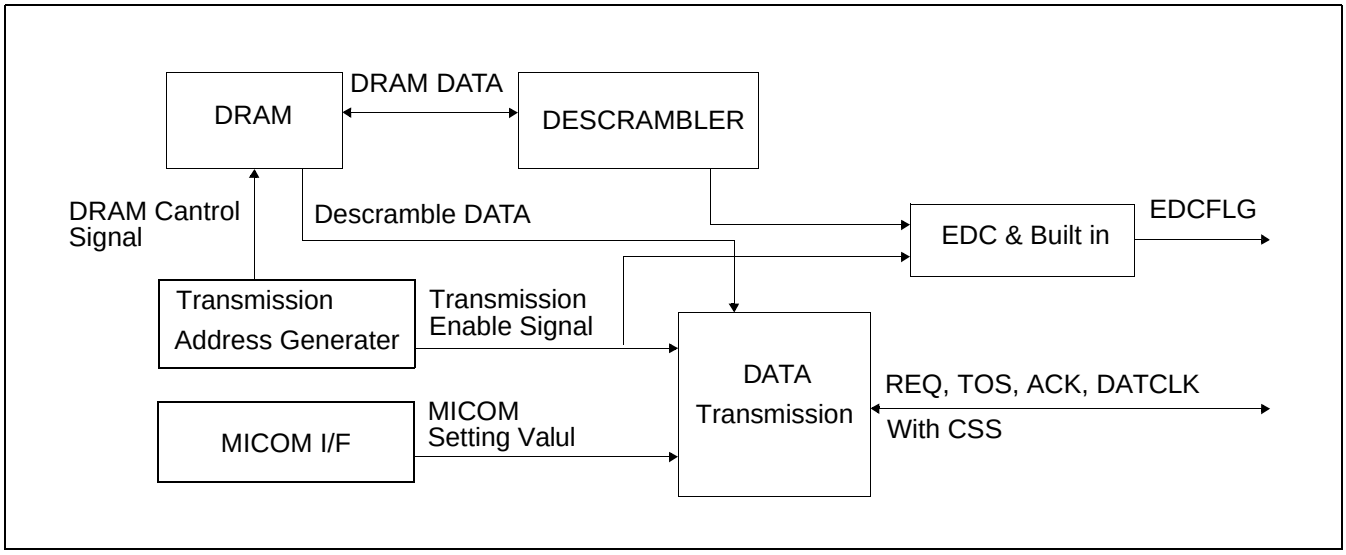


Figure 2. Transmitter Block Diagram

4) CD Audio Feature

- Data with all its errors corrected is input in Bytes, and output serially
- In case of CD - DA, Interpolation, Mute and Attenuation are handled.

5) Subcode I/f Feature

- Serially outputs the Subcode Data (P, Q, R, S, T, V, W) for CD Graphic handling
- Outputs the Subcode Data (Q) for Disc Control after checking for Errors

$(p(x) = x^{16} + x^{12} + x^5 + 1)$

6) BCA Feature

- BCA Code Structure
  - . 4 RS ECC code max (52, 48) codes/Number of Pure information Bytes - 188 Bytes
  - . Composed of maximm 208 Bytes. Interleaved in units of 4 Bytes.
  - . Disc Rotation Speed: 1440 rpm (24 Hz), Channel bit time width - 8.89 us (01 or 10)
- BCA Block Implementation
  - . Data PLL is designed as an X-tal based clock
  - . 188 * 8 bits information bits EDC check (32 bits $x^{32} + x^{31} + x^4 + 1$)
  - . PE RZ mod. [0] $\rightarrow$ 10, [1] $\rightarrow$ 01
  - . BCK Data and Size Detection
  - . Sync detection (Sync byte, Resync) and Demodulation
  - . Memory control design for deinterleave and buffering, ECC and EDC
  - . ECC decoding for 4 (52, 48) codes

7) EFM Demodulator Feature

- CD Player, CD - ROM, DVD Player Mode Operation
- Demodulator: EFM + Demodulation (DVD)
  EFM Demodulation (CD)
- ID Sync, Frame Sync Detection/Protection/Insertion:
  4 step ID Sync/Frame Sync Protection Window section selection
  4 step ID Sync/Frame Sync Insertion Frame Number selection
- SID Error Correction
- ID (Frame) Sync Continuous Check

8) Micom I/F Feature

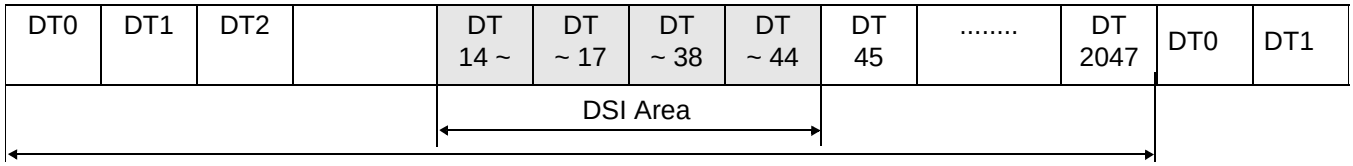
- Address/Command Data: 1 Byte
- Read/Write Register Access

9) DSI I/F Feature

In the 2048 Main Data of the DVD Decoder:

. System Header Start Code (00, 00, 01, BB) from the 15th Byte
. Packet Header (00, 00, 01, BF, **, **) from the 39th Byte, Sub_Stream_id

The sector is determined to be DSI Pack and DSINT is set to "1". When CLRINT bit is "1", and the MICOM read in S4A4B [A8] Register Conditions, it becomes cleared to '0"



2048 Main Data Within Sector 1.

. Dont care in CD MODE

INTERFACE

MICOM I/F

MICOM I/F Timing Diagram

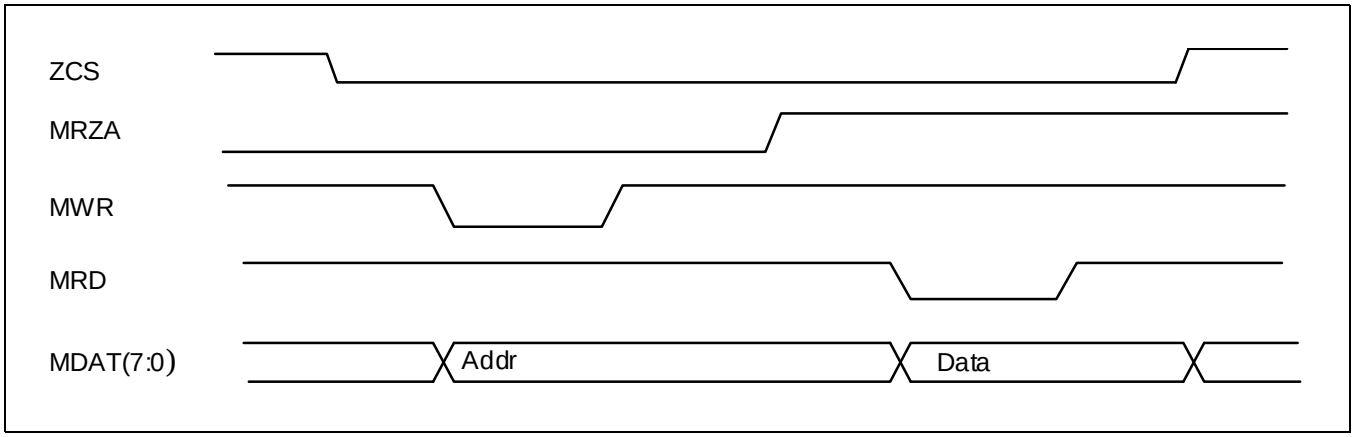


Figure 3. Read Cycle

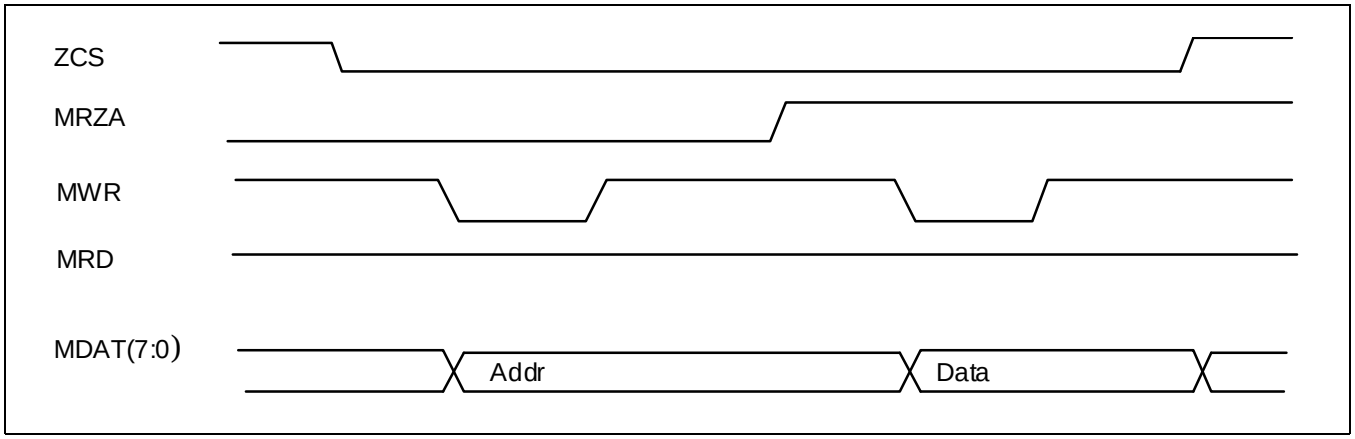


Figure 4. Write Cycle

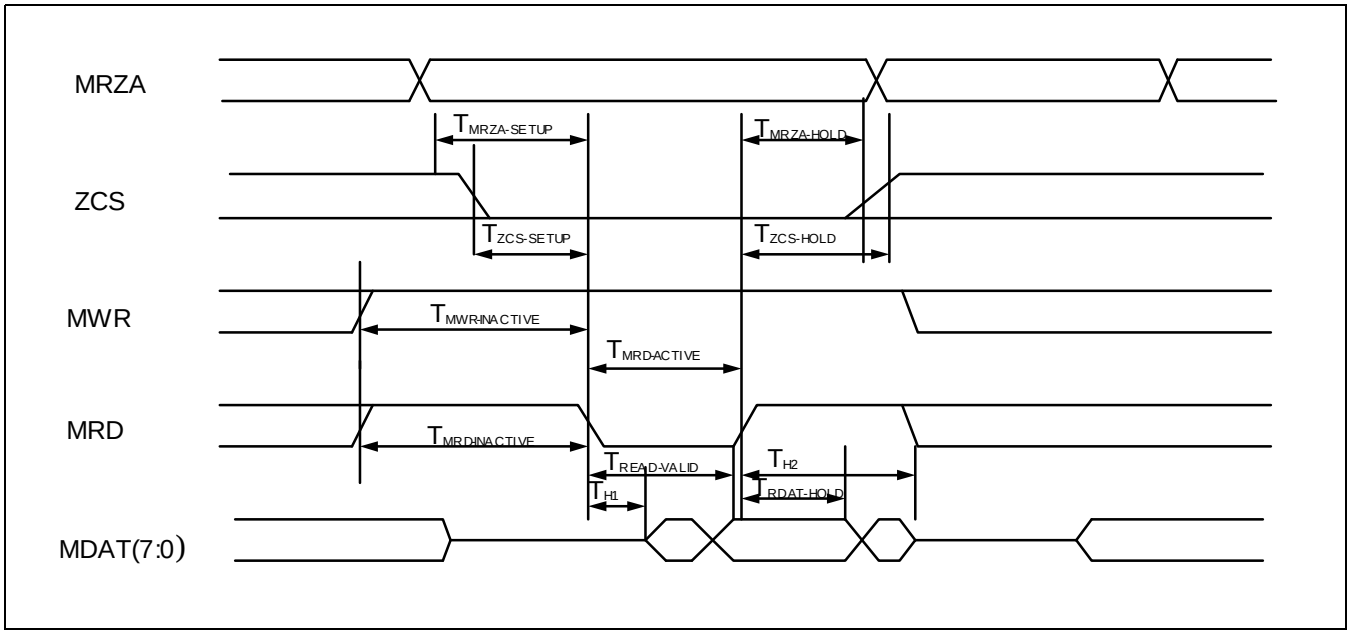


Figure 5. Read Cycle

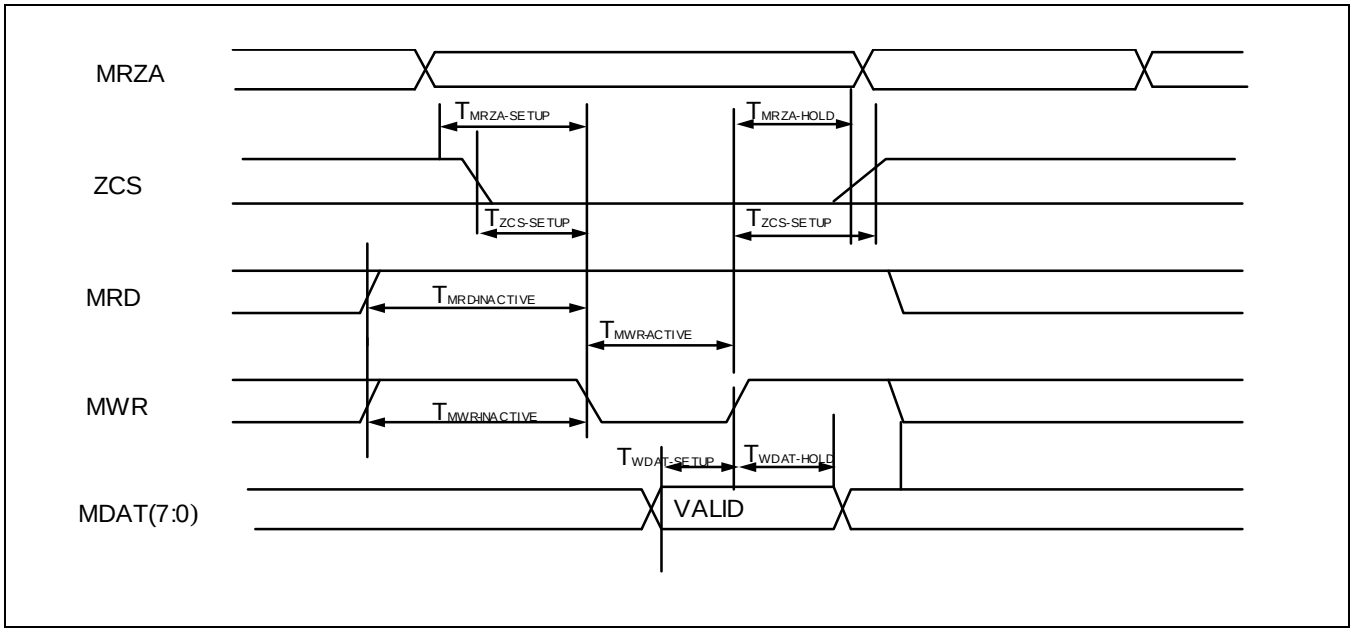


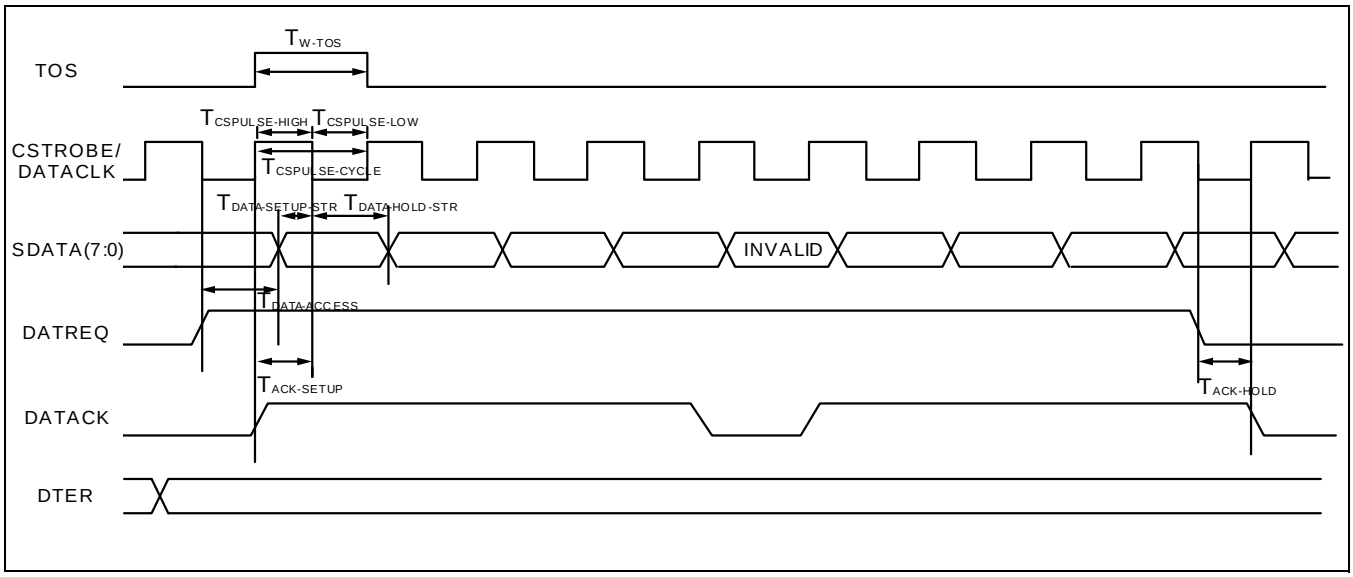
Figure 6. Write Cycle

Time	Description	Min	Max	Unit
$T_{MRZA-SETUP}$	MRZA SETUP	0		ns
$T_{MRZA-HOLD}$	MRZA HOLD	10		ns
$T_{ZCS-SETUP}$	ZCS SETUP	10		ns
$T_{ZCS-HOLD}$	ZCS HOLD	10		ns
$T_{MWR-INACTIVE}$	MWR INACTIVE	30		ns
$T_{MWR-ACTIVE}$	MWR ACTIVE PULSE WIDTH	30		ns
$T_{MRD-INACTIVE}$	MRD INACTIVE	30		ns
$T_{MRD-ACTIVE}$	MRD ACTIVE PULSE WIDTH	120		ns
$T_{READ-VALID}$	MRD ACTIVE TO READ DATA VALID		60	ns
T_{H1}	MRD ACTIVE TO MDAT(7:0) LOW IMPEDANCE	-		ns
T_{H2}	MRD INACTIVE TO MDAT(7:0) HIGH IMPEDANCE	-	-	ns
$T_{RDAT-HOLD}$	READ DATA HOLD AFTER MRD INACTIVE	10		ns
$T_{WDAT-SETUP}$	WRITE DATA SETUP	20		ns
$T_{WDAT-HOLD}$	WRITE DATA HOLD	10		ns

NOTE: There are to be no glitches in the MRZA, ZCS, MWR, and MRD signal

AV DECODER I/F

: Burst out Mode (DVD-P I/F (C-Qube) Synchronous, Samsung Multi, Sanyo)



MODE1: 2048 Bytes Main data only --> compared to MODE2 $T_{DATA-ACCESS}$ is delayed for about T.

MODE2: 2064 Bytes data in a Sector

(4 Bytes ID + 2 Bytes IEC + 6 Bytes RSV + 2048 Bytes Main Data + 4 Bytes EDC)

*DTER Signals are output in units of sectors

*Data must be taken from CSTROBE/DATACLK's falling Edge (In reverse mode, Rising edge).

*CSTROBE/DATACLK's duty cycle is not regular, and DATACK

*$T_{CSPULSE-HIGH/LOW}$: 4T

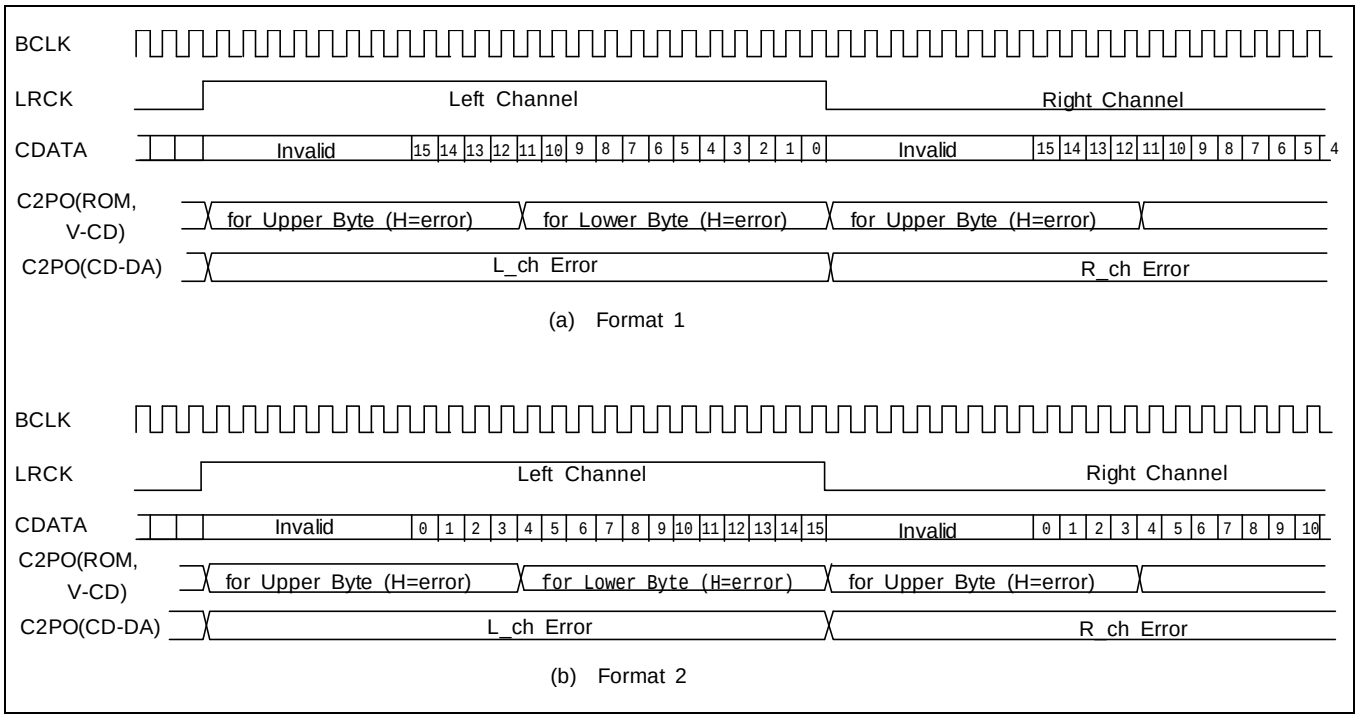
*$T_{CSPULSE-CYCLE}$: 8T (240 ns)

* CSTROBE, DATREQ, DATACK's EDGE is programmable (Reversible).

- Timing Spec

Time	Description	Min	Max	Unit
$T_{DATA-SETUP-STR}$	SDATA(7:0) Setup to CSTROBE Asserted (Synchronous)	5		ns
$T_{SDATA-D}$	SDATA(7:0) Hold from CSTROBE Asserted (Synchronous)	5		ns
T_D	Delay from DATREQ Asserted to DATACK (Asynchronous)	0		ns
$T_{ACK-LOW}$	DATACK Low Time (Asynchronous)	50		ns
T_{ACK-P}	DATACK Period	75		ns
$T_{ACK-DIS}$	DATACK Disabled Time	12		ns
$T_{SDATA-D}$	SDATA(7:0) Delay from DATACK Falling		10	ns
$T_{ACK-SETUP}$	DATACK Setup to CSTROBE (Synchronous)	5		ns
$T_{ACK-HOLD}$	DATACK Hold from CSTROBE (Synchronous)	5		ns

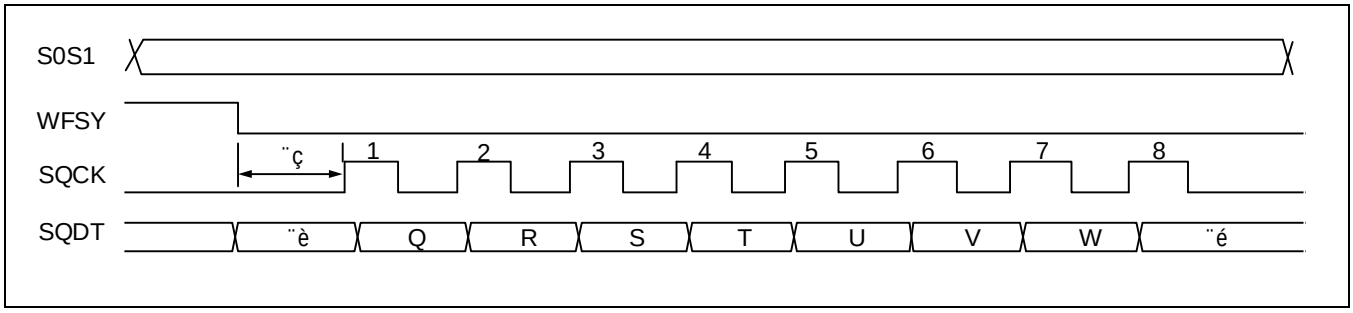
CD - DA/ CD - ROM/ V-CD DATA OUTPUT TIMING



(a) Format 1

(b) Format 2

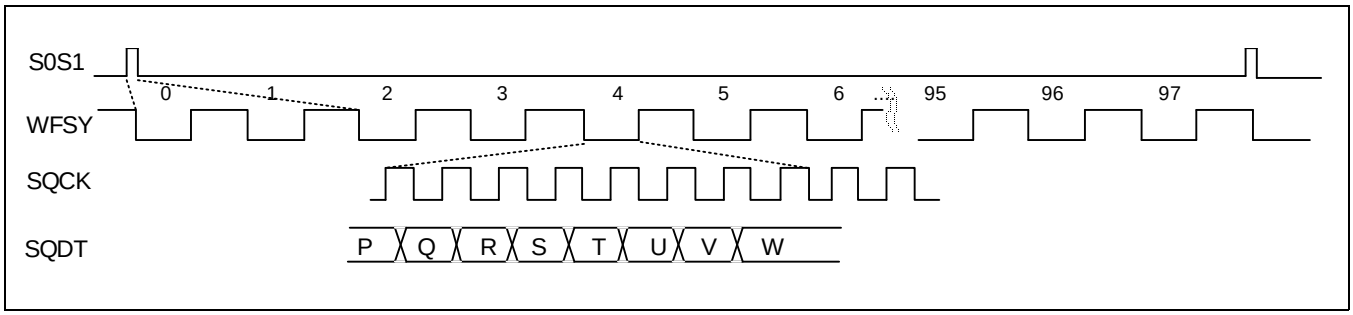
SUBCODE OUTPUT I/F (FOR CD-G)



①: After WFSY becomes falling edge, SQCK becomes 'L' during about 10 μsec.

②: If S0S1 is 'L' Subcode P is output, and if 'H' Subcode sync S0 and S1 is output.

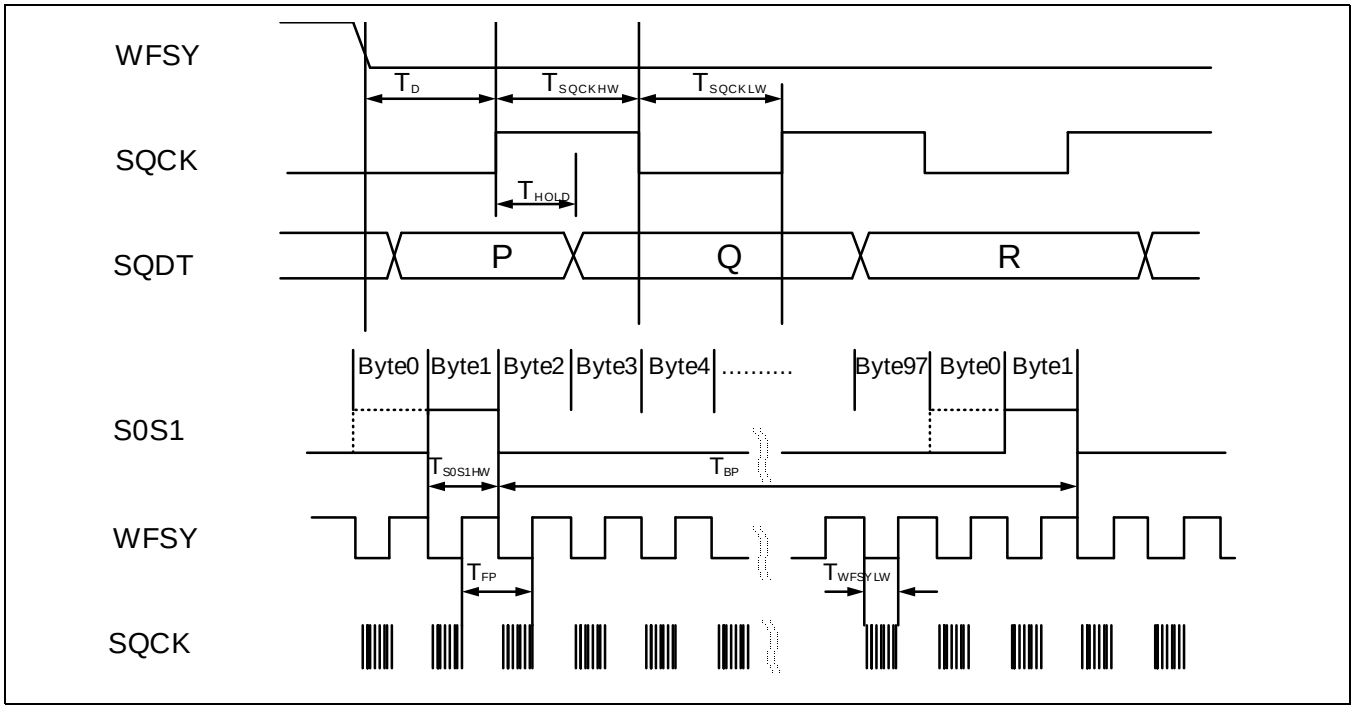
③: If pulses are input into the SQCK terminal over seven, Subcode Data (P,Q,R,S,T,U,V, W) are repeated



◆ 1 Subcode SYNC = 98 EFM Frames (1 EFM Frame = 7.35 KHz, 1 Subcode SYNC = 75 Hz)

◆ 98 EFM Frames = 2 Bytes for Subcode SYNC (S0, S1) + 96 Bytes for Subcode Data

◆ 96 Bytes Subcode Data = 1 (P) Bit × 96 + 1 (Q) Bit × 80 + 16 Bits (CRC for EDC) for CDP
+ 6 (R ~ W) Bits × 96 for CDG



Time	Description	Min	Typ	Max	Unit
T_D	Delay Time from WFSY LOW to SQCK HIGH edge for "P" Subcode bit (SQCK input)	1	-	-	µs
T_{SQCKHW}	SQCK (input) HIGH Pulse Width	1	-	3	µs
T_{SQCKLW}	SQCK (input) LOW pulse Width	1	-	3	µs
T_{HOLD}	SQDT Hold Time from SQCK HIGH	0	-	-	ns
T_{S0S1HW}	S0S1 HIGH Pulse Width	-	136	-	µs
T_{BP}	Block Period	-	13	-	ms
T_{FP}	Frame Period	-	136	-	µs
T_{WFSYLW}	WFSY LOW Pulse Width	-	68	-	µs

NOTE: Complete SQDT READ in the WFSY LOW Section (T_{WFSYLW}).

EXTERNAL DRAM MEMORY MAP

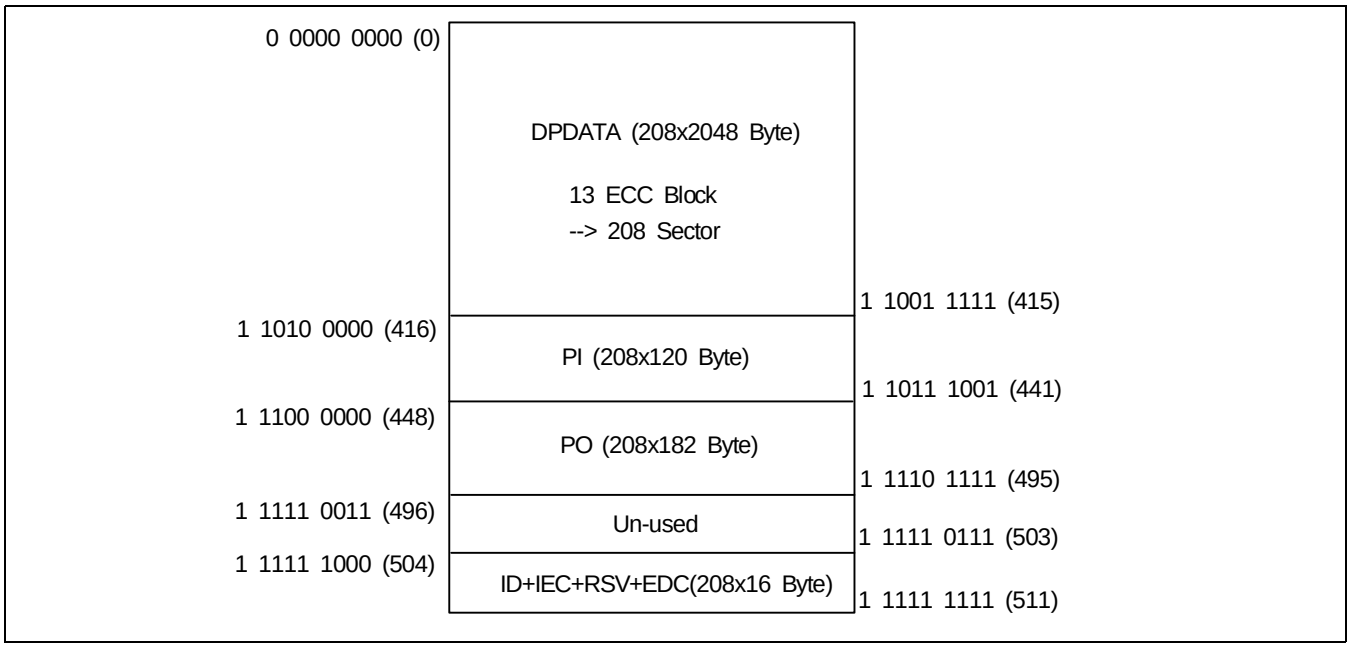
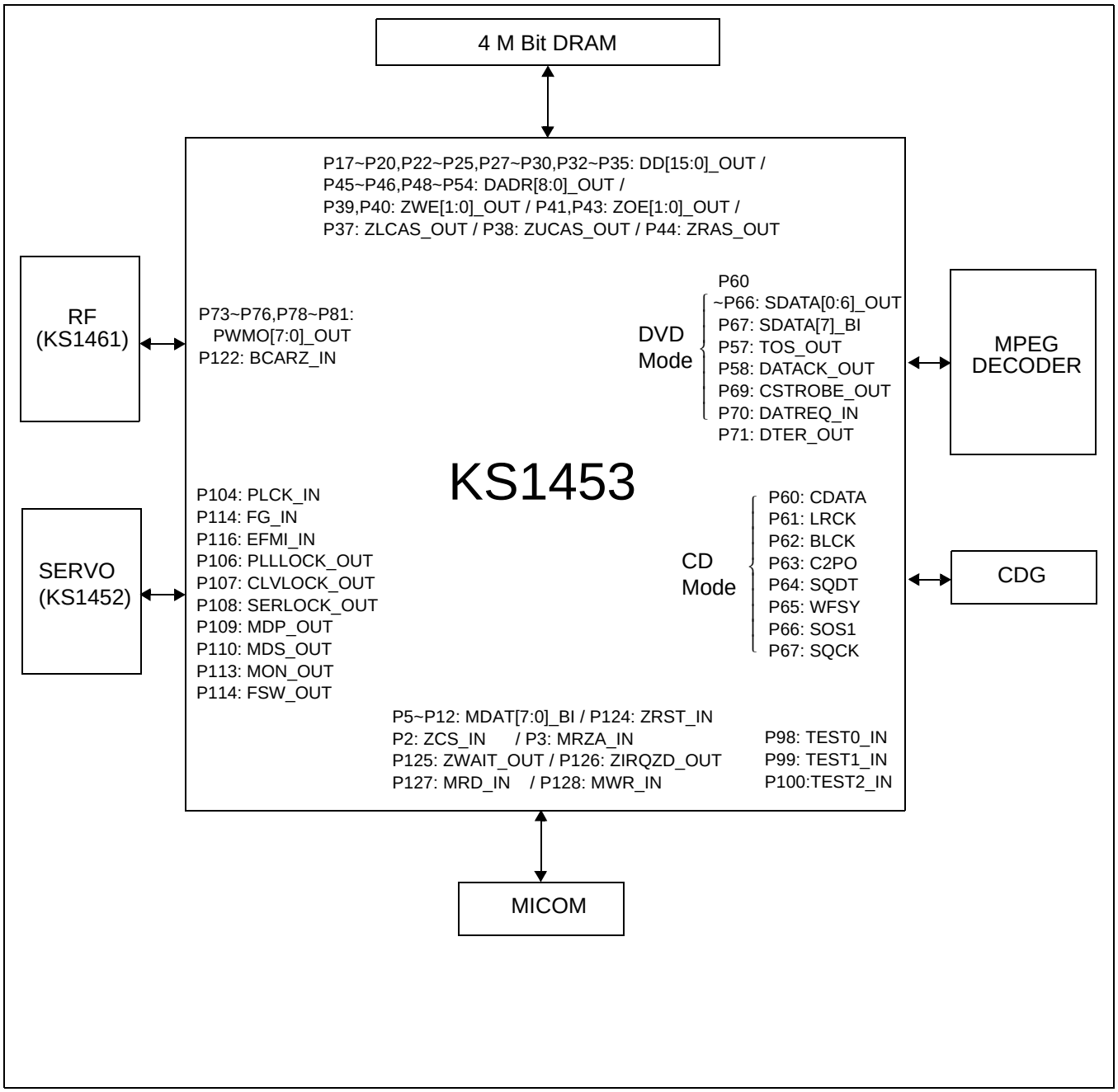


Figure 7. External DRAM Memory MAP

APPLICATION CIRCUIT



PKG INFORMATION