Document Title

1Mx4 Bit High Speed Static RAM(5V Operating). Operated at Extended and Industrial Temperature Ranges.

Revision History

<u>RevNo.</u>	<u>History</u>				Draft Data	<u>Remark</u>
Rev. 0.0	Initial release with	Preliminary.			Feb. 12. 1999	Preliminary
Rev. 1.0	1.1 Removed Low 1.2 Removed Dat 1.3 Changed IsB1	Mar. 29. 1999	Preliminary			
Rev. 2.0	2.1 Relax D.C par	rameters.			Aug. 19. 1999	Preliminary
	Iter	n	Previous	Current		
		12ns	160mA	190mA		
	Icc	15ns	155mA	185mA		
		20ns	150mA	180mA		
	2.2 Relax Absolut	e Maximum Rat	ing.			

Item	Previous	Current
Voltage on Any Pin Relative to Vss	-0.5 to 7.0	-0.5 to Vcc+0.5

Rev. 3.0 3.1 Delete Preliminary

3.2 Update D.C parameters and 10ns part.

		Previous		Current				
	Icc	lsb	sb1	lcc	lsb	sb1		
10ns	-		20mA	160mA		10mA		
12ns	190mA	70mA		150mA	60mA			
15ns	185mA			140mA	UUIIA			
20ns	ns 180mA	+	130mA					

3.3 Added Extended temperature range

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.



Mar. 27. 2000 Final

1M x 4 Bit (with OE)High-Speed CMOS Static RAM

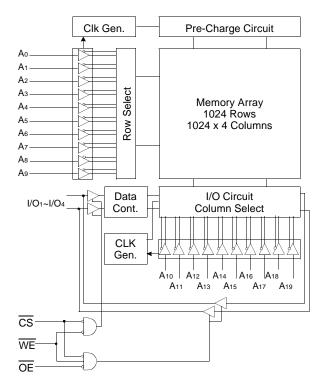
FEATURES

- Fast Access Time 10,12,15,20ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 60mA(Max.)
 - (CMOS) : 10mA(Max.)
 - Operating KM644002C 10 : 160mA(Max.) KM644002C - 12 : 150mA(Max.) KM644002C - 15 : 140mA(Max.) KM644002C - 20 : 130mA(Max.)
- Single 5.0V ±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
- No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
 - KM644002CJ : 32-SOJ-400

ORDERING INFORMATION

KM644002C - 10/12/15/20	Commercial Temp.				
KM644002CE - 10/12/15/20	Extended Temp.				
KM644002CI - 10/12/15/20	Industrial Temp.				

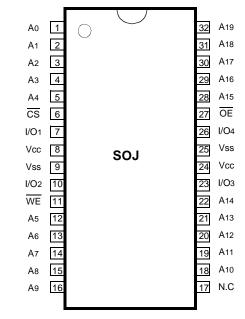
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM644002C is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM644002C uses 4 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM644002C is packaged in a 400 mil 32-pin plastic SOJ.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to Vcc+0.5	V
Voltage on Vcc Supply Relative to Vss		Vcc	-0.5 to 7.0	V
Power Dissipation		PD	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	ТА	0 to 70	٥C
	Extended	TA	-25 to 85	٥C
	Industrial	ТА	-40 to 85	٥C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*(TA=0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	Vih	2.2	-	Vcc+0.5***	V
Input Low Voltage	VIL	-0.5**	-	0.8	V

* The above parameters are also guaranteed at industrial temperature range.

** VIL(Min) = -2.0V a.c(Pulse Width $\leq 8ns$) for I $\leq 20mA$.

*** VIH(Max) = Vcc + 2.0V a.c (Pulse Width \leq 8ns) for I \leq 20mA.

DC AND OPERATING CHARACTERISTICS*(TA=0 to 70°C, Vcc=5.0V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	Iц	VIN=Vss to Vcc		-2	2	μA
Output Leakage Current	ILO	CS=VIH or OE=VIH or WE=VIL VOUT=Vss to Vcc	-2	2	μΑ	
Operating Current			10ns	-	160	mA
		CS=VIL, VIN=VIH or VIL, IOUT=0mA	12ns	-	150	
			15ns	-	140	
			20ns	-	130	
Standby Current	lsв	Min. Cycle, CS=Vін	U	-	60	mA
	ISB1 f=0MHz, CS≥Vcc-0.2V, VIN≥Vcc-0.2V or VIN≤0.2V			-	10	
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level	Vон	Iон=-4mA		2.4	-	V
	V0H1**	Іон1=-0.1mA		-	3.95	V

* The above parameters are also guaranteed at industrial temperature range.

** Vcc=5.0V±5%, Temp.=25°C.

CAPACITANCE*(TA=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	Ci/O	VI/O=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	7	pF

* Capacitance is sampled and not 100% tested.



AC CHARACTERISTICS(TA=0 to 70°C, Vcc=5.0V±10%, unless otherwise noted.)

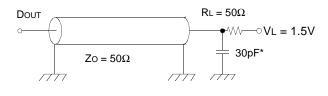
TEST CONDITIONS*

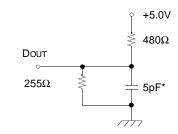
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

* The above test conditions are also applied at industrial temperature range.

Output Loads(A)

Output Loads(B) for tHz, tLz, tWHz, tOW, tOLz & tOHz





* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE*

Parameter	Symbol	KM644	002C-10	KM644002C-12		KM644002C-15		KM644002C-20		Unit
Falameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	10	-	12	-	15	-	20	-	ns
Address Access Time	tAA	-	10	-	12	-	15	-	20	ns
Chip Select to Output	tco	-	10	-	12	-	15	-	20	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	-	8	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tolz	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	0	9	ns
Output Disable to High-Z Output	tonz	0	5	0	6	0	7	0	9	ns
Output Hold from Address Change	tон	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	10	-	12	-	15	-	20	ns

* The above parameters are also guaranteed at industrial temperature range.



KM644002C, KM644002CE, KM644002CI

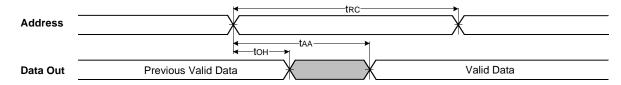
WRITE CYCLE*

Deremeter	Symbol	KM644002C-10		KM644	KM644002C-12		KM64400C-15		KM644002C-20	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	twc	10	-	12	-	15	-	20	-	ns
Chip Select to End of Write	tcw	7	-	8	-	10	-	12	-	ns
Address Set-up Time	tas	0	-	0	-	0	-	0	-	ns
Address Valid to End of	taw	7	-	8	-	10	-	12	-	ns
Write Pulse Width(OE High)	twp	7	-	8	-	10	-	12	-	ns
Write Pulse Width(OE Low)	tWP1	10	-	12	-	15	-	20	-	ns
Write Recovery Time	twr	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	twnz	0	5	0	6	0	7	0	9	ns
Data to Write Time Overlap	tDW	5	-	6	-	7	-	9	-	ns
Data Hold from Write Time	tdн	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tow	3	-	3	-	3	-	3	-	ns

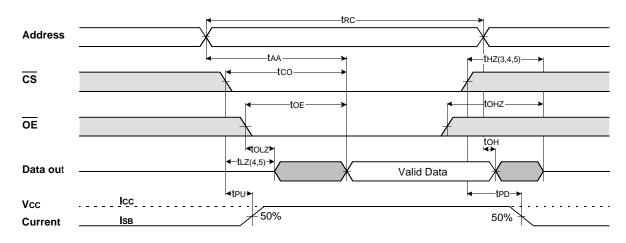
* The above parameters are also guaranteed at industrial temperature range.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

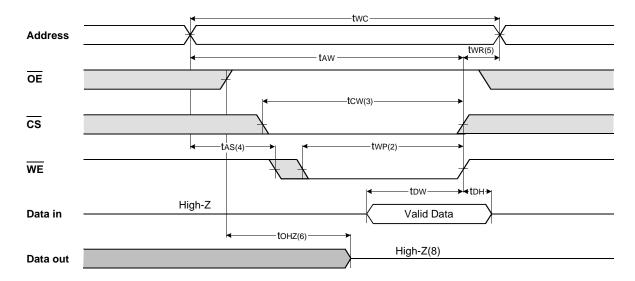


NOTES(READ CYCLE)

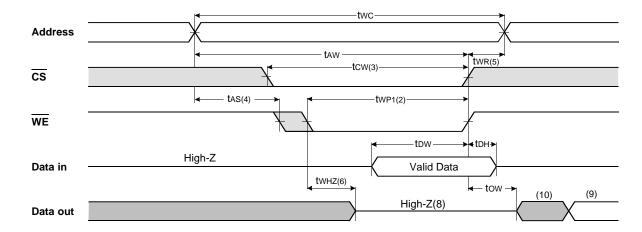
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHz and toHz are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL levels.
- 4. At any given temperature and voltage condition, tHz(Max.) is less than tLz(Min.) both for a given device and from device to device.
- Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
 Device is continuously selected with CS=VIL
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.



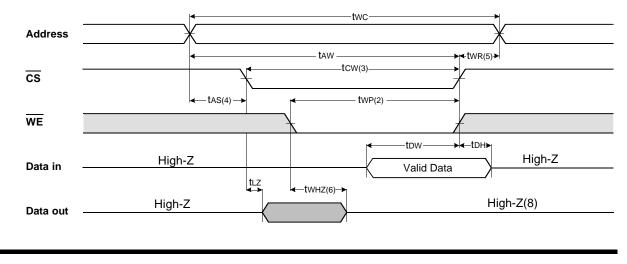
TIMING WAVEFORM OF WRITE CYCLE(1) (OE= Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS=Controlled)





NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address. 2. A write occurs during the overlap of a low CS and WE. A write begins at the latest transition CS going low and WE going low ; A write ends at the earliest transition CS going high or WE going high. twp is measured from the beginning of write to the end of write. 3. tcw is measured from the later of CS going low to end of write.

- 4. tas is measured from the address valid to the beginning of write.
- 5. tw<u>R</u> is <u>measured from</u> the end of write to the address change. twR applied in case a write ends as \overline{CS} or \overline{WE} going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.

7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.

9. Dout is the read data of the new address.

10. When CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	OE	Mode	I/O Pin	Supply Current
н	Х	Х*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	Icc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	DIN	Icc

* X means Don't Care.



PACKAGE DIMENSIONS

Units:millimeters/Inches

32-SOJ-400

