

## Document Title

128Kx8 bit Low Power and Low Voltage CMOS Static RAM

## Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	September 10, 1998	Preliminary
1.0	Finalize	April 12, 1999	Final

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## 128Kx8 bit Low Power and Low Voltage CMOS Static RAM

### FEATURES

- Process Technology: TFT
- Organization: 128Kx8
- Power Supply Voltage: 2.3V ~ 2.7V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-TSOP1-0820F, 32-TSOP1-0813.4F

### GENERAL DESCRIPTION

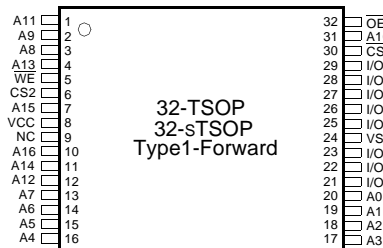
The K6T1008S2E families are fabricated by SAMSUNG's advanced CMOS process technology. The families support industrial operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Max)	Operating (I <sub>CC2</sub> , Max)	
K6T1008S2E-F	Industrial(-40~85°C)	2.3~2.7V	85 <sup>1)</sup> /100ns	10μA	15mA	32-TSOP1-0820F 32-TSOP1-0813.4F

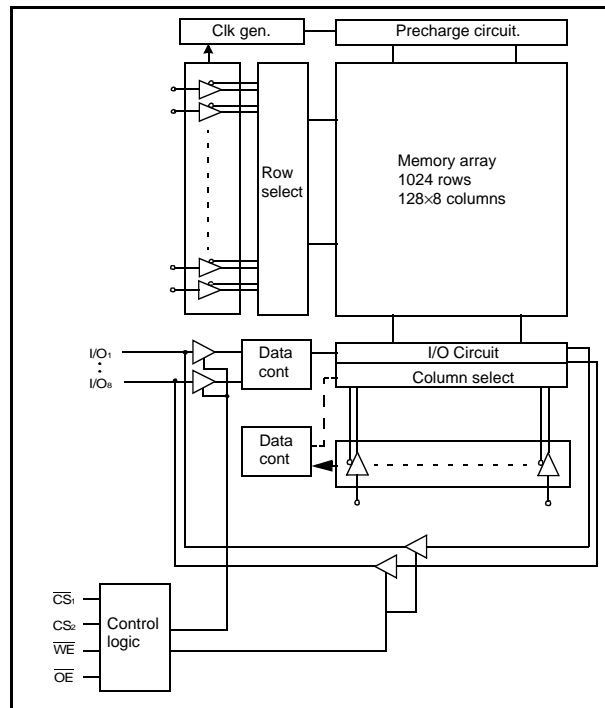
1. The parameters are tested with 30pF test load

### PIN DESCRIPTION



Name	Function
A0~A16	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}, \overline{CS2}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C.	No Connection

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K6T1008S2E-TF85	32-TSOP F, 85ns, 2.5V
K6T1008S2E-TF10	32-TSOP F, 100ns, 2.5V
K6T1008S2E-YF85	32-sTSOP F, 85ns, 2.5V
K6T1008S2E-YF10	32-sTSOP F, 100ns, 2.5V

## FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	$\overline{CS}_2$	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.3 to 4.0	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	-40 to 85	°C	K6T1008S2E-P

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	K6T1008S2E Family	2.3	2.5	2.7	V
Ground	V <sub>SS</sub>	All Family	0	0	0	V
Input high voltage	V <sub>IH</sub>	K6T1008S2E Family	2.0	-	V <sub>CC</sub> +0.3	V
Input low voltage	V <sub>IL</sub>	K6T1008S2E Family	-0.3 <sup>3)</sup>	-	0.6	V

Note:

1. T<sub>A</sub>=-40 to 85°C, otherwise specified
2. Overshoot : V<sub>CC</sub>+1.0V in case of pulse width≤20ns
3. Undershoot : -1.0V in case of pulse width≤20ns
4. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

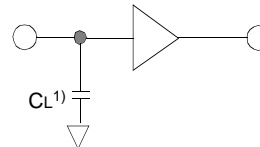
## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , Read	-	-	1	mA
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100%duty, I <sub>IO</sub> =0mA, $\overline{CS}_1\leq 0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤0.2V	-	-	2	mA
	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	15	mA
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =0.5mA	-	-	0.4	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-0.5mA	2.0	-	-	V
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}_1=V_{IH}$ , CS <sub>2</sub> =V <sub>IL</sub> , Other inputs=V <sub>IH</sub> or V <sub>IL</sub>	-	-	0.3	mA
Standby Current(CMOS)	I <sub>SB1</sub>	$\overline{CS}_1\geq V_{CC}-0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V or CS <sub>2</sub> ≤0.2V, Other inputs=0~V <sub>CC</sub>	-	0.2	10	μA

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V  
 Input rising and falling time : 5ns  
 Input and output reference voltage : 1.1V  
 Output load(see right) :  $C_L=100\text{pF}+1\text{TTL}$   
 $C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

## AC CHARACTERISTICS ( $V_{CC}=2.3\sim 2.7\text{V}$ , $T_A=-40$ to $85^\circ\text{C}$ )

Parameter List		Symbol	Speed Bins				Units
			85ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	85	-	100	-	ns
	Address access time	t <sub>AA</sub>	-	85	-	100	ns
	Chip select to output	t <sub>CO1</sub> , t <sub>CO2</sub>	-	85	-	100	ns
	Output enable to valid output	t <sub>OE</sub>	-	40	-	50	ns
	Chip select to low-Z output	t <sub>LZ</sub>	10	-	10	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	ns
	Chip disable to high-Z output	t <sub>HZ</sub>	0	25	0	30	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	0	25	0	30	ns
	Output hold from address change	t <sub>OH</sub>	10	-	15	-	ns
Write	Write cycle time	t <sub>WC</sub>	85	-	100	-	ns
	Chip select to end of write	t <sub>CW</sub>	70	-	80	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	70	-	80	-	ns
	Write pulse width	t <sub>WP</sub>	60	-	70	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	25	0	30	ns
	Data to write time overlap	t <sub>DW</sub>	35	-	40	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	ns
	End write to output low-Z	t <sub>OW</sub>	5	-	5	-	ns

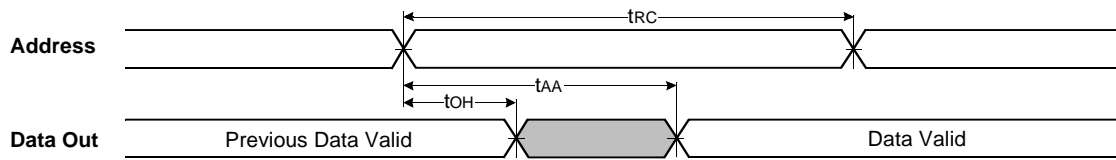
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{CS}_1 \geq V_{CC}-0.2\text{V}^1$	2.0	-	2.7	V
Data retention current	I <sub>DR</sub>	$V_{CC}=2.5\text{V}$ , $\overline{CS}_1 \geq V_{CC}-0.2\text{V}^1$	-	0.2	10	μA
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms
Recovery time	t <sub>RDR</sub>		5	-	-	

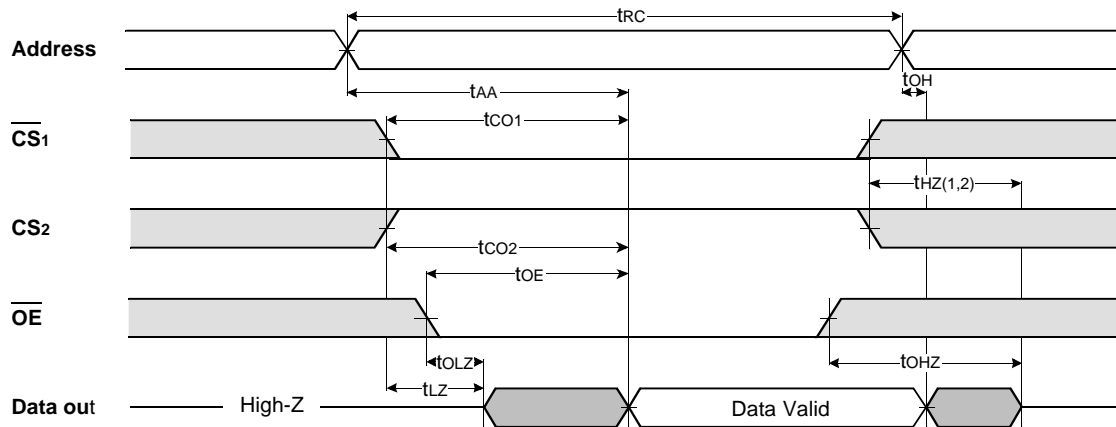
1.  $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$ ,  $\overline{CS}_2 \geq V_{CC}-0.2\text{V}$  ( $\overline{CS}_1$  controlled) or  $\overline{CS}_2 \leq 0.2\text{V}$  ( $\overline{CS}_2$  controlled)

## TIMMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS1}=\overline{OE}=V_{IL}$ ,  $CS2=\overline{WE}=V_{IH}$ )



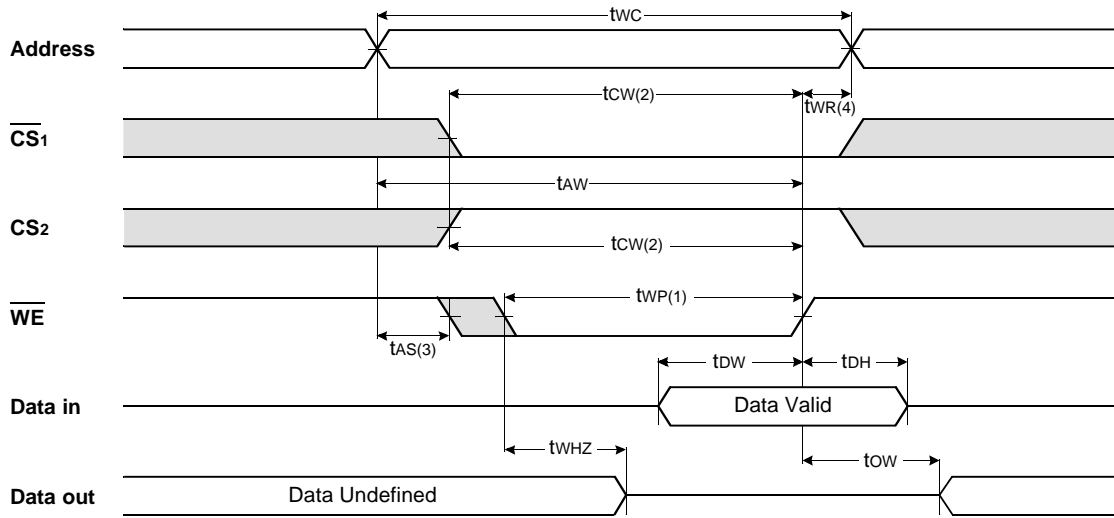
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE}=V_{IH}$ )



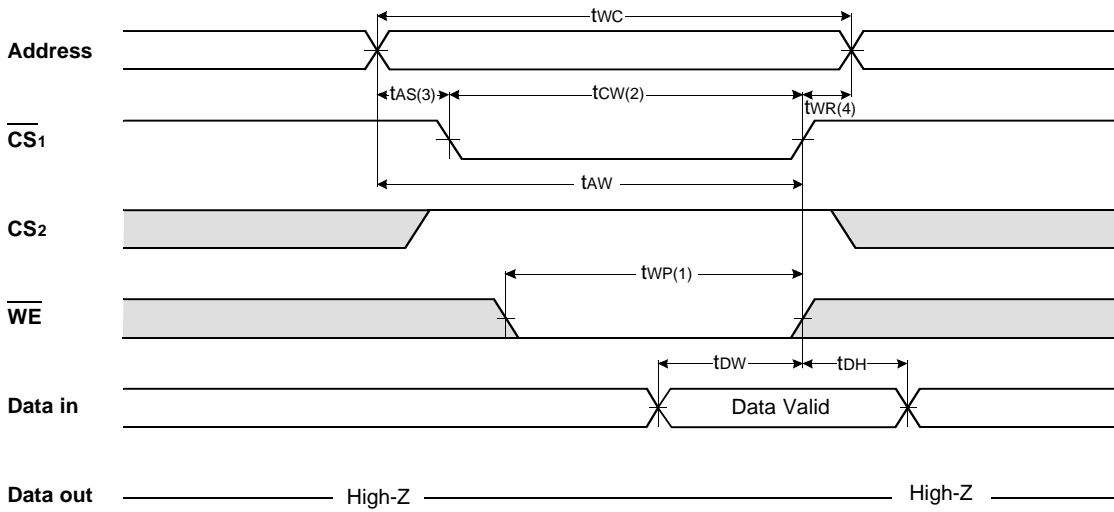
**NOTES (READ CYCLE)**

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS<sub>2</sub> Controlled)

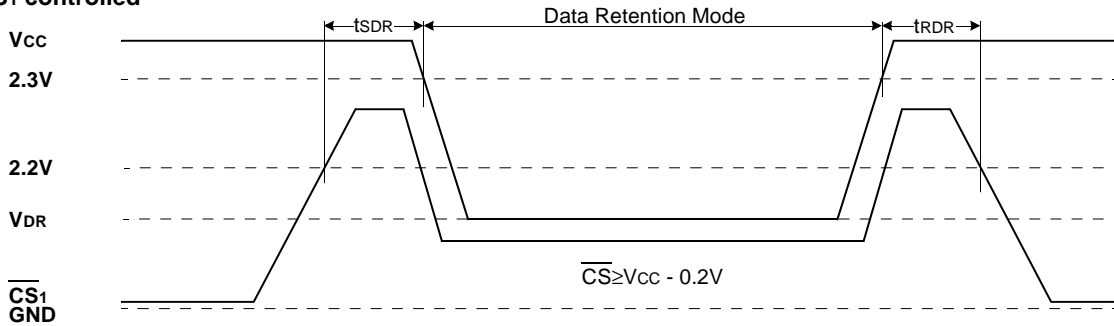


NOTES (WRITE CYCLE)

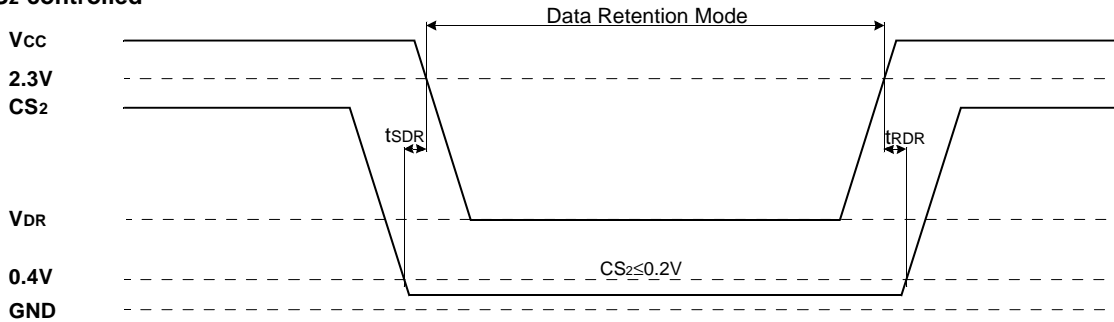
1. A write occurs during the overlap of a low  $\overline{CS}_1$ , a high  $CS_2$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  goes low,  $CS_2$  going high and  $\overline{WE}$  going low : A write ends at the earliest transition among  $\overline{CS}_1$  going high,  $CS_2$  going low and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}_1$  going low or  $CS_2$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR1}$  applied in case a write ends as  $\overline{CS}_1$  or  $\overline{WE}$  going high  $t_{WR2}$  applied in case a write ends as  $CS_2$  going to low.

DATA RETENTION WAVE FORM

CS<sub>1</sub> controlled



CS<sub>2</sub> controlled

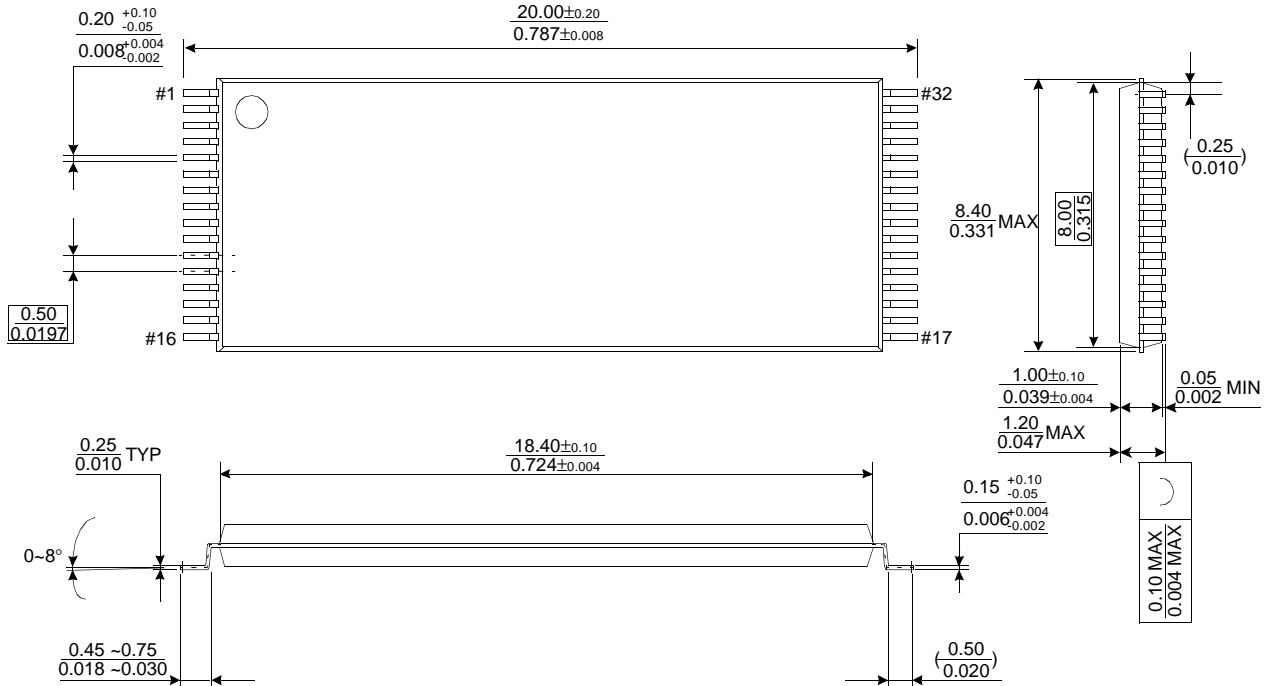




## PACKAGE DIMENSIONS

Units: millimeters(inches)

### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)

