

K4C89183AF

288Mb x18 Network-DRAM2 Specification
Version 0.7

K4C89183AF

Revision History

Version 0.0 (Oct. 2002)

- First Release

Version 0.01 (Nov. 2002)

- Changed die revision from D-die to F-die
- Corrected typo
- Corrected DQS to DS and QS(DQS -> DS and QS) in AC timing table and timing diagram.

Version 0.1 (Apr. 2003)

- Added 800Mbps(400Mhz) product
- Changed operating temperature from Ta to Tc.
- Changed capacitance of ADDR/CMD/CLK

| | From | | To | |
|--------------|------|-----|-----|-----|
| | Min | Max | Min | Max |
| Addr/CMD/CLK | 1.5 | 2.5 | 1.5 | 3.0 |

- Changed tDSS(DS input Falling Edge to Clock Setup Time)

| | From | | | To | | | |
|-----|------|-----|-----|------|------|-----|-----|
| | F6 | FB | F5 | G7 | F6 | FB | F5 |
| CL4 | 0.9 | 0.9 | 1.0 | 0.75 | 0.75 | 0.8 | 1.0 |
| CL5 | 0.9 | 0.9 | 1.0 | 0.75 | 0.75 | 0.8 | 1.0 |
| CL6 | 0.9 | 0.9 | 1.0 | 0.75 | 0.75 | 0.8 | 1.0 |
| CL7 | - | - | - | 0.75 | - | - | - |

- Added CL7 for 800Mbps
- Deleted TSOP package outline

Version 0.11 (Apr. 2003)

- Corrected typo in page 3.(Deleted bi-directional strobe)
- Corrected min. Vref to VDDQ/2x95% in page 7

Version 0.2 (Aug. 2003)

- Added package physical dimension
- Extracted 800Mbps(G7) binning from target spec (G7 will be added in the future)
- Changed DC test condition

| From | To | Changed point |
|-----------------------------|------------------------------|-------------------|
| IDD1S,IDD2N,IDD2P,IDD5,IDD6 | IDD1S,IDD2N,IDD2P,IDD5B,IDD6 | Changed condition |
| - | IDD4W, IDD4R | newly inserted |

- Changed low frequency spec like below

| Unit : ns | From | | | To | | |
|--------------|------|-----|-----|-----|-----|-----|
| | F6 | FB | F5 | F6 | FB | F5 |
| tCK max@CL=4 | 7.5 | 7.5 | 7.5 | 6.0 | 6.0 | 6.0 |
| tCK max@CL=5 | 7.5 | 7.5 | 7.5 | 6.0 | 6.0 | 6.0 |
| tCK max@CL=6 | 7.5 | 7.5 | 7.5 | 6.0 | 6.0 | 6.0 |

- Changed AC test load picture

Version 0.3 (Nov. 2003)

- Changed Package type from die-exposed to full molded
- Changed Package code in Partnumber

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Version 0.31 (Mar., 2004)

- Corrected typo. in page 7 (Changed operating Temperature to 85°C, case temperature)

Version 0.4 (Jun., 2004)

- Changed from "target" to "Preliminary"
- Changed min. t_{CK@CL5} to 3.5ns in "-F6"

| | | From | To |
|--|--------|---------|--------|
| | | F6 | F6 |
| t _{CK} Clock Cycle Time (min) | CL = 4 | 4.0 ns | 4.0 ns |
| | CL = 5 | 3.33 ns | 3.5 ns |
| | CL = 6 | 3.0ns | 3.0ns |

Version 0.5 (Aug., 2004)

- Deleted self-refresh function and BL2 from spec

Version 0.51 (Aug., 2004)

- Corrected error in page 54, "Package Out line Drawing". (Just 4 balls were missing in drawing)

Version 0.6 (Nov., 2004)

- Deleted "preliminary"
- Changed current value in page 9

Version 0.7 (Jan., 2005)

- Deleted the t_{DQSQA} in page 11
- Deleted the t_{SSK} in page 11

K4C89183AF

4,194,304-WORDS x 4 BANKS x 18-BITS DOUBLE DATA RATE Network-DRAM

DESCRIPTION

K4C89183AF is a CMOS Double Data Rate Network-DRAM containing 301,989,888 memory cells. K4C89183AF is organized as 4,194,304-words x 4 banks x 18 bits. K4C89183AF feature a fully synchronous operation referenced to clock edge whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. K4C89183AF can operate fast core cycle compared with regular DDR SDRAM.

K4C89183AF is suitable for Server, Network and other applications where large memory density and low power consumption are required. The Output Driver for Network-DRAM is capable of high quality fast data transfer under light loading condition.

FEATURES

| Parameter | | K4C89183AF | | |
|---|--------|------------|---------|--------|
| | | F6 | FB | F5 |
| t _{CK} Clock Cycle Time (min) | CL = 4 | 4.0 ns | 4.5 ns | 5.0 ns |
| | CL = 5 | 3.5 ns | 3.75 ns | 4.5 ns |
| | CL = 6 | 3.0ns | 3.33 ns | 4.0 ns |
| t _{RC} Random Read/Write Cycle Time (min) | | 20.0 ns | 22.5 ns | 25 ns |
| t _{RAC} Random Access Time (min) | | 20.0 ns | 22.5 ns | 25 ns |
| I _{DD1S} Operating Current (single bank) (max) | | 320mA | 300mA | 280mA |
| I _{DD2P} Power Down Current (max) | | 70mA | 65mA | 60mA |

- Fully Synchronous Operation
 - Double Data Rate (DDR)
 - Data input/output are synchronized with both edges of DS / QS.
 - Differential Clock (CLK and CLK) inputs
 - \overline{CS} , FN and all address input signals are sampled on the positive edge of CLK.
 - Output data (DQs and QS) is aligned to the crossings of CLK and CLK.
- Fast clock cycle time of 3.0 ns minimum
 - Clock : 333 MHz maximum
 - Data : 666 Mbps/pin maximum
- Quad Independent Banks operation
- Fast cycle and Short Latency
- Uni-directional Data Strobe
- Distributed Auto-Refresh cycle in 3.9us
- Power Down Mode
- Variable Write Length Control
- Write Latency = CAS Latency-1
- Programmable CAS Latency and Burst Length
 - CAS Latency = 4, 5, 6
 - Burst Length = 4
- Organization : 4,194,304 words x 4 banks x 18 bits
- Power Supply Voltage V_{DD} : 2.5V ± 0.125V
- V_{DDQ} : 1.4V ~ 1.9V
- 1.8V CMOS I/O comply with SSTL - 1.8 (half strength driver) and HSTL
- Package : 60Ball BGA, 1.0mm x 1.0mm Ball pitch
- Notice : Network-DRAM is trademark of Samsung Electronics., Co LTD

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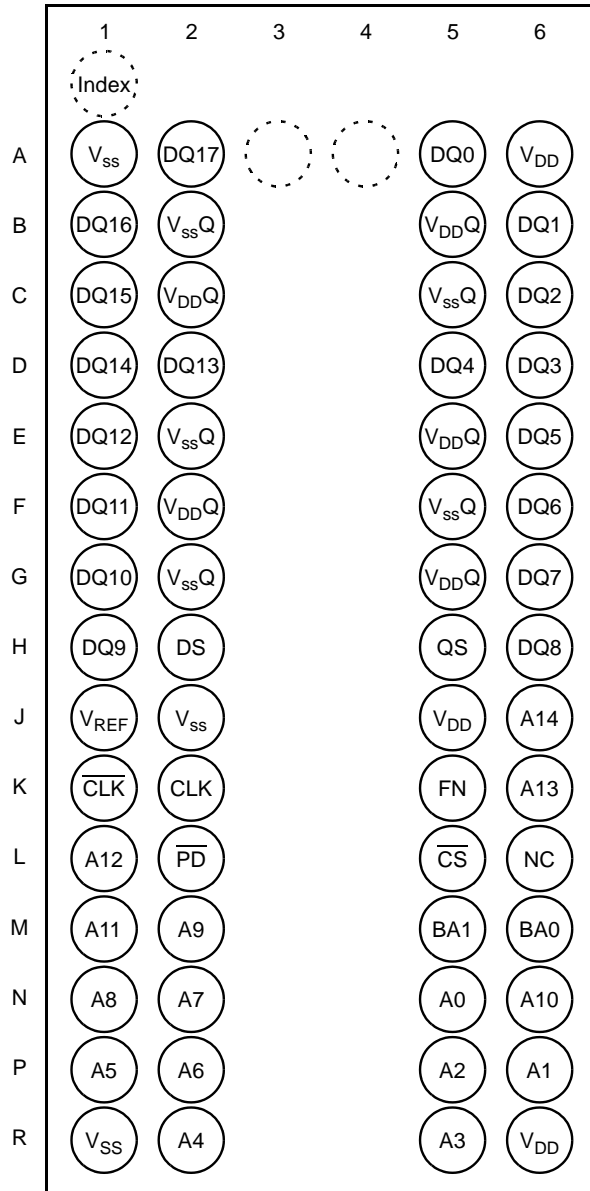
Pin Names

| Pin | Name |
|-----------------------|-----------------------------------|
| A0 ~ A14 | Address Input |
| BA0, BA1 | Bank Address |
| DQ0 ~ DQ17 | Data Input/Output |
| \overline{CS} | Chip Select |
| FN | Function Control |
| \overline{PD} | Power Down Control |
| CLK, \overline{CLK} | Clock Input |
| DS/QS | Write/Read data strobe |
| VDD | Power (+2.5V) |
| V _{SS} | Ground |
| V _{DDQ} | Power (+1.8V) (for I/O buffer) |
| V _{SSQ} | Ground (for I/O buffer) |
| V _{REF} | Reference Voltage |
| NC | No Connection |

PIN ASSIGNMENT (TOP VIEW)

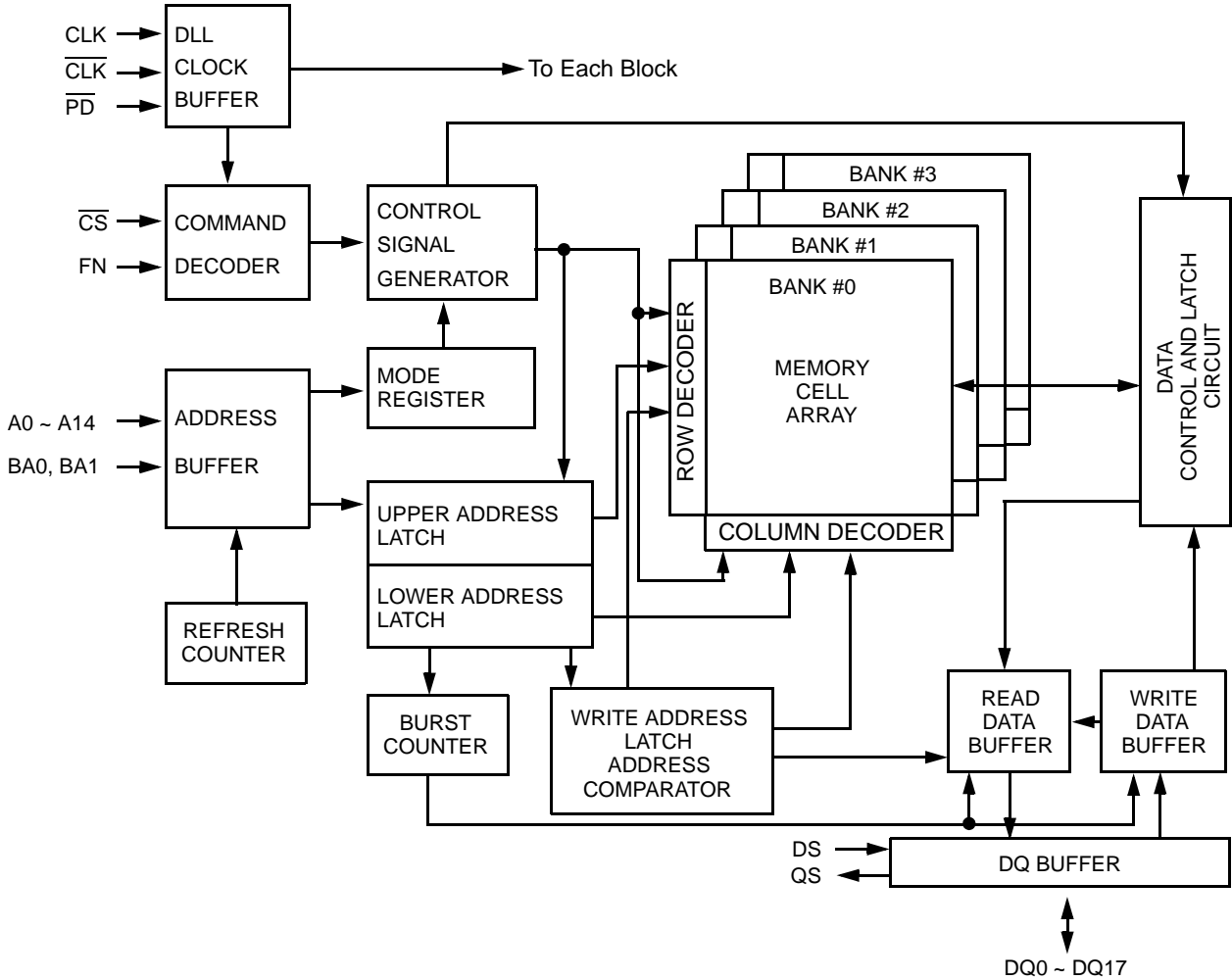
ball pitch=1.0 x 1.0mm

x18



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Block Diagram



Note : The K4C89183AD configuration is 4 Bank of 32768 x 128 x 18 of cell array with the DQ pins numbered DQ0~DQ17.

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Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units | Notes |
|---------------------|---------------------------------------|-------------------------------|-------|------------|
| V _{DD} | Power Supply Voltage | -0.3 ~ 3.3 | V | |
| V _{DDQ} | Power Supply Voltage (for I/O buffer) | -0.3 ~ V _{DD} + 0.3 | V | |
| V _{IN} | Input Voltage | -0.3 ~ V _{DD} + 0.3 | V | |
| V _{OUT} | DQ pin Voltage | -0.3 ~ V _{DDQ} + 0.3 | V | |
| V _{REF} | Input Reference Voltage | -0.3 ~ V _{DDQ} + 0.3 | V | |
| T _{OPR} | Operating Temperature | 0 ~ 85 | °C | Case Temp. |
| T _{STG} | Storage Temperature | -55 ~ 150 | °C | |
| T _{SOLDER} | Soldering Temperature(10s) | 260 | °C | |
| P _D | Power Dissipation | 2 | W | |
| I _{OUT} | Short Circuit Output Current | ± 50 | mA | |

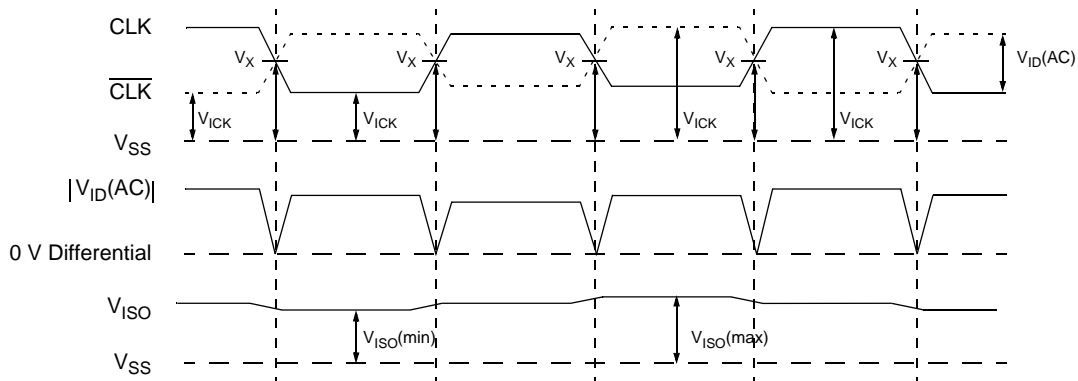
Caution : Conditions outside the limits listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may affect device reliability.

Recommended DC,AC Operating Conditions (Notes : 1) (T_{case} = 0 ~ 85 °C)

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|-----------------------|---|---------------------------|---------------------|---------------------------|-------|-------|
| V _{DD} | Power Supply Voltage | 2.375 | 2.5 | 2.625 | V | |
| V _{DDQ} | Power Supply Voltage (for I/O Buffer) | 1.7 | 1.8 | 1.9 | V | |
| V _{REF} | Input Reference Voltage | V _{DDQ} /2x95% | V _{DDQ} /2 | V _{DDQ} /2x105% | V | 2 |
| V _{IH} (DC) | Input DC high Voltage | V _{REF} +0.125 | - | V _{DDQ} +0.2 | V | 5 |
| V _{IL} (DC) | Input DC Low Voltage | -0.1 | - | V _{REF} -0.125 | V | 5 |
| V _{ICK} (DC) | Differential Clock DC Input Voltage | -0.1 | - | V _{DDQ} +0.1 | V | 10 |
| V _{ID} (DC) | Input Differential Voltage. CLK and $\overline{\text{CLK}}$ Inputs (DC) | 0.4 | - | V _{DDQ} +0.2 | V | 7,10 |
| V _{IH} (AC) | Input AC High Voltage | V _{REF} +0.2 | - | V _{DDQ} +0.2 | V | 3,6 |
| V _{IL} (AC) | Input AC Low Voltage | -0.1 | - | V _{REF} -0.2 | V | 4,6 |
| V _{ID} (AC) | Input Differential Voltage. CLK and $\overline{\text{CLK}}$ Inputs (AC) | 0.55 | - | V _{DDQ} +0.2 | V | 7,10 |
| V _X (AC) | Differential AC Input Cross Point Voltage | V _{DDQ} /2-0.125 | - | V _{DDQ} /2+0.125 | V | 8,10 |
| V _{ISO} (AC) | Differential Clock AC Middle Level | V _{DDQ} /2-0.125 | - | V _{DDQ} /2+0.125 | V | 9,10 |

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- Notes:**
1. All voltages are referenced to Vss, VssQ.
 2. V_{REF} is expected to track variations in VddQ DC level of the transmitting device.
Peak to peak AC noise on V_{REF} may not exceed $\pm 2\%$ of V_{REF} (DC).
 3. Overshoot limit : $V_{IH(max.)} = V_{DDQ} + 0.7V$ with a pulse width $\leq 5ns$
 4. Undershoot limit : $V_{IL(min.)} = -0.7V$ with a pulse width $\leq 5ns$
 5. $V_{IH(DC)}$ and $V_{IL(DC)}$ are levels to maintain the current logic state.
 6. $V_{IH(AC)}$ and $V_{IL(AC)}$ are levels to change to the new logic state.
 7. V_{ID} is magnitude of the difference between CLK input level and \overline{CLK} input level.
 8. The value of $V_x(AC)$ is expected to equal $V_{DDQ}/2$ of the transmitting device.
 9. V_{ISO} means $[V_{ICK}(CLK) + V_{ICK}(\overline{CLK})]/2$
 10. Refer to the figure below.



11. In the case of external termination, VTT(Termination Voltage) should be gone in the range of $V_{REF}(DC) \pm 0.04V$.

Pin Capacitance ($V_{DD} = 2.5V, V_{DDQ} = 1.8V, f = 1 MHz, T_a = 25^\circ C$)

| Symbol | Parameter | Min | Max | Delts | Units |
|-----------|--|-----|-----|-------|-------|
| C_{IN} | Input Pin Capacitance | 1.5 | 3.0 | 0.25 | pF |
| C_{INC} | Clock Pin (CLK, \overline{CLK}) Capacitance | 1.5 | 3.0 | 0.25 | pF |
| $C_{I/O}$ | DQ, DS, QS Capacitance | 2.5 | 3.5 | 0.5 | pF |
| C_{NC} | NC Pin Capacitance | - | 1.5 | - | pF |

Note : These parameters are periodically sampled and not 100% tested.

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DC Characteristics and Operating Conditions (VDD = 2.5V ± 0.125V, VDDQ = 1.8V ± 0.1V, Tcase = 0~85 °C)

| Parameter | Symbol | Max | | | Units | Notes |
|--|------------|-----|-----|-----|-------|-------|
| | | F6 | FB | F5 | | |
| Operating Current One bank Read or Write operation; $t_{CK} = \min$, $I_{RC} = \min$, $I_{OUT} = 0mA$; Burst Length = 4, CAS Latency = 6, Free running QS mode; $0V \leq V_{IN} \leq V_{IL(AC)} (\max.)$, $V_{IH(AC)}(\min.) \leq V_{IN} \leq V_{DDQ}$; Address inputs change up to 2 times during minimum I_{RC} , Read data change twice per clock cycle | I_{DD1S} | 320 | 300 | 280 | mA | 1, 2 |
| Standby Current All Banks : inactive state; $t_{CK} = \min$, $\overline{CS} = V_{IH}$, $\overline{PD} = V_{IH}$; $0V \leq V_{IN} \leq V_{IL(AC)}(\max.)$, $V_{IH(AC)}(\min.) \leq V_{IH} \leq V_{DDQ}$; Other input signals change one time during $4 \cdot t_{CK}$, DQ and DS inputs change twice per clock cycle | I_{DD2N} | 100 | 95 | 90 | | 1 |
| Standby (Power Down) Current All Banks : inactive state; $t_{CK} = \min$, $\overline{PD} = V_{IL}$ (Power Down); CAS Latency = 6, Free running QS mode; $0V \leq V_{IN} \leq V_{IL(AC)}(\max.)$, $V_{IH(AC)}(\min.) \leq V_{IN} \leq V_{DDQ}$; Other input signals change one time during $4 \cdot t_{CK}$, DQ and DS inputs are floating($V_{DDQ}/2$) | I_{DD2P} | 70 | 65 | 60 | | 1 |
| Write Operating Current(4 Banks) 4 Bank interleaved continuous burst write operation; $t_{CK} = \min$, $I_{RC} = \min$; Burst Length = 4, CAS Latency = 6, Free running QS mode; $0V \leq V_{IN} \leq V_{IL(AC)} (\max.)$, $V_{IH(AC)}(\min.) \leq V_{IN} \leq V_{DDQ}$; Address inputs change once per clock cycle, DQ and DS inputs change twice per clock cycle | I_{DD4W} | 650 | 600 | 550 | | 1 |
| Read Operating Current(4 Banks) 4 Bank interleaved continuous burst write operation; $t_{CK} = \min$, $I_{RC} = \min$, $I_{OUT} = 0mA$; Burst Length = 4, CAS Latency = 6, Free running QS mode; $0V \leq V_{IN} \leq V_{IL(AC)} (\max.)$, $V_{IH(AC)}(\min.) \leq V_{IN} \leq V_{DDQ}$; Address inputs change once per clock cycle, Read data change twice per clock cycle | I_{DD4R} | 650 | 600 | 550 | | 1,2 |
| Burst Auto-Refresh Current Refresh command at every I_{REFC} interval; $t_{CK} = \min$, $I_{REFC} = \min$; CAS Latency = 6, Free running QS mode; $0V \leq V_{IN} \leq V_{IL(AC)} (\max.)$, $V_{IH(AC)} (\min.) \leq V_{IN} \leq V_{DDQ}$; Address change up to 2 times during minimum I_{REFC} , DQ and DS inputs change twice per clock cycle | I_{DD5B} | 250 | 235 | 210 | | 1,3 |

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DC Characteristics and Operating Conditions (VDD = 2.5V ± 0.125V, VDDQ = 1.8V ± 0.1V, Tcase = 0~85 °C)

| Parameter | | Symbol | Min | Max | Unit | Notes | |
|---|---------------------------------------|------------------|---------|------|------|-------|---|
| Input Leakage Current (0V ≤ VIN ≤ VDDQ, All other pins not under test = 0V) | | ILI | -5 | 5 | µA | | |
| Output Leakage Current (Output disabled, 0V ≤ VOUT ≤ VDDQ) | | ILO | -5 | 5 | µA | | |
| VREF Current | | IREF | -5 | 5 | µA | | |
| Normal Output Driver | Output DC Current (VDDQ = 1.7 ~ 1.9V) | VOH = 1.420V | IOH(DC) | -5.6 | - | mA | 4 |
| | | VOL = 0.280V | IOL(DC) | 5.6 | - | | 4 |
| VOH = 1.420V | | IOH(DC) | -9.8 | - | 4 | | |
| VOL = 0.280V | | IOL(DC) | 9.8 | - | 4 | | |
| Weak Output Driver | | VOH = 1.420V | IOH(DC) | -2.8 | - | | 4 |
| | | VOL = 0.280V | IOL(DC) | 2.8 | - | | |
| Normal Output Driver | Output DC Current (VDDQ = 1.4 ~ 1.6V) | VOH = VDDQ - 0.4 | IOH(DC) | -4 | - | mA | 3 |
| | | VOL = 0.4V | IOL(DC) | -4 | - | | 3 |
| VOH = VDDQ - 0.4 | | IOH(DC) | -8 | - | 3 | | |
| VOL = 0.4V | | IOL(DC) | -8 | - | 3 | | |
| Weak Output Driver | | Not defined | IOH(DC) | - | - | | |
| | | Not defined | IOL(DC) | - | - | | |

- Notes :
1. These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK} , t_{RC} and I_{RC} .
 2. These parameters depend on the output loading. The specified values are obtained with the output open.
 3. I_{DD5B} is specified under burst refresh condition. Actual system should use distributed refresh that meet to t_{REFI} specification
 4. Refer to output driver characteristics for the detail. Output Driver Strength is selected by Extended Mode Register.

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AC Characteristics and Operating Conditions (Notes : 1, 2)

| Symbol | Parameter | | F6 | | FB | | F5 | | Units | Notes |
|---------------------|---|--------------------|---|------------------------------|---|------------------------------|---|------------------------------|-------|-------|
| | | | Min | Max | Min | Max | Min | Max | | |
| t _{RC} | Random Cycle Time | | 20.0 | - | 22.5 | - | 25 | - | ns | 3 |
| t _{CK} | Clock Cycle Time | C _L = 4 | 4.0 | 6.0 | 4.5 | 6.0 | 5.0 | 6.0 | | 3 |
| | | C _L = 5 | 3.33 | 6.0 | 3.75 | 6.0 | 4.5 | 6.0 | | 3 |
| | | C _L = 6 | 3.0 | 6.0 | 3.33 | 6.0 | 4.0 | 6.0 | | 3 |
| t _{RAC} | Random Access Time | | - | 20.0 | - | 22.5 | - | 25 | | 3 |
| t _{CH} | Clock High Time | | 0.45*t _{CK} | - | 0.45*t _{CK} | - | 0.45*t _{CK} | - | | 3 |
| t _{CL} | Clock Low Time | | 0.45*t _{CK} | - | 0.45*t _{CK} | - | 0.45*t _{CK} | - | | 3 |
| t _{CKQS} | QS Access Time from CLK | | -0.45 | 0.45 | -0.45 | 0.45 | -0.5 | 0.5 | | 3, 8 |
| t _{QSQ} | Data Output Skew from QS | | - | 0.2 | - | 0.25 | - | 0.3 | | 4 |
| t _{AC} | Data Access Time from CLK | | -0.5 | 0.5 | -0.5 | 0.5 | -0.6 | 0.6 | | 3, 8 |
| t _{OH} | Data Output Hold Time from CLK | | -0.5 | 0.5 | -0.5 | 0.5 | -0.6 | 0.6 | | 3, 8 |
| t _{HP} | CLK half period (minimum of Actual t _{CH} , t _{CL}) | | min(t _{CH} , t _{CL}) | - | min(t _{CH} , t _{CL}) | - | min(t _{CH} , t _{CL}) | - | | 3 |
| t _{QSP} | QS(Read) Pulse Width | | t _{HP} -t _{QHS} | - | t _{HP} -t _{QHS} | - | t _{HP} -t _{QHS} | - | | 4, 8 |
| t _{QSQV} | Data Output Valid Time from QS | | t _{HP} -t _{QHS} | - | t _{HP} -t _{QHS} | - | t _{HP} -t _{QHS} | - | | 4, 8 |
| t _{QHS} | DQ, QS Hold skew factor | | - | 0.055x t _{CK} +0.17 | - | 0.055x t _{CK} +0.17 | - | 0.055x t _{CK} +0.17 | | |
| t _{DQSS} | DS(Write) Low to High Setup Time | | 0.8*t _{CK} | 1.2*t _{CK} | 0.8*t _{CK} | 1.2*t _{CK} | 0.8*t _{CK} | 1.2*t _{CK} | 3 | |
| t _{DSPRE} | DS(Write) Preamble Pulse Width | | 0.4*t _{CK} | - | 0.4*t _{CK} | - | 0.4*t _{CK} | - | 4 | |
| t _{DSPRES} | DS First Input Setup Time | | 0 | - | 0 | - | 0 | - | 3 | |
| t _{DSPREH} | DS First Low Input Hold Time | | 0.3*t _{CK} | - | 0.3*t _{CK} | - | 0.3*t _{CK} | - | 3 | |
| t _{DSP} | DS High or Low Input Pulse Width | | 0.45*t _{CK} | 0.55*t _{CK} | 0.45*t _{CK} | 0.55*t _{CK} | 0.45*t _{CK} | 0.55*t _{CK} | 4 | |
| t _{DSS} | DS Input Falling Edge to Clock Setup Time | C _L = 4 | 0.75 | - | 0.8 | - | 1.0 | - | 3, 4 | |
| | | C _L = 5 | 0.75 | - | 0.8 | - | 1.0 | - | 3, 4 | |
| | | C _L = 6 | 0.75 | - | 0.8 | - | 1.0 | - | 3, 4 | |
| | | C _L = 7 | - | - | - | - | - | - | 3, 4 | |
| t _{DSPST} | DS(Write) Postamble Pulse Width | | 0.45*t _{CK} | - | 0.45*t _{CK} | - | 0.45*t _{CK} | - | 4 | |
| t _{DSPSTH} | DS(Write) Postamble Hold Time | C _L = 4 | 0.75 | - | 0.8 | - | 1.0 | - | 3, 4 | |
| | | C _L = 5 | 0.75 | - | 0.8 | - | 1.0 | - | 3, 4 | |
| | | C _L = 6 | 0.75 | - | 0.8 | - | 1.0 | - | 3, 4 | |
| | | C _L = 7 | - | - | - | - | - | - | 3, 4 | |
| t _{DS} | Data Input Setup Time from DS | | 0.3 | - | 0.35 | - | 0.4 | - | 4 | |
| t _{DH} | Data Input Hold Time from DS | | 0.3 | - | 0.35 | - | 0.4 | - | 4 | |
| t _{IS} | Command / Address Input Setup Time | | 0.6 | - | 0.6 | - | 0.7 | - | 3 | |
| t _{IH} | Command / Address Input Hold Time | | 0.6 | - | 0.6 | - | 0.7 | - | 3 | |

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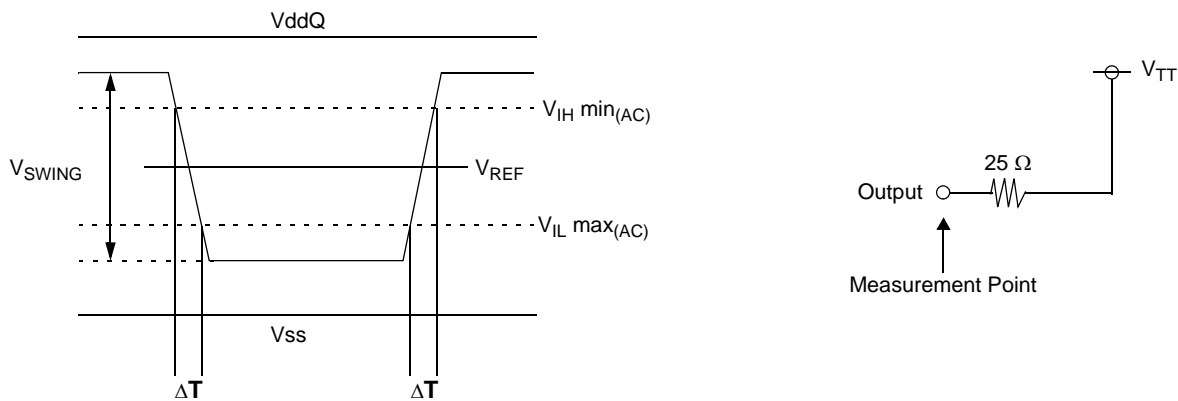
AC Characteristics and Operating Conditions (Notes : 1, 2) (Continued)

| Symbol | Parameter | F6 | | FB | | F5 | | Units | Notes | |
|--------------------|---|----------------------------|-----|----------------------------|-----|----------------------------|-----|-------|---------|--|
| | | Min | Max | Min | Max | Min | Max | | | |
| t _{LZ} | Data-out Low Impedance Time from CLK | -0.5 | - | -0.5 | - | -0.6 | - | | 3, 6, 8 | |
| t _{HZ} | Data-out High Impedance Time from CLK | - | 0.5 | - | 0.5 | - | 0.6 | | 3, 7, 8 | |
| t _{QPDH} | Last Output to $\overline{\text{PD}}$ High Hold Time | 0 | - | 0 | - | 0 | - | | | |
| t _{PDEX} | Power Down Exit Time | 0.6 | - | 0.6 | - | 0.7 | - | | 3 | |
| t _T | Input Transition Time | 0.1 | 1 | 0.1 | 1 | 0.1 | 1 | | | |
| t _{FPDL} | $\overline{\text{PD}}$ Low Input Window for Self-Refresh Entry | $-0.5 \cdot t_{\text{CK}}$ | 5 | $-0.5 \cdot t_{\text{CK}}$ | 5 | $-0.5 \cdot t_{\text{CK}}$ | 5 | | 3 | |
| t _{REFI} | Auto-Refresh Average Interval | 0.4 | 3.9 | 0.4 | 3.9 | 0.4 | 3.9 | us | 5 | |
| t _{PAUSE} | Pause Time after Power-up | 200 | - | 200 | - | 200 | - | | | |
| I _{RC} | Random Read/Write Cycle Time (Applicable to Same Bank) | C _L = 4 | 5 | - | 5 | - | 5 | - | Cycle | |
| | | C _L = 5 | 6 | - | 6 | - | 6 | - | | |
| | | C _L = 6 | 7 | - | 7 | - | 7 | - | | |
| | | C _L = 7 | - | - | - | - | - | - | | |
| I _{RCD} | RDA/WRA to LAL Command Input Delay (Applicable to Same Bank) | 1 | 1 | 1 | 1 | 1 | 1 | | | |
| I _{RAS} | LAL to RDA/WRA Command Input Delay (Applicable to Same Bank) | C _L = 4 | 4 | - | 4 | - | 4 | - | | |
| | | C _L = 5 | 5 | - | 5 | - | 5 | - | | |
| | | C _L = 6 | 6 | - | 6 | - | 6 | - | | |
| | | C _L = 7 | - | - | - | - | - | - | | |
| I _{RBD} | Random Bank Access Delay (Applicable to Other Bank) | 2 | - | 2 | - | 2 | - | | | |
| I _{RWD} | LAL following RDA to WRA Delay (Applicable to Other Bank) | BL = 4 | 3 | - | 3 | - | 3 | - | | |
| I _{WRD} | LAL following WRA to RDA Delay (Applicable to Other Bank) | | 1 | - | 1 | - | 1 | - | | |
| I _{RSC} | Mode Register Set Cycle Time | C _L = 4 | 7 | - | 7 | - | 7 | - | | |
| | | C _L = 5 | 7 | - | 7 | - | 7 | - | | |
| | | C _L = 6 | 7 | - | 7 | - | 7 | - | | |
| | | C _L = 7 | | | | | | | | |
| I _{PD} | $\overline{\text{PD}}$ Low to Inactive State of Input Buffer | - | 2 | - | 2 | - | 2 | | | |
| I _{PDA} | $\overline{\text{PD}}$ High to Active State of Input Buffer | 1 | - | 1 | - | 1 | - | | | |
| I _{PDV} | Power down mode valid from REF command | C _L = 4 | 19 | - | 19 | - | 19 | - | | |
| | | C _L = 5 | 23 | - | 23 | - | 23 | - | | |
| | | C _L = 6 | 25 | - | 25 | - | 25 | - | | |
| | | C _L = 7 | | | | | | | | |
| I _{REFC} | Auto-Refresh Cycle Time | C _L = 4 | 19 | - | 19 | - | 19 | - | | |
| | | C _L = 5 | 23 | - | 23 | - | 23 | - | | |
| | | C _L = 6 | 25 | - | 25 | - | 25 | - | | |
| | | C _L = 7 | | | | | | | | |
| I _{LOCK} | DLL Lock-on Time (Applicable to RDA command) | 200 | - | 200 | - | 200 | - | | | |

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AC Test Conditions

| Symbol | Parameter | Value | Units | Notes |
|---------------|---|-----------------|-------|-------|
| $V_{IH(min)}$ | Input high voltage (minimum) | $V_{REF} + 0.2$ | V | |
| $V_{IL(max)}$ | Input low voltage (maximum) | $V_{REF} - 0.2$ | V | |
| V_{REF} | Input reference voltage | $V_{DDQ}/2$ | V | |
| V_{TT} | Termination voltage | V_{REF} | V | |
| V_{SWING} | Input signal peak to peak swing | 0.7 | V | |
| V_R | Differential clock input reference level | $V_{X(AC)}$ | V | |
| $V_{ID(AC)}$ | Input differential voltage | 1.0 | V | |
| SLEW | Input signal minimum slew rate | 2.5 | V/ns | |
| V_{OTR} | Output timing measurement reference voltage | $V_{DDQ}/2$ | V | 9 |



$$\text{Slew} = (V_{IH\ min(AC)} - V_{IL\ max(AC)}) / \Delta T$$

AC Test Load

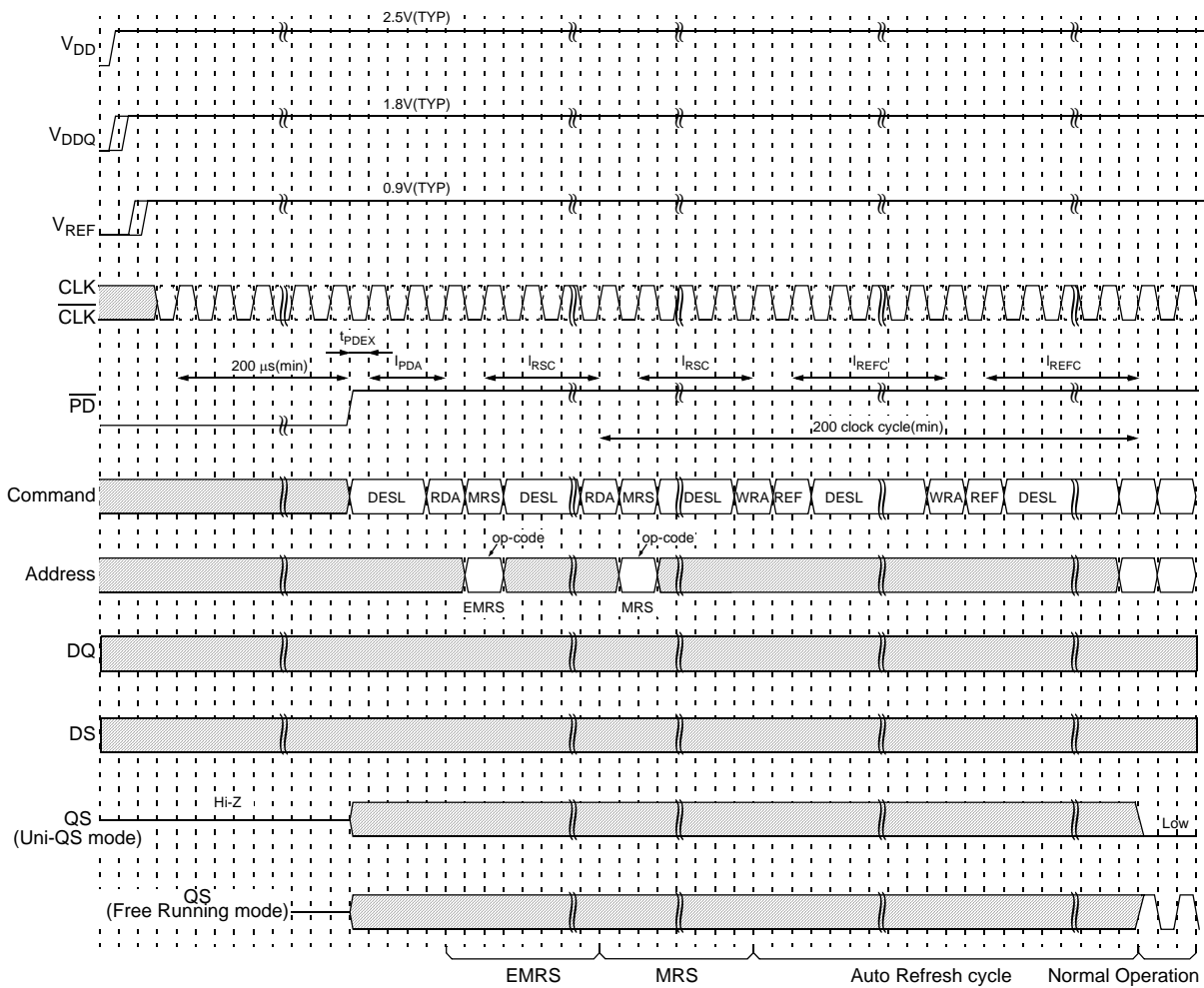
- Notes :**
- Transition times are measured between $V_{IH\ min(DC)}$ and $V_{IL\ max(DC)}$.
Transition (rise and fall) of input signals have a fixed slope.
 - If the result of nominal calculation with regard to t_{CK} contains more than one decimal place, the result is rounded up to the nearest decimal place.
(i.e., $t_{DQSS} = 0.8 * t_{CK}$, $t_{CK} = 3.3\text{ns}$, $0.8 * 3.3\text{ ns} = 2.64\text{ ns}$ is rounded up to 2.7 ns.)
 - These parameters are measured from the differential clock (CLK and $\overline{\text{CLK}}$) AC cross point.
 - These parameters are measured from signal transition point of DS crossing V_{REF} level.
 - The $t_{REFI}\ (MAX.)$ applies to equally distributed refresh method.
The $t_{REFI}\ (MIN.)$ applies to both burst refresh method and distributed refresh method.
In such case, the average interval of eight consecutive Auto-Refresh commands has to be more than 400ns always. In other words, the number of Auto-Refresh cycles which can be performed within 3.2 μs (8X400ns) is to 8 times in the maximum.
 - Low Impedance State is specified at $V_{DDQ}/2 \pm 0.2\text{V}$ from steady state.
 - High Impedance State is specified where output buffer is no longer driven.
 - These parameters depend on the clock jitter. These parameters are measured at stable clock.
 - Output timing is measured by using Normal driver strength at $V_{DDQ} = 1.7\text{V} \sim 1.9\text{V}$.
Output timing is measured by using Strong driver strength at $V_{DDQ} = 1.4\text{V} \sim 1.6\text{V}$

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Power Up Sequence

1. As for \overline{PD} , being maintained by the low state ($\leq 0.2V$) is desirable before a power-supply injection.
2. Apply V_{DD} before or at the same time as V_{DDQ} .
3. Apply V_{DDQ} before or at the same time as V_{REF} .
4. Start clock (CLK, \overline{CLK}) and maintain stable condition for 200us (min.).
5. After stable power and clock, apply DESL and take $\overline{PD} = H$.
6. Issue EMRS to enable DLL and to define driver strength and data strobe type. (Note : 1)
7. Issue MRS for set \overline{CAS} Latency (CL), Burst Type (BT), and Burst Length (BL). (Note : 1)
8. Issue two or more Auto-Refresh commands. (Note:1)
9. Ready for normal operation after 200 clocks from Extended Mode Register programming.

Note : 1. Sequence 6, 7 and 8 can be issued in random order.
 2. L=Logic Low, H = Logic High

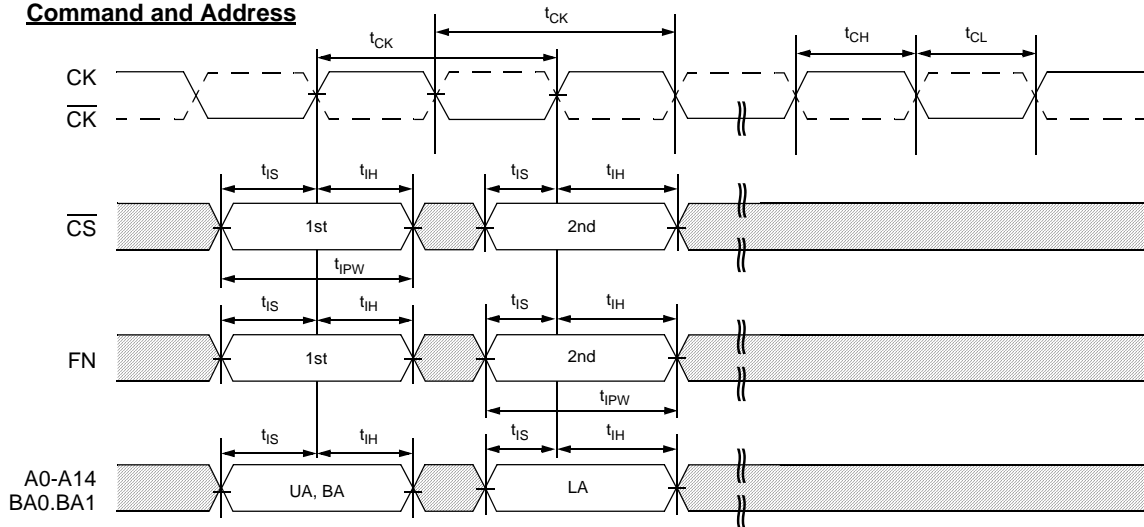


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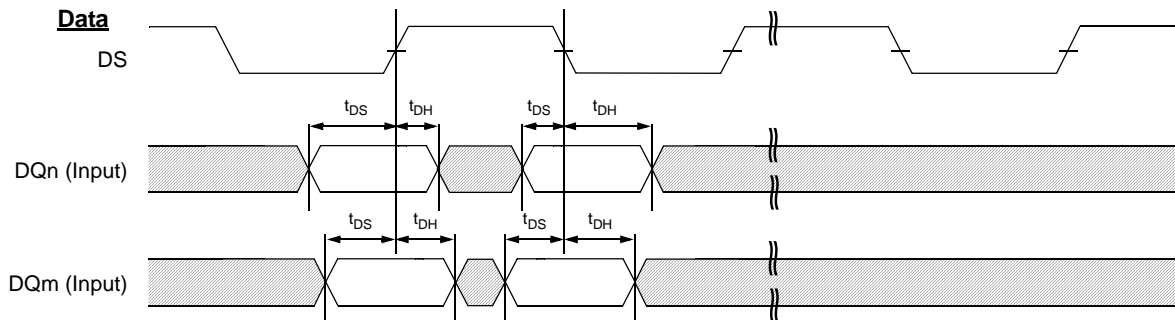
Basic Timing Diagrams

Input Timing

Command and Address

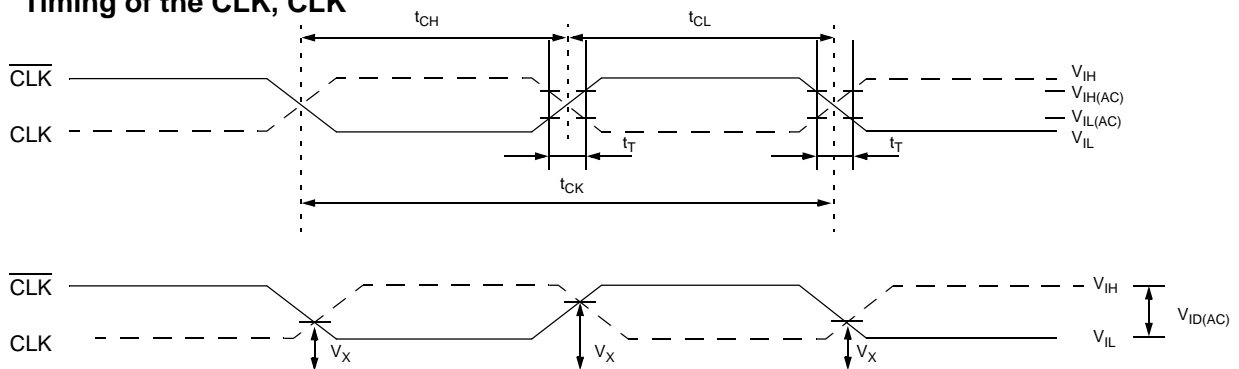


Data



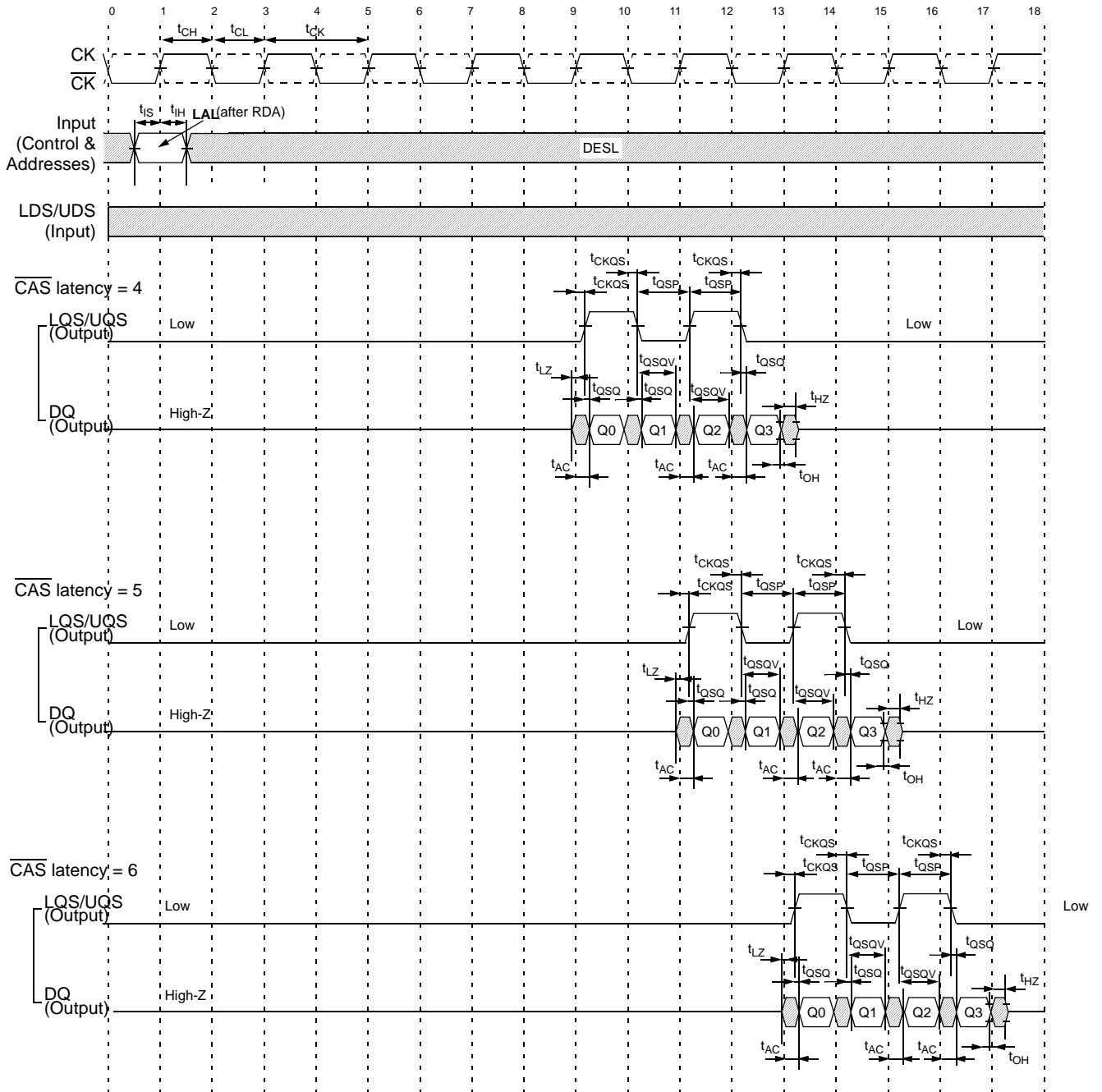
Refer to the Command Truth Table.

Timing of the CLK, \overline{CLK}



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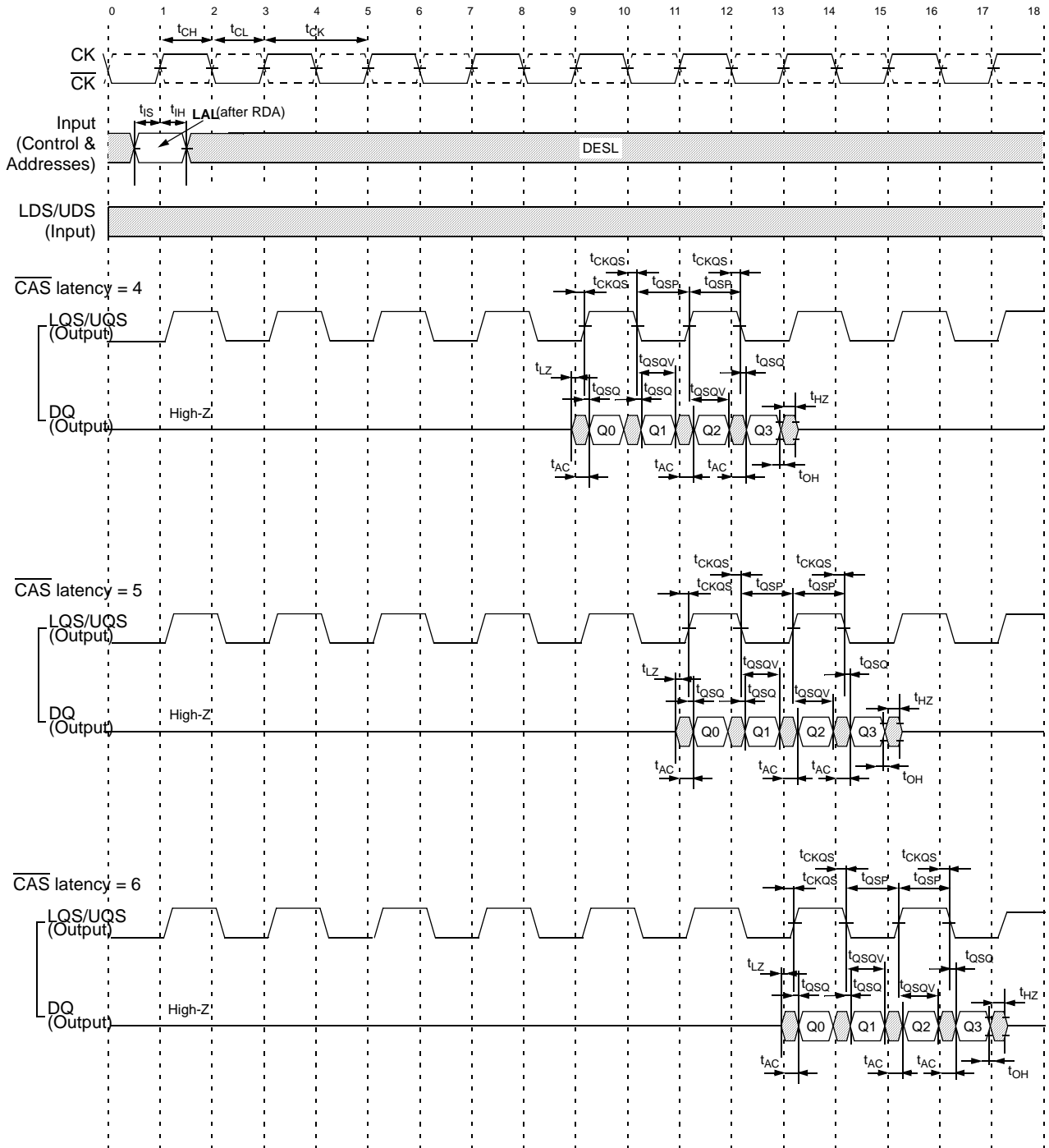
Read Timing (Burst Length = 4) Unidirectional DS/QS mode



Note : DQ0 to DQ17 are aligned with LQS.
DQ18 to DQ35 are aligned with UQS.

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Read Timing (Burst Length = 4) Unidirectional DS/Free Running QS mode

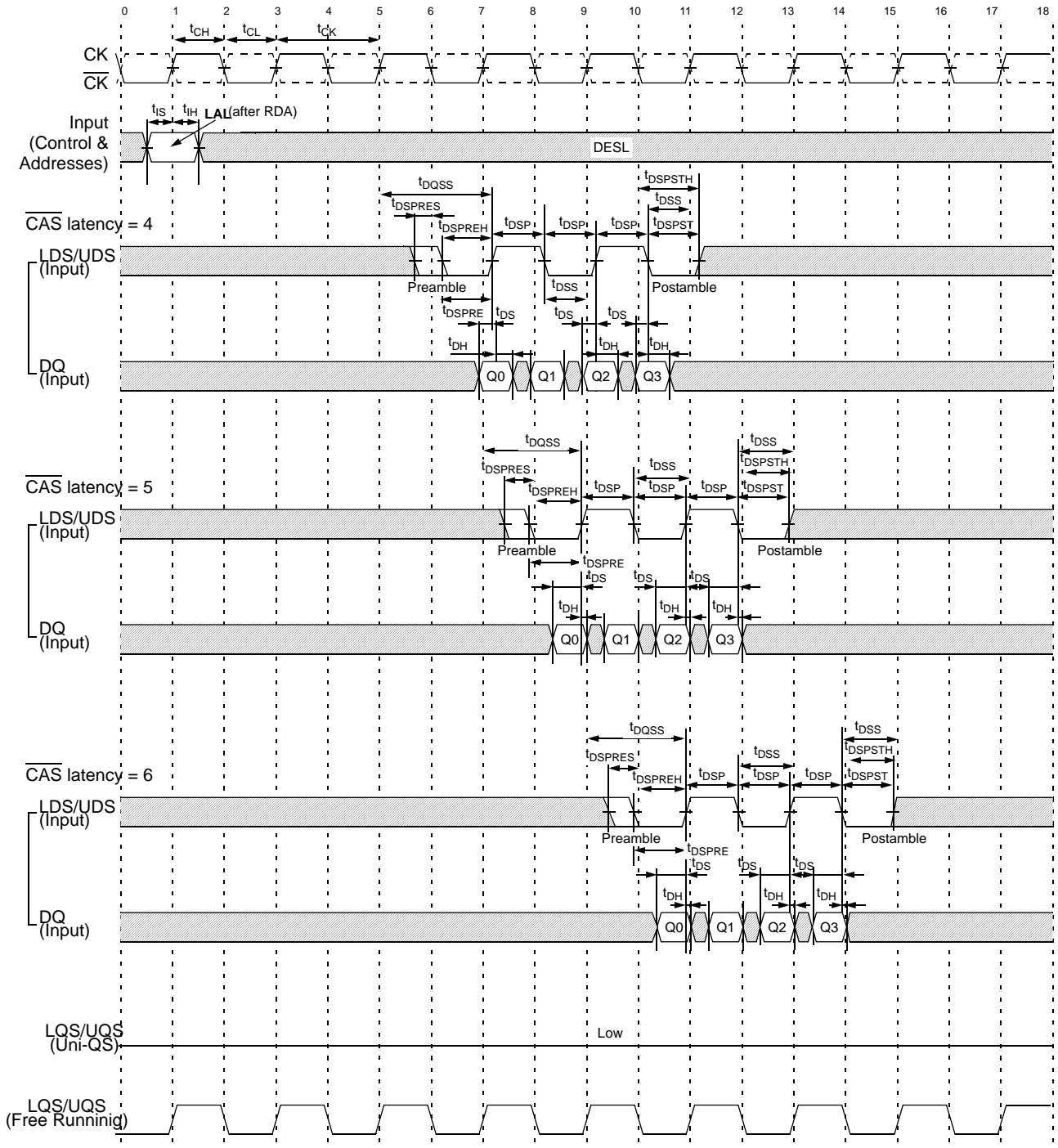


Note : DQ0 to DQ17 are aligned with LQS.
DQ18 to DQ35 are aligned with UQS.
LQS/UQS is always asserted in Free Running QS mode.

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Write Timing (Burst Length = 4)

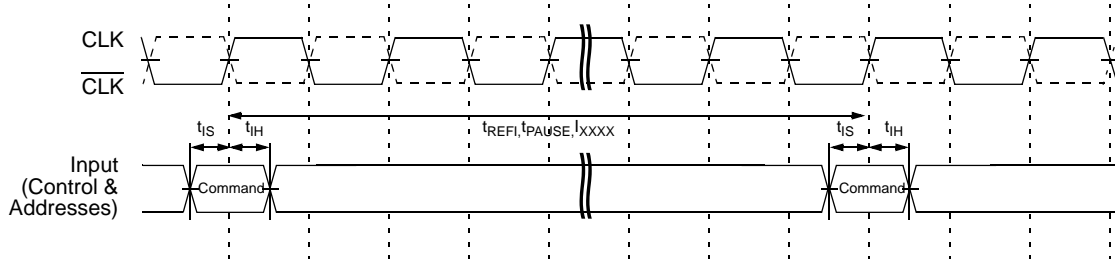
Unidirectional DS/QS mode, Unidirectional DS/Free Running QS mode



Note : DQ0 to DQ17 are sampled at both edges of LDS.
DQ18 to DQ35 are sampled at both edges of UDS.

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t_{REFI} , t_{PAUSE} , t_{XXXX} Timing



Note. "XXXX" means "t_{RC}", "t_{RCD}", "t_{RAS}", etc.

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Function Truth Table (Notes : 1,2,3)

Command Truth Table (Notes : 4)

•The First Command

| Symbol | Function | \overline{CS} | FN | BA1-BA0 | A14-A9 | A8 | A7 | A6-A0 |
|--------|-----------------------|-----------------|----|---------|--------|----|----|-------|
| DESL | Device Deselect | H | X | X | X | X | X | X |
| RDA | Read with Auto-close | L | H | BA | UA | UA | UA | UA |
| WRA | Write with Auto-close | L | L | BA | UA | UA | UA | UA |

•The Second Command (The next clock of RDA or WRA command)

| Symbol | Function | \overline{CS} | FN | BA1-BA0 | A14-A13 | A12-A11 | A10-A9 | A8 | A7 | A6-A0 |
|--------|---------------------|-----------------|----|---------|---------|---------|--------|----|----|-------|
| LAL | Lower Address Latch | H | X | X | V | X | X | X | X | LA |
| REF | Auto-Refresh | L | X | X | X | X | X | X | X | X |
| MRS | Mode Register Set | L | X | V | L | L | L | L | V | V |

Notes : 1. L = Logic Low, H = Logic High, X = either L or H, V = Valid (Specified Value), BA = Bank Address, UA = Upper Address, LA = Lower Address.

2. All commands are assumed to issue at a valid state.

3. All inputs for command (excluding SELFX and PDEX) are latched on the crossing point of differential clock input where CLK goes to High.

4. Operation mode is decided by the combination of 1st command and 2nd command refer to "STATE DIAGRAM" and the command table below.

Read Command Table

| Command (Symbol) | \overline{CS} | FN | BA1-BA0 | A14-A9 | A8 | A7 | A6-A0 | Notes |
|------------------|-----------------|----|---------|--------|----|----|-------|-------|
| RDA (1st) | L | H | BA | UA | UA | UA | UA | |
| LAL (2nd) | H | X | X | X | X | X | LA | |

Write Command Table

| Command (Symbol) | \overline{CS} | FN | BA1-BA0 | A14 | A13 | A12 | A11 | A10~A9 | A8 | A7 | A6-A0 |
|------------------|-----------------|----|---------|-----|-----|-----|-----|--------|----|----|-------|
| WRA (1st) | L | L | BA | UA | UA | UA | UA | UA | UA | UA | UA |
| LAL (2nd) | H | X | X | VW0 | VW1 | X | X | X | X | X | LA |

Notes : 5. A14~A13 are used for Variable Write Length (VW) control at Write Operation.

VW Truth Table

| | Function | VW0 | VW1 |
|--------|-----------------------|-----|-----|
| BL = 4 | Reserved | L | L |
| | Write All Words | H | L |
| | Write First Two Words | L | H |
| | Write First One Word | H | H |

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Function Truth Table (Continued)

Mode Register Set Command Truth Table

| Command (Symbol) | \overline{CS} | FN | BA1-BA0 | A14-A9 | A8 | A7 | A6-A0 | Notes |
|------------------|-----------------|----|---------|--------|----|----|-------|-------|
| RDA (1st) | L | H | X | X | X | X | X | |
| MRS (2nd) | L | X | V | L | L | V | V | 6 |

Note : 6. Refer to "Mode Register Table".

Auto-Refresh Command Table

| Function | Command (Symbol) | Current State | \overline{PD} | | \overline{CS} | FN | BA1-BA0 | A14-A9 | A8 | A7 | A6-A0 | Notes |
|--------------|------------------|---------------|-----------------|---|-----------------|----|---------|--------|----|----|-------|-------|
| | | | n-1 | n | | | | | | | | |
| Active | WRA(1st) | Standby | H | H | L | L | X | X | X | X | X | |
| Auto-Refresh | REF(2nd) | Active | H | H | L | X | X | X | X | X | X | |

Power Down Table

| Function | Command (Symbol) | Current State | \overline{PD} | | \overline{CS} | FN | BA1-BA0 | A14-A9 | A8 | A7 | A6-A0 | Notes |
|---------------------|------------------|---------------|-----------------|---|-----------------|----|---------|--------|----|----|-------|-------|
| | | | n-1 | n | | | | | | | | |
| Power Down Entry | PDEN | Standby | H | L | H | X | X | X | X | X | X | 8 |
| Power Down Continue | - | Power Down | L | L | X | X | X | X | X | X | X | |
| Power Down Exit | PDEX | Power Down | L | H | H | X | X | X | X | X | X | 9 |

Notes : 7. \overline{PD} has to be brought to Low within t_{FPDL} from REF command.

8. \overline{PD} should be brought to Low after DQ's state turned high impedance.

9. When \overline{PD} is brought to High from Low, this function is executed asynchronously.

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Function Truth Table (Continued)

| Current State | PD | | \overline{CS} | FN | Address | Command | Action | Notes |
|-------------------------|-----|---|-----------------|----|---------|------------|---|-------|
| | n-1 | n | | | | | | |
| Idle | H | H | H | X | X | DESL | NOP | |
| | H | H | L | H | BA, UA | RDA | Row activate for Read | |
| | H | H | L | L | BA, UA | WRA | Row activate for Write | |
| | H | L | H | X | X | PDEN | Power Down Entry | 10 |
| | H | L | L | X | X | - | Illegal | |
| | L | X | X | X | X | - | Refer to Power Down state | |
| Row Active for Read | H | H | H | X | LA | LAL | Begin read | |
| | H | H | L | X | Op-Code | MRS/EMRS | Access to Mode Register | |
| | H | L | H | X | X | PDEN | Illegal | |
| | H | L | L | X | X | MRS/EMRS | Illegal | |
| | L | X | X | X | X | - | Invalid | |
| Row Active for Write | H | H | H | X | LA | LAL | Begin Write | |
| | H | H | L | X | X | REF | Auto-Refresh | |
| | H | L | H | X | X | PDEN | Illegal | |
| | H | L | L | X | X | REF (Self) | Self-Refresh entry | |
| | L | X | X | X | X | - | Invalid | |
| Read | H | H | H | X | X | DESL | Continue burst read to end | |
| | H | H | L | H | BA, UA | RDA | Illegal | 11 |
| | H | H | L | L | BA, UA | WRA | Illegal | 11 |
| | H | L | H | X | X | PDEN | Illegal | |
| | H | L | L | X | X | - | Illegal | |
| | L | X | X | X | X | - | Invalid | |
| Write | H | H | H | X | X | DESL | Data write & continue burst write to end | |
| | H | H | L | H | BA, UA | RDA | Illegal | 11 |
| | H | H | L | L | BA, UA | WRA | Illegal | 11 |
| | H | L | H | X | X | PDEN | Illegal | |
| | H | L | L | X | X | - | Illegal | |
| | L | X | X | X | X | - | Invalid | |
| Auto-Refreshing | H | H | H | X | X | DESL | NOP-> Idle after t_{REFC} | |
| | H | H | L | H | BA, UA | RDA | Illegal | |
| | H | H | L | L | BA, UA | WRA | Illegal | |
| | H | L | H | X | X | PDEN | Self-Refresh entry | 12 |
| | H | L | L | X | X | - | Illegal | |
| | L | X | X | X | X | - | Refer to Self-Refreshing state | |
| Mode Register Accessing | H | H | H | X | X | DESL | Nop-> Idle after t_{RSC} | |
| | H | H | L | H | BA, UA | RDA | Illegal | |
| | H | H | L | L | BA, UA | WRA | Illegal | |
| | H | L | H | X | X | PDEN | Illegal | |
| | H | L | L | X | X | - | Illegal | |
| | L | X | X | X | X | - | Invalid | |
| Power Down | H | X | X | X | X | - | Invalid | |
| | L | L | X | X | X | - | Maintain Power Down Mode | |
| | L | H | H | X | X | RDEX | Exit Power Down Mode->Idle after t_{PDEX} | |
| | L | H | L | X | X | - | Illegal | |

Notes : 10. Illegal if any bank is not idle.

11. Illegal to bank in specified states : Function may be Legal in the bank indicated by bank Address (BA).

12. Illegal if t_{FPDL} is not Satisfied.

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Mode Register Table

Regular Mode Register (Notes : 1)

| Address | BA1 ^{*1} | BA0 ^{*1} | A14-A8 | A7 ^{*3} | A6-A4 | A3 | A2-A0 |
|----------|-------------------|-------------------|--------|------------------|-------|----|-------|
| Register | 0 | 0 | 0 | TM | CL | BT | BL |

| A7 | Test Mode (TE) |
|----|-------------------|
| 0 | Regular (Default) |
| 1 | Test Mode Entry |

| A3 | Burst Type (BT) |
|----|-----------------|
| 0 | Sequential |
| 1 | Interleave |

| A6 | A5 | A4 | CAS Latency (CL) |
|----|----|----|------------------------|
| 0 | 0 | X | Reserved ^{*2} |
| 0 | 1 | 0 | Reserved ^{*2} |
| 0 | 1 | 1 | Reserved ^{*2} |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | Reserved ^{*2} |

| A2 | A1 | A0 | Burst Length (BL) |
|----|----|----|------------------------|
| 0 | 0 | 0 | Reserved ^{*2} |
| 0 | 0 | 1 | Reserved ^{*2} |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | Reserved ^{*2} |
| 1 | X | X | |

Extended Mode Register (Notes : 4)

| Address | BA1 ^{*4} | BA0 ^{*4} | A14-A7 | A6~A5 | A4-A3 | A2~A1 | A0 ^{*5} |
|----------|-------------------|-------------------|--------|-------|---------|---------|------------------|
| Register | 0 | 1 | 0 | SS | DIC(QS) | DIC(DQ) | DS |

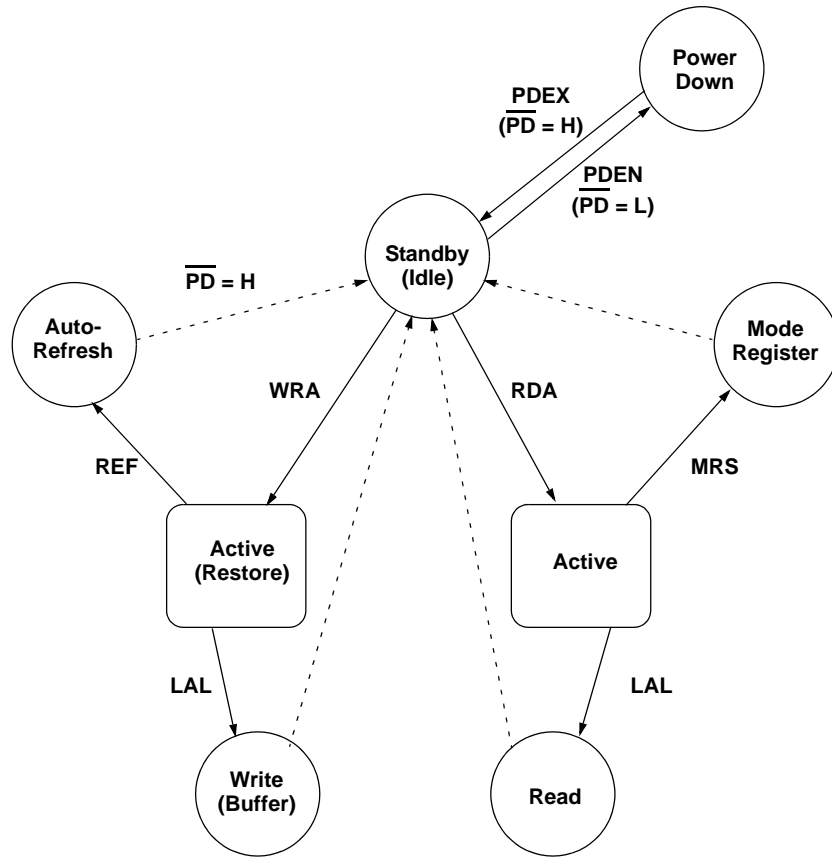
| A6 | A5 | Strobe Select | QS | | DQ | | Output Driver Impedance Control (DIC) |
|----|----|-----------------------------------|----|----|----|----|---------------------------------------|
| | | | A4 | A3 | A2 | A1 | |
| 0 | 0 | Reserved ^{*2} | 0 | 0 | 0 | 0 | Normal Output Driver |
| 0 | 1 | Reserved ^{*2} | 0 | 1 | 0 | 1 | Strong Output Driver |
| 1 | 0 | Unidirectional DS/QS | 1 | 0 | 1 | 0 | Weak Output Driver |
| 1 | 1 | Unidirectional DS/Free Running QS | 1 | 1 | 1 | 1 | Reserved |

- Note :**
1. Regular Mode Register Is Chosen Using the combination of BA0 = 0 and BA1 = 0.
 2. "Reserved" places in Regular Mode Register should not be set.
 3. A7 in Regular Mode Register must be set to "0"(Low state).
Because Test Mode is specific mode for supplier.
 4. Extended Mode Register is chosen using the Combination of BA0 = 1 and BA1 = 0.
 5. A0 in Extended Mode Register must be set to "0" to enable DLL for normal operation.

| A0 | DLL Switch (DS) |
|----|-----------------|
| 0 | DLL Enable |
| 1 | DLL Disable |

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State Diagram



—————> Command Input

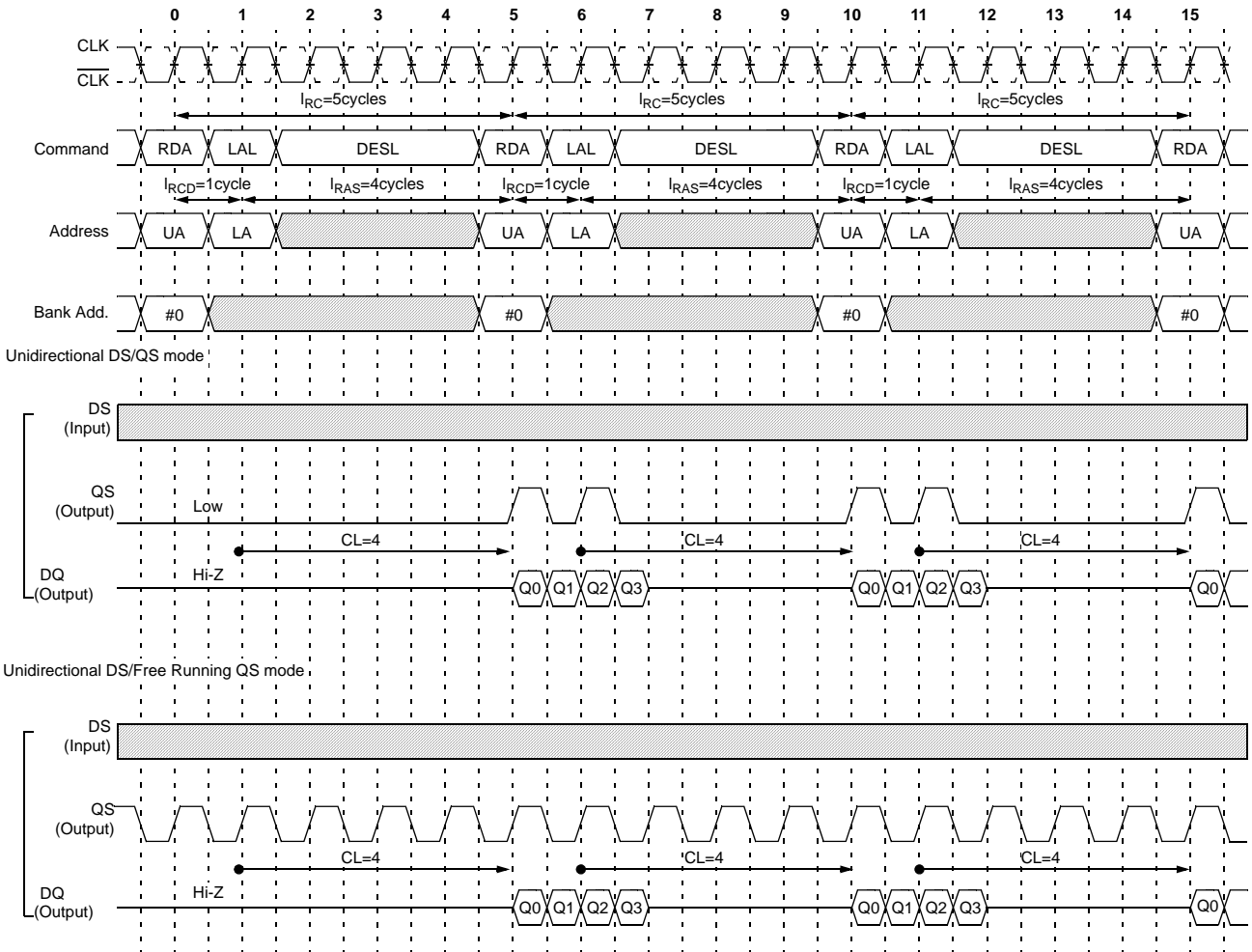
- - - - -> Automatic Return

The second command at Active state must be issued 1clock after RDA or WRA command input

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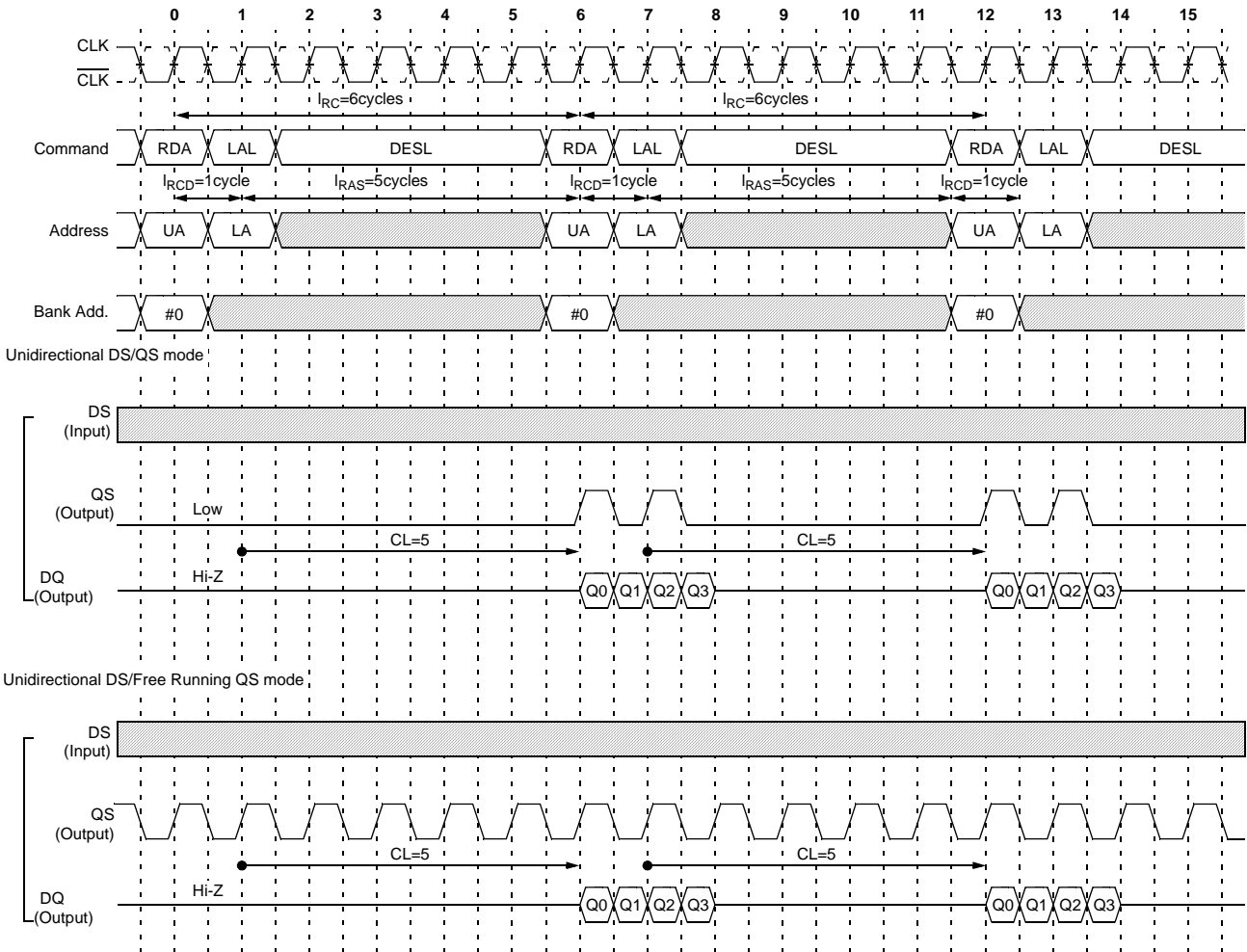
Timing Diagrams

Single Bank Read Timing (CL=4)



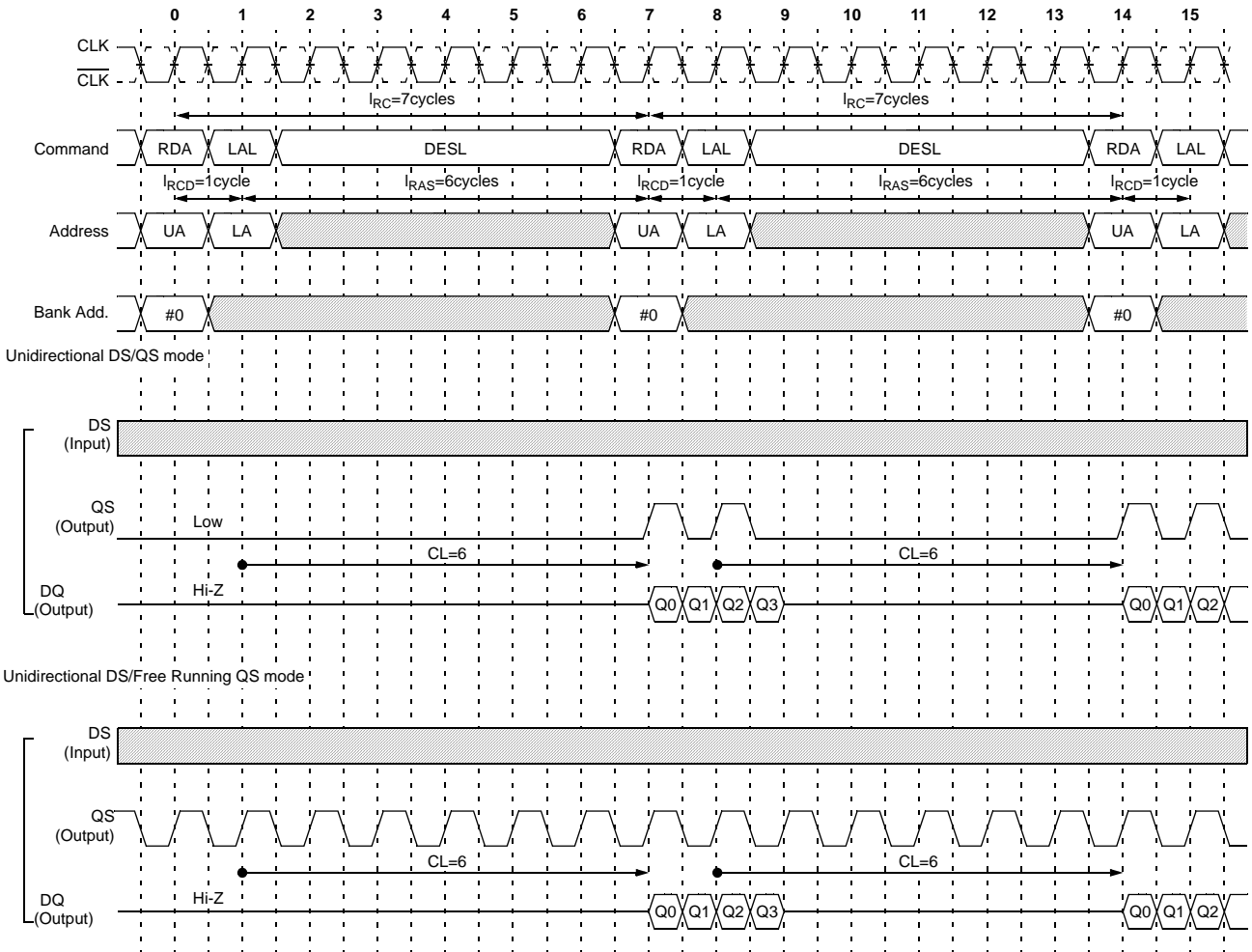
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Single Bank Read Timing (CL=5)



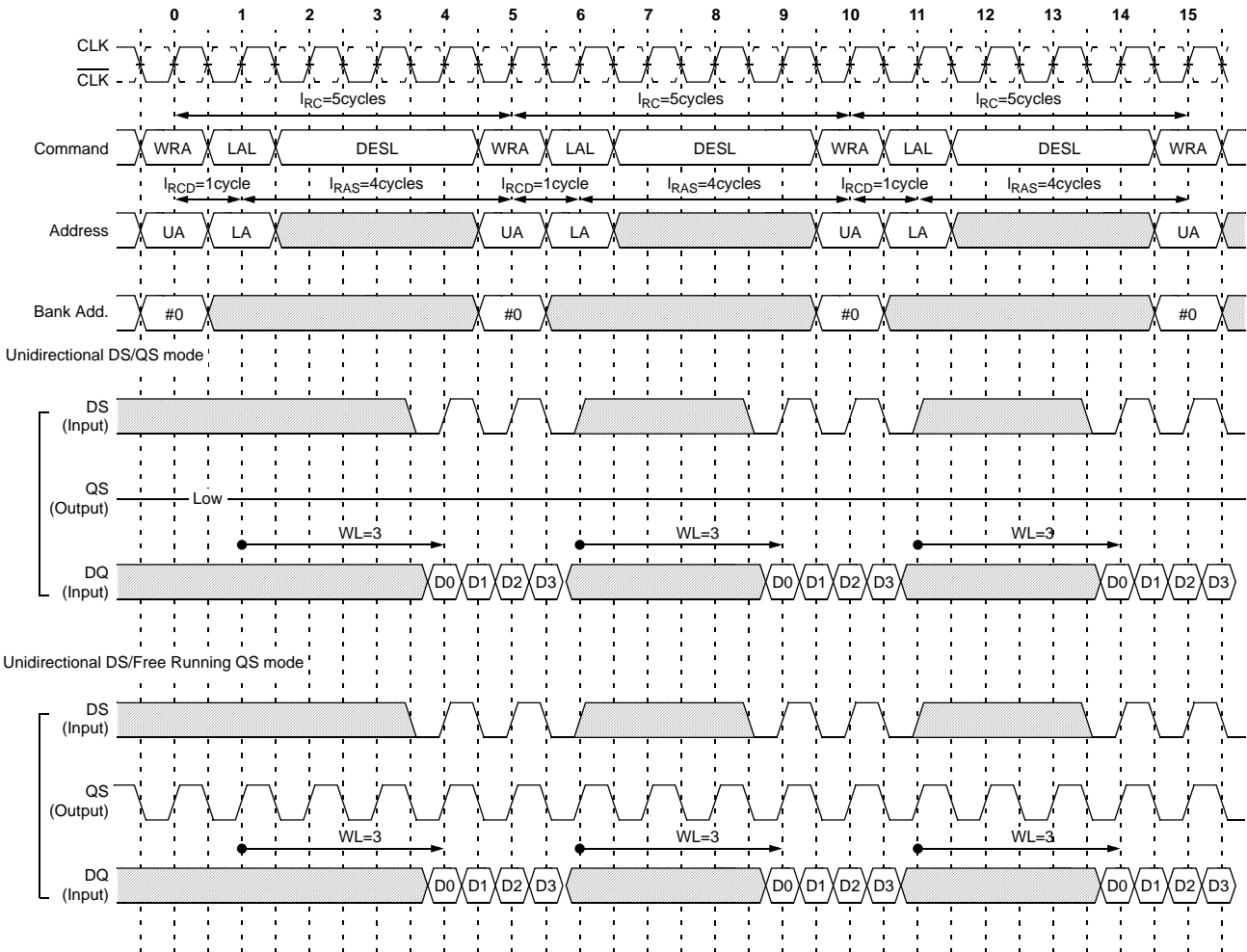
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Single Bank Read Timing (CL=6)



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Single Bank Write Timing (CL=4)



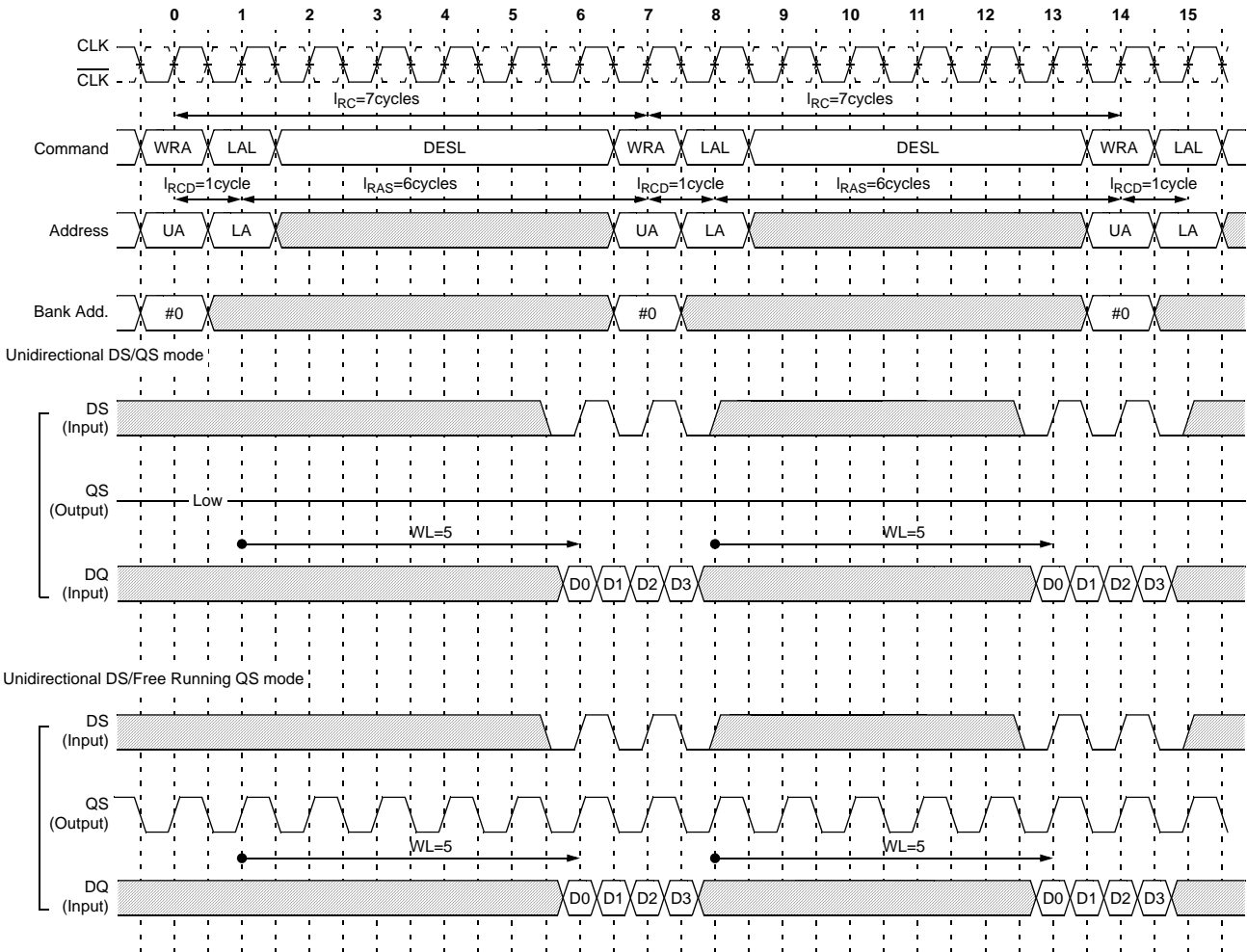
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Single Bank Write Timing (CL=5)



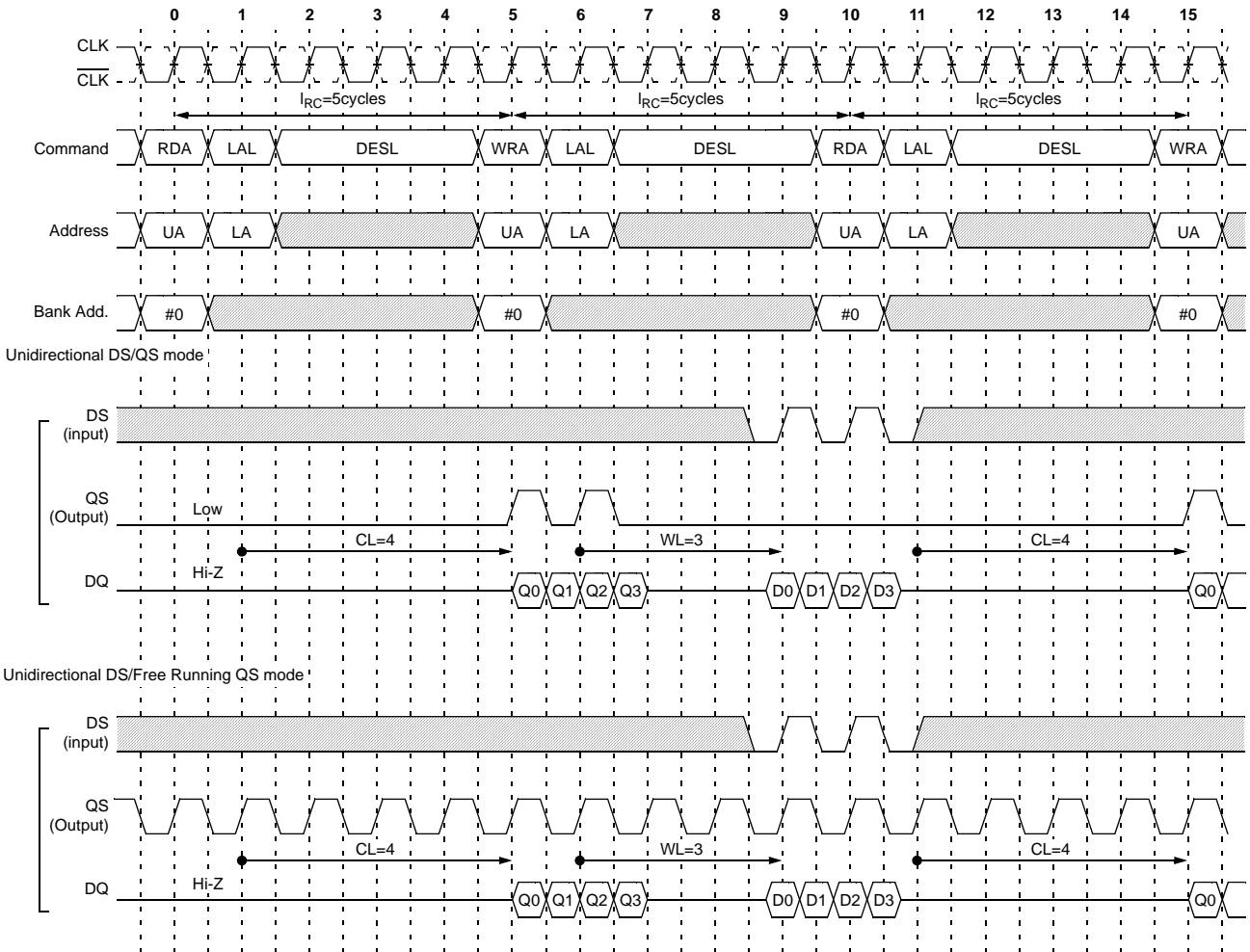
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Single Bank Write Timing (CL=6)



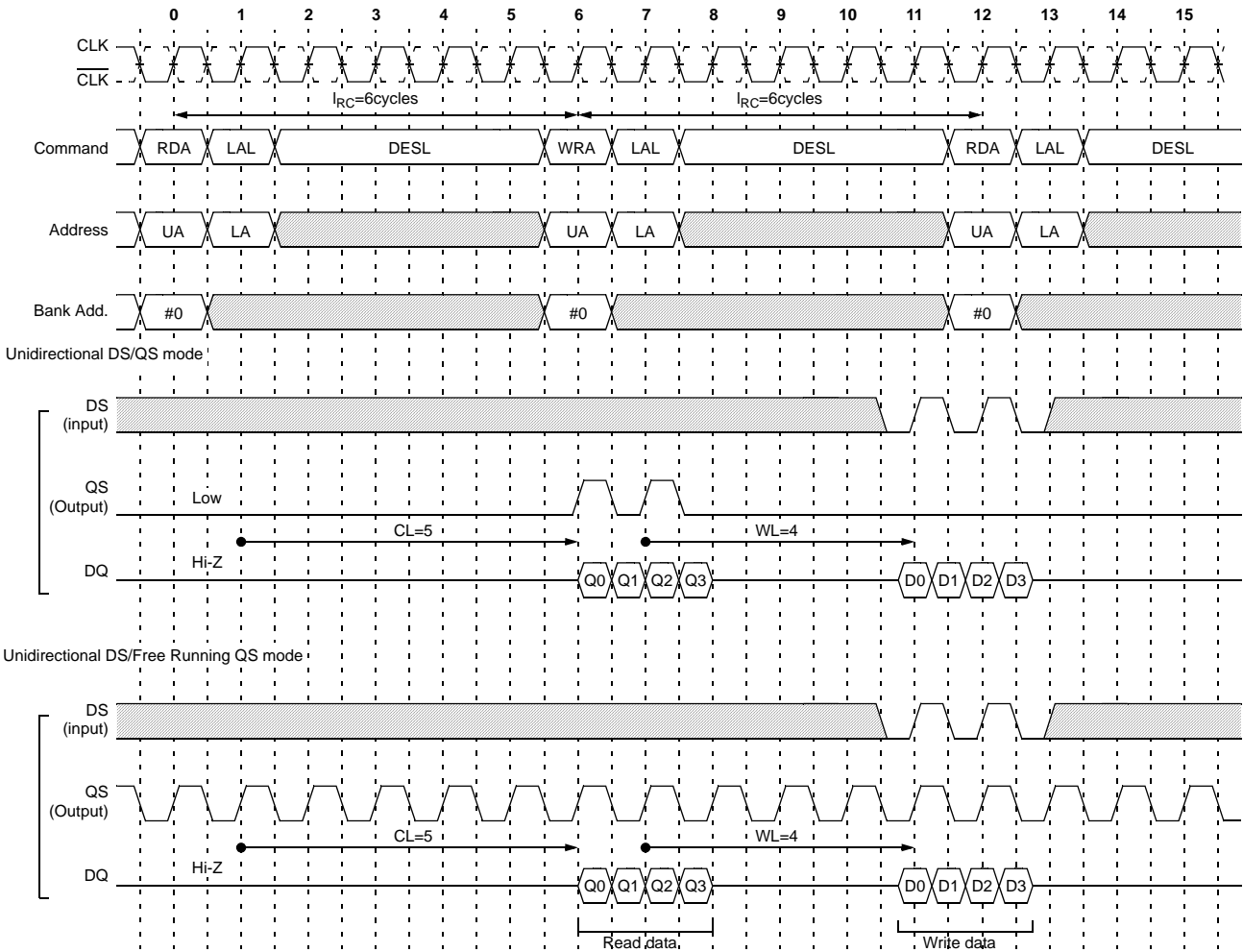
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Single Bank Read-Write Timing (CL=4)



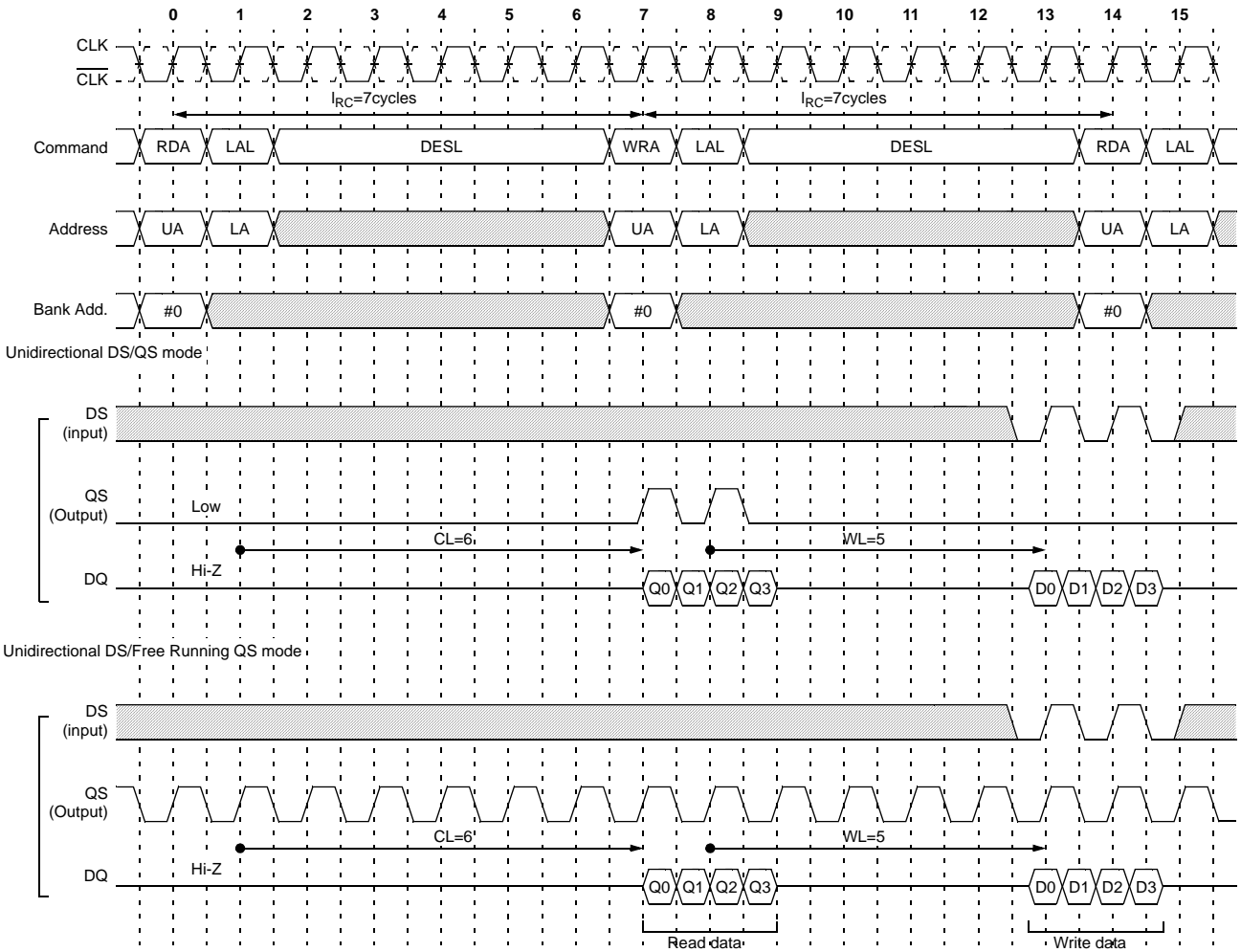
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Single Bank Read-Write Timing (CL=5)



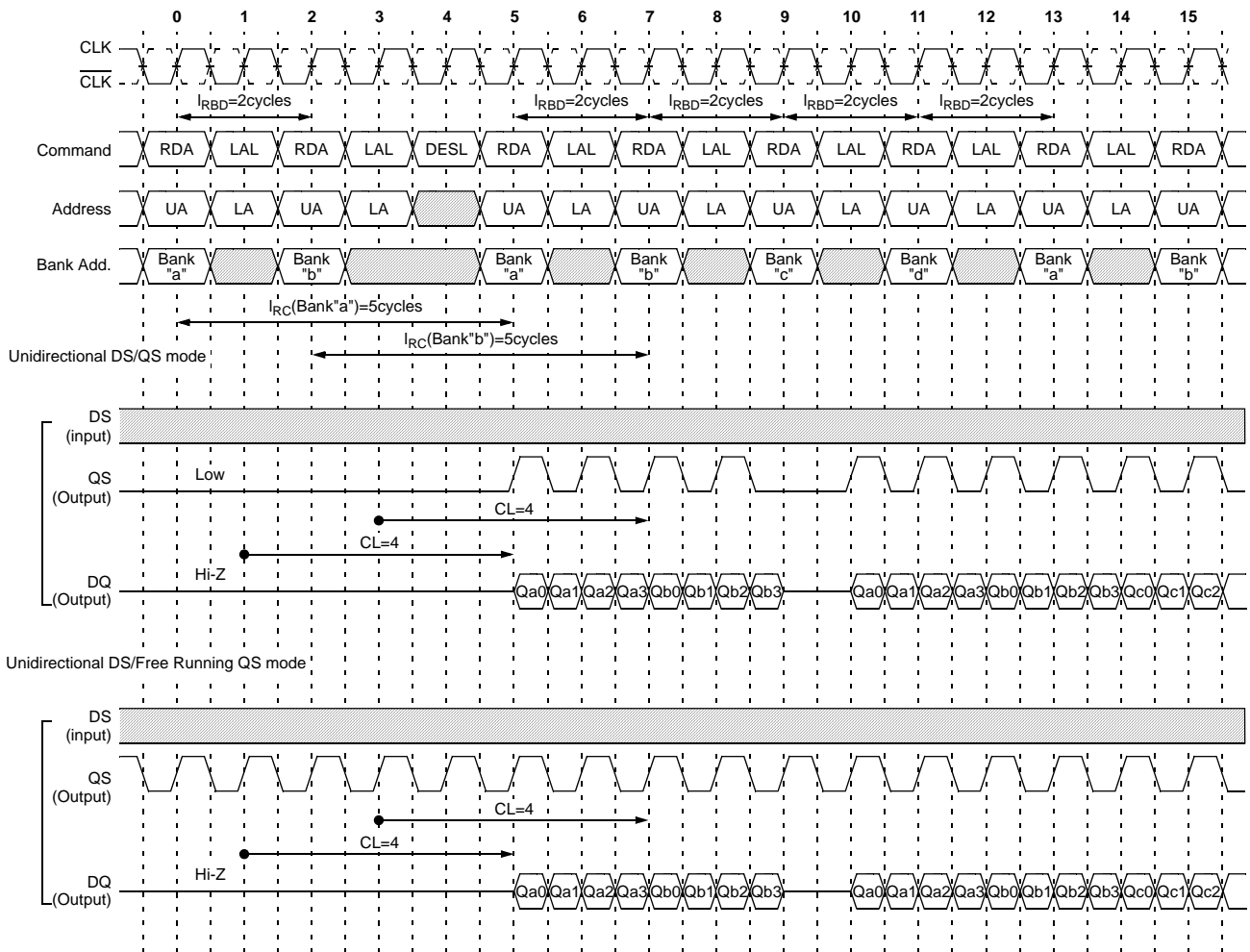
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Single Bank Read-Write Timing (CL=6)



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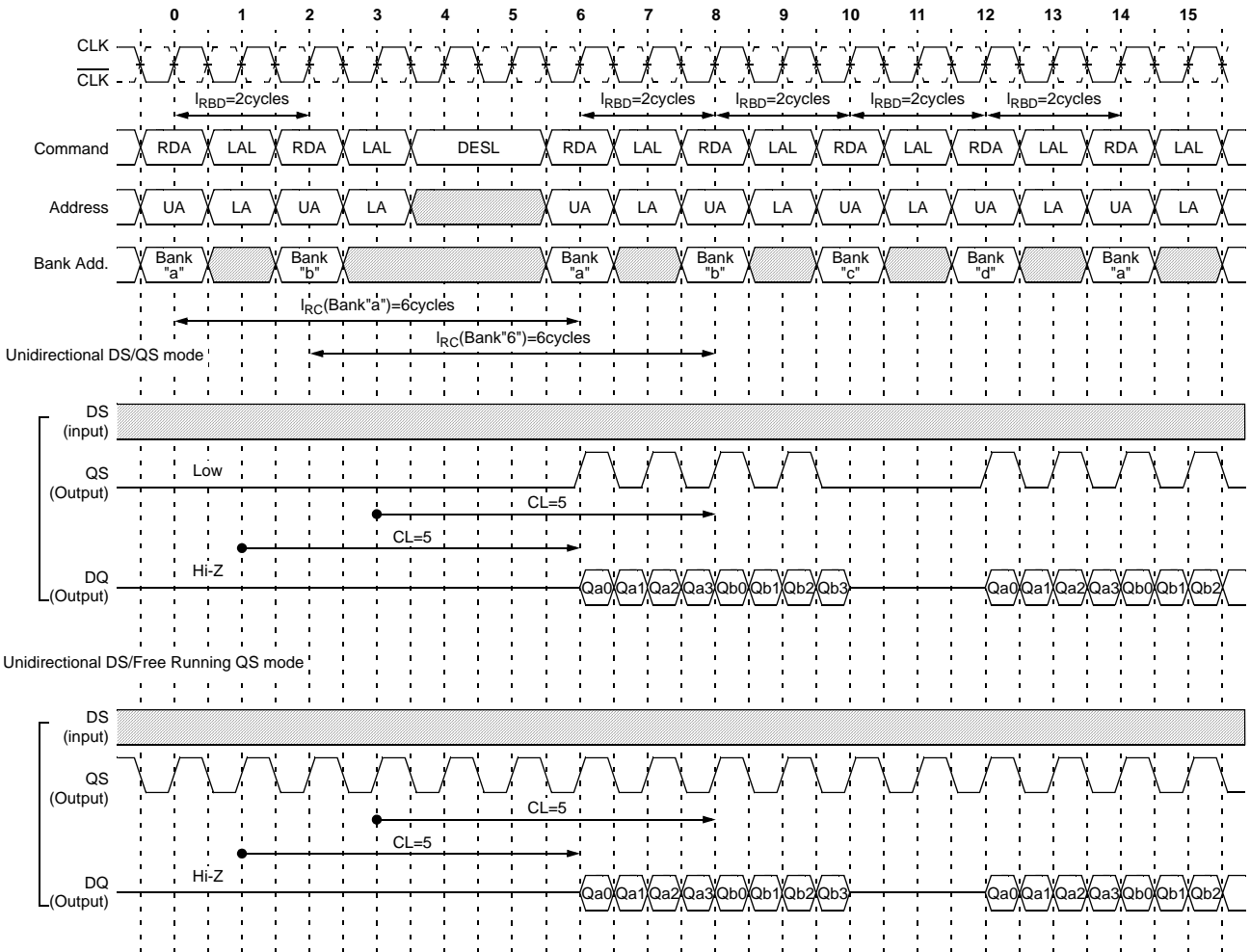
Multiple Bank Read Timing (CL=4)



Note : I_{RC} to the same bank must be satisfied

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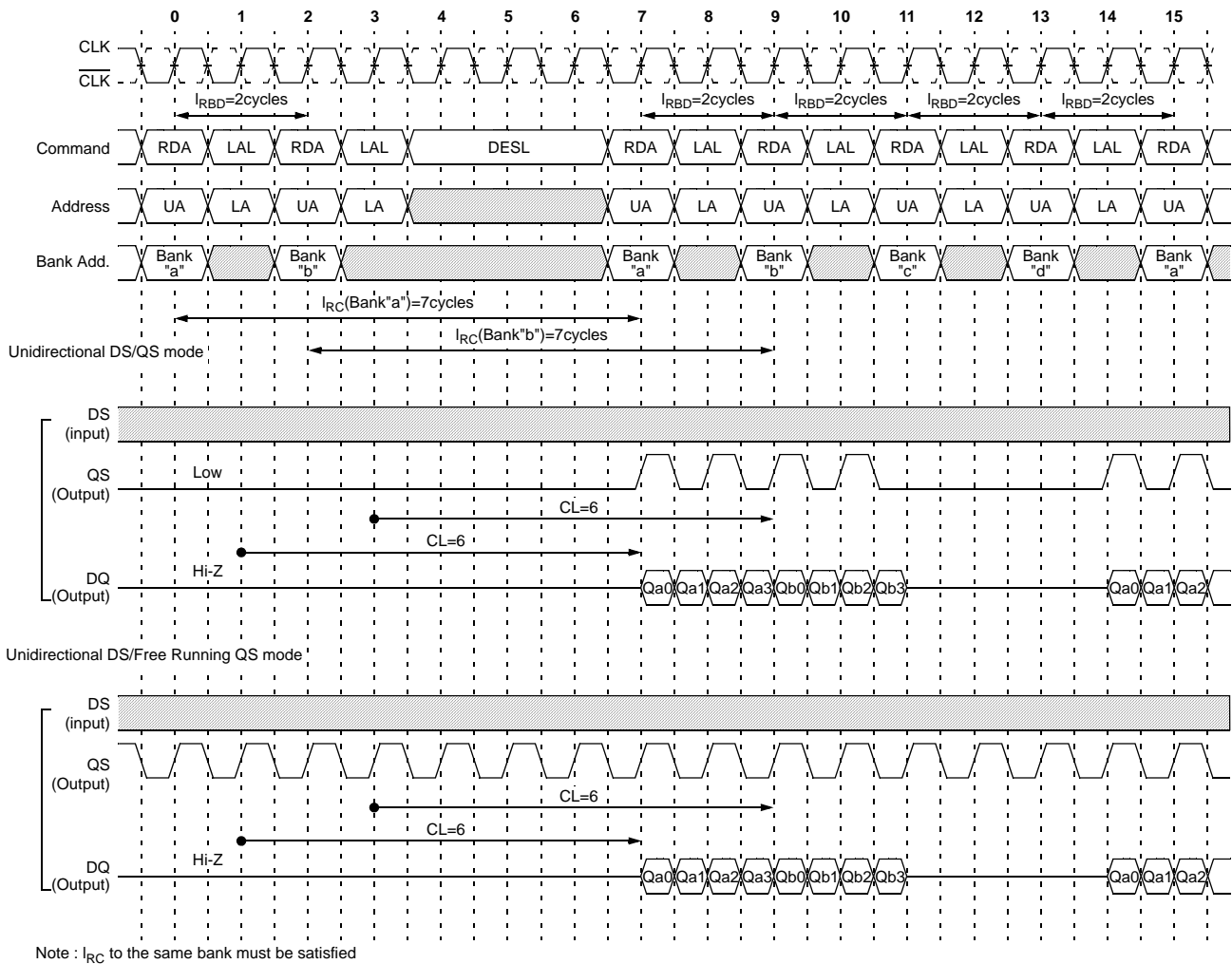
Multiple Bank Read Timing (CL=5)



Note : t_{RC} to the same bank must be satisfied

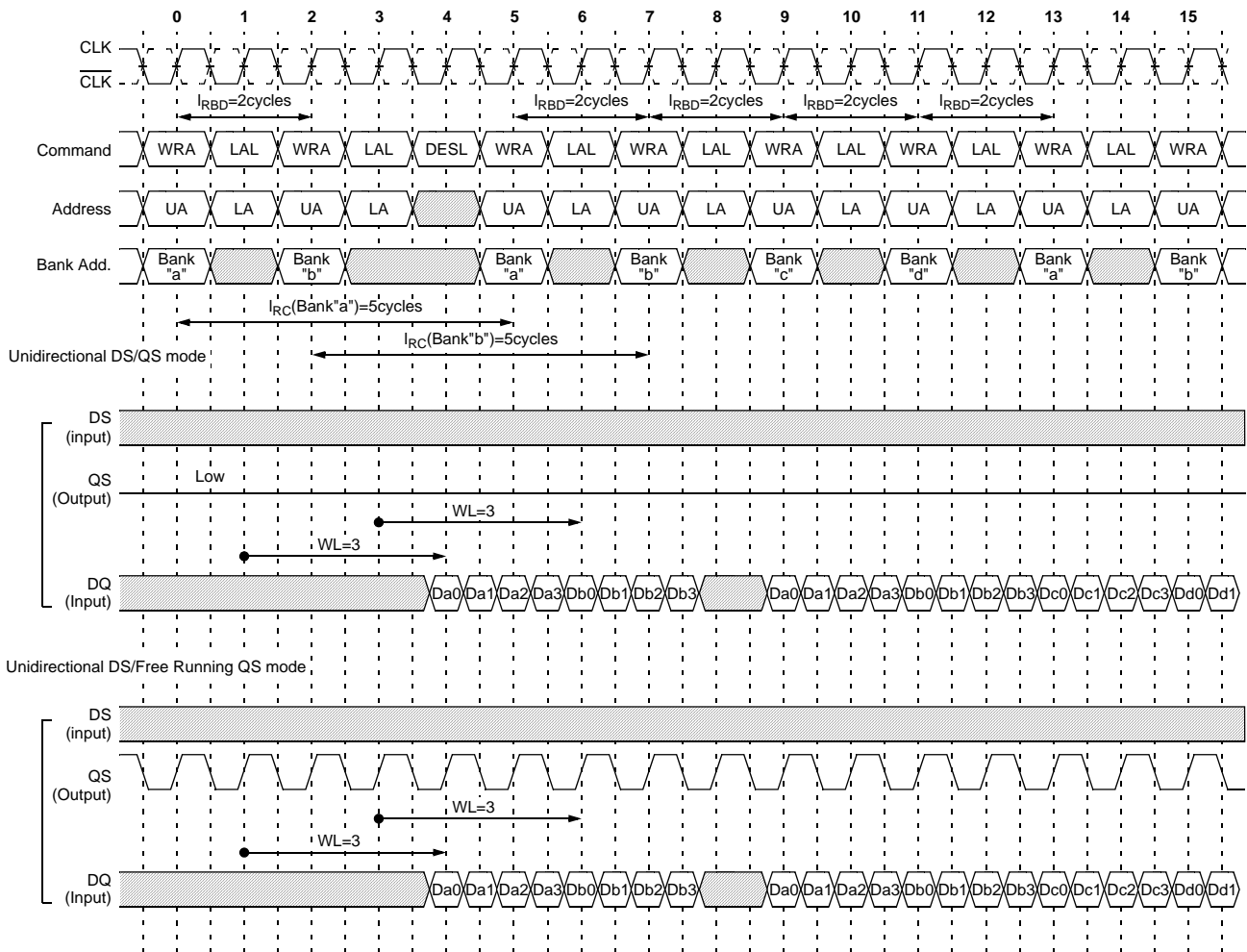
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Multiple Bank Read Timing (CL=6)



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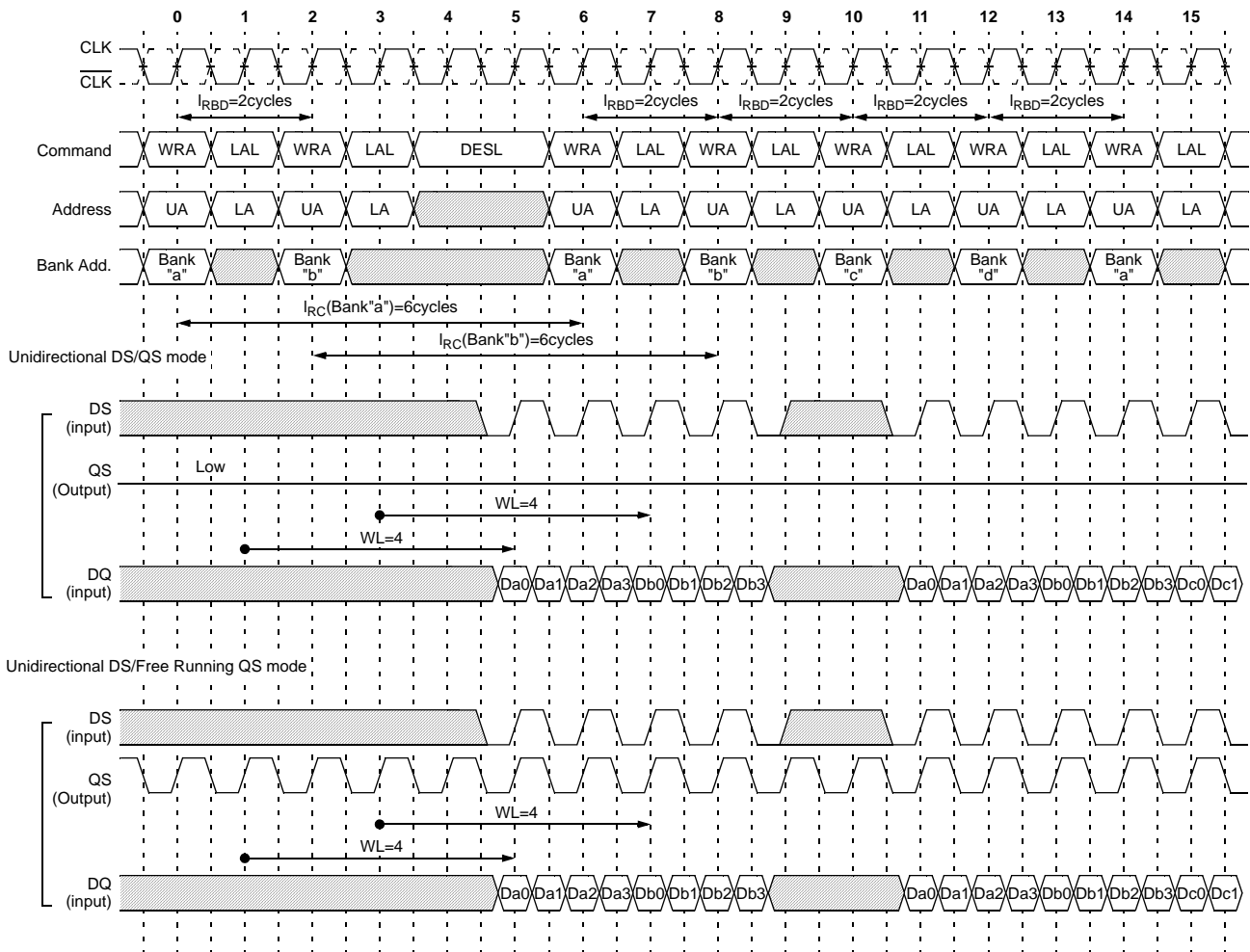
Multiple Bank Write Timing (CL=4)



Note : I_{RC} to the same bank must be satisfied

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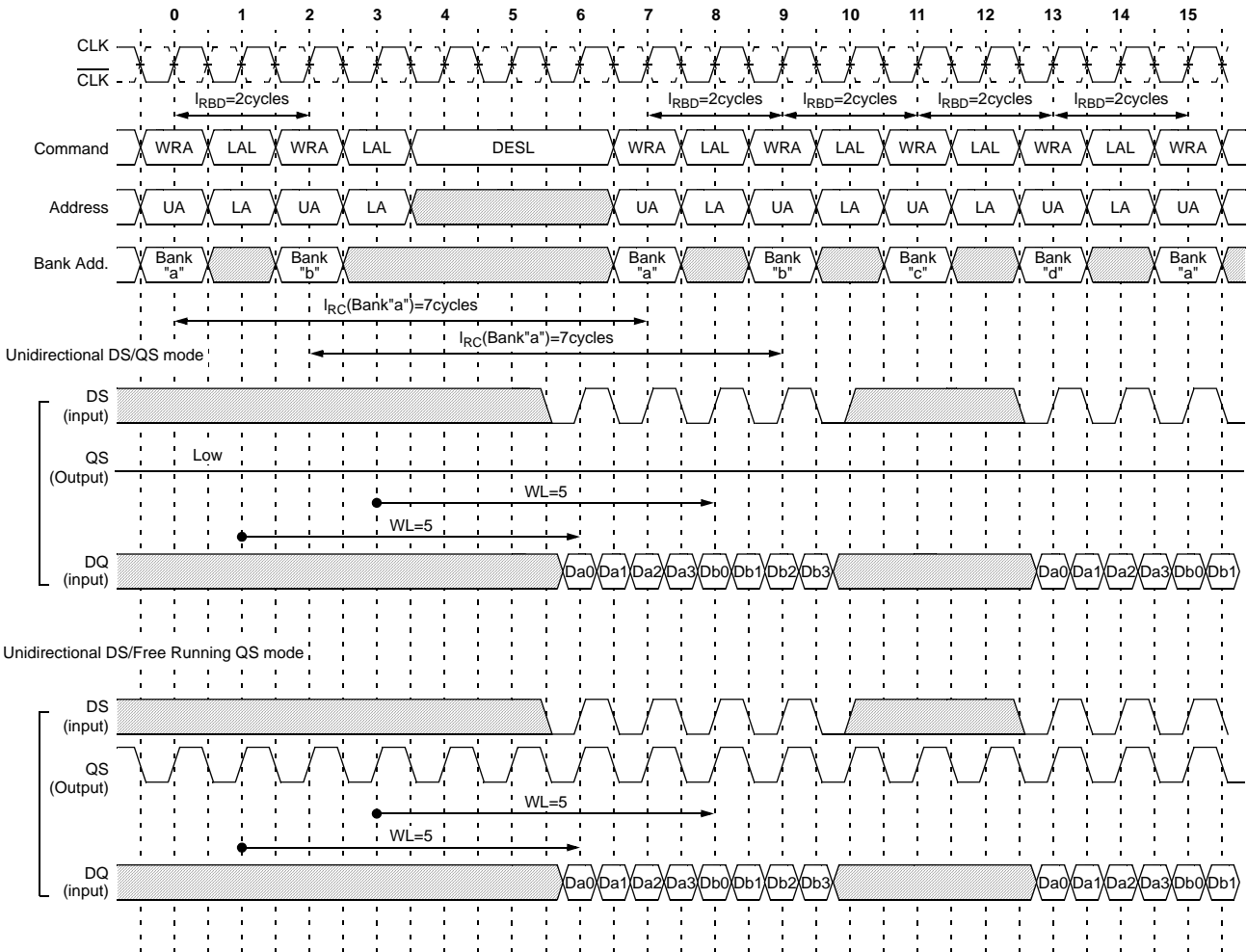
Multiple Bank Write Timing (CL=5)



Note: I_{RC} to the same bank must be satisfied.

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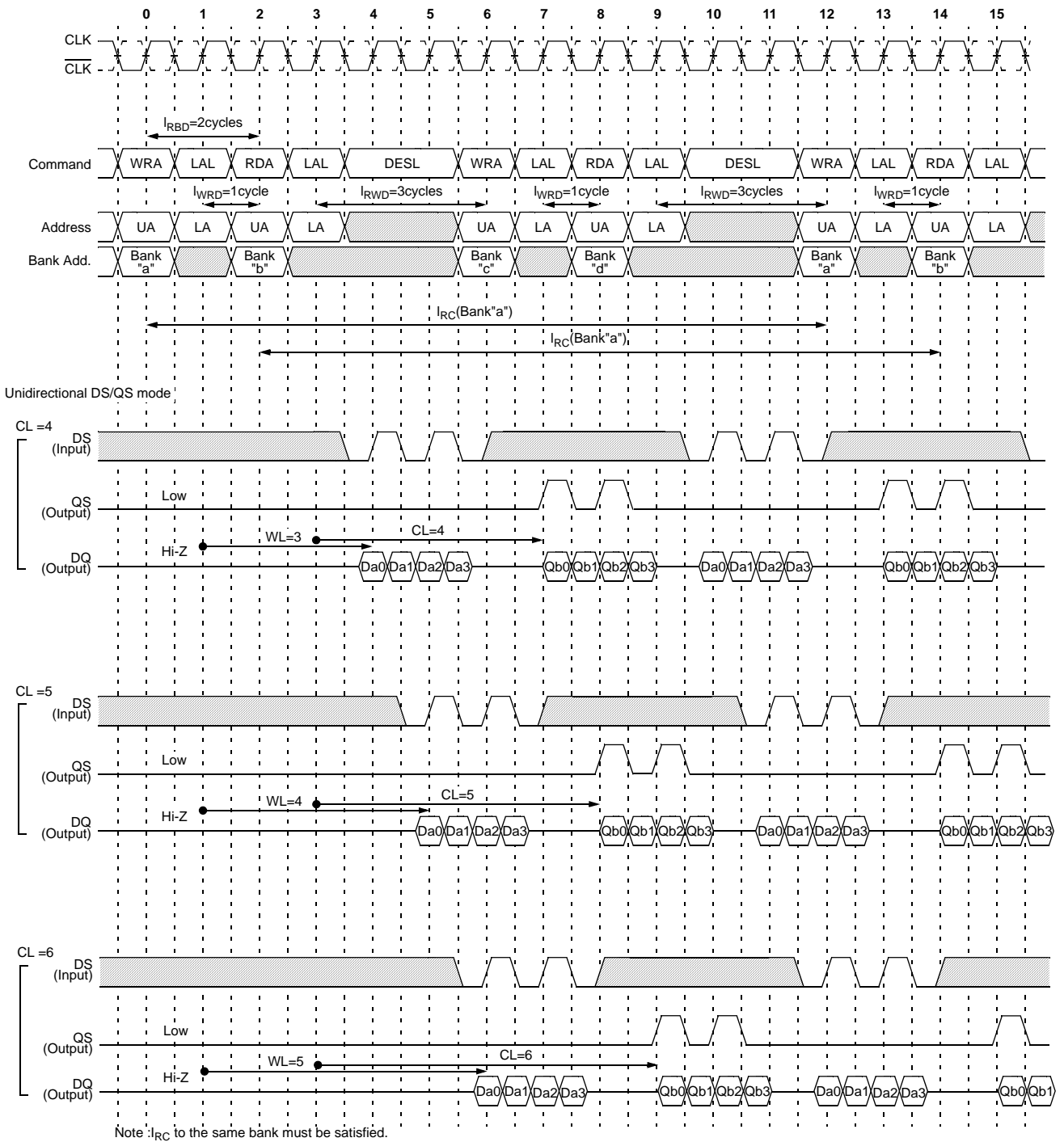
Multiple Bank Write Timing (CL=6)



Note : I_{RC} to the same bank must be satisfied.

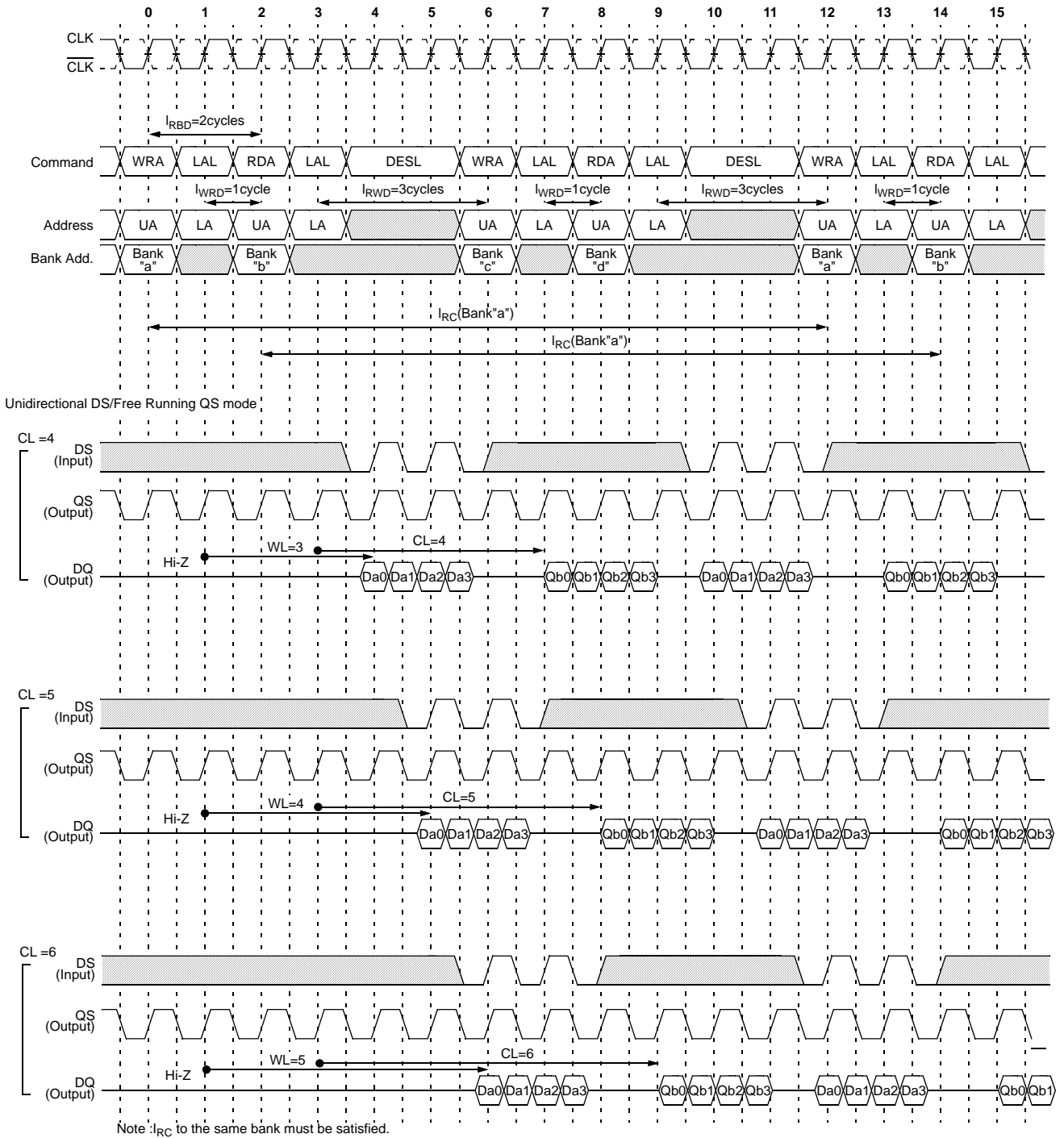
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Multiple Bank Read-Write Timing (BL=4)



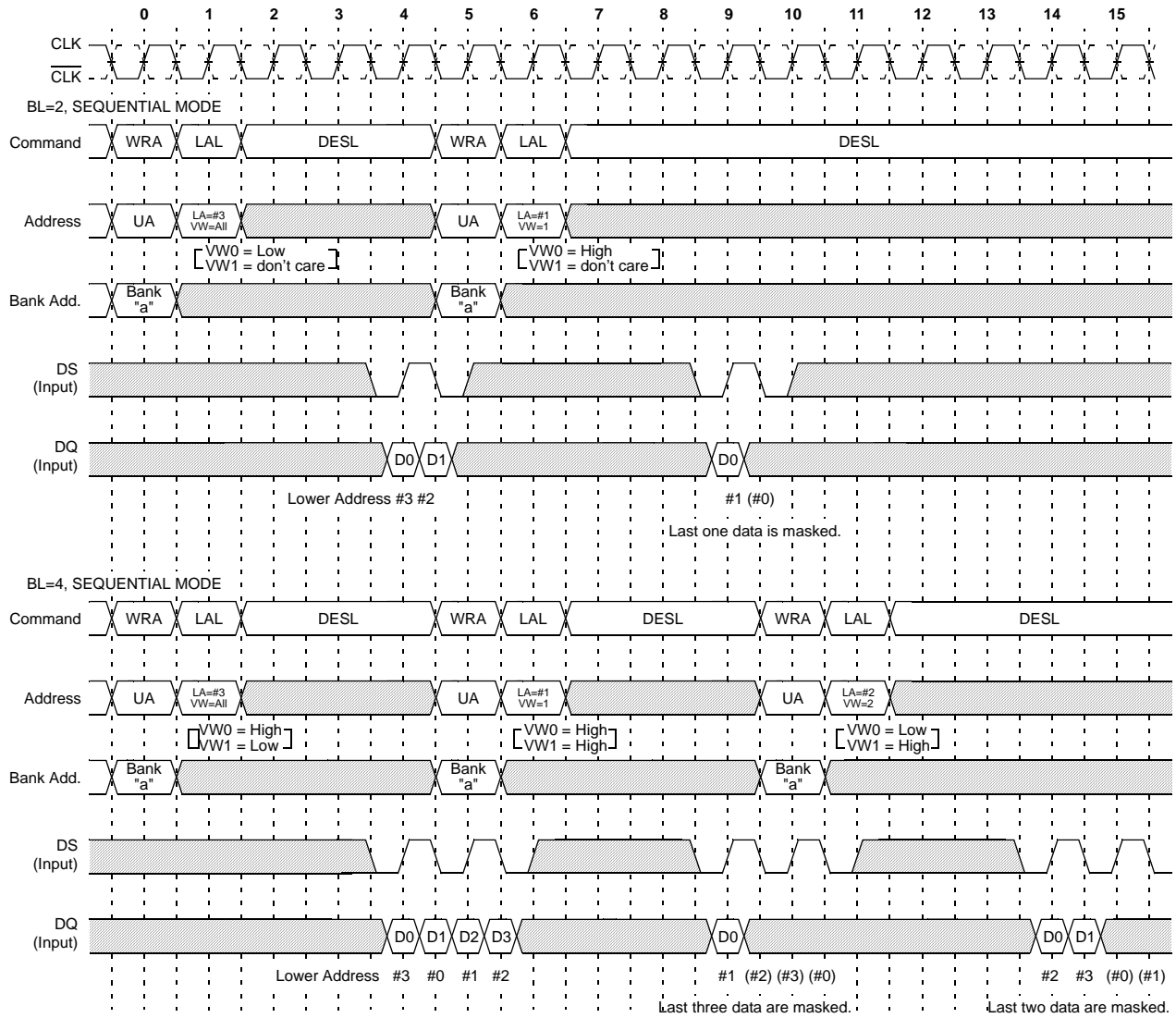
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Multiple Bank Read-Write Timing (BL=4)



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Write with Variable Write Length (VW) Control (CL=4)

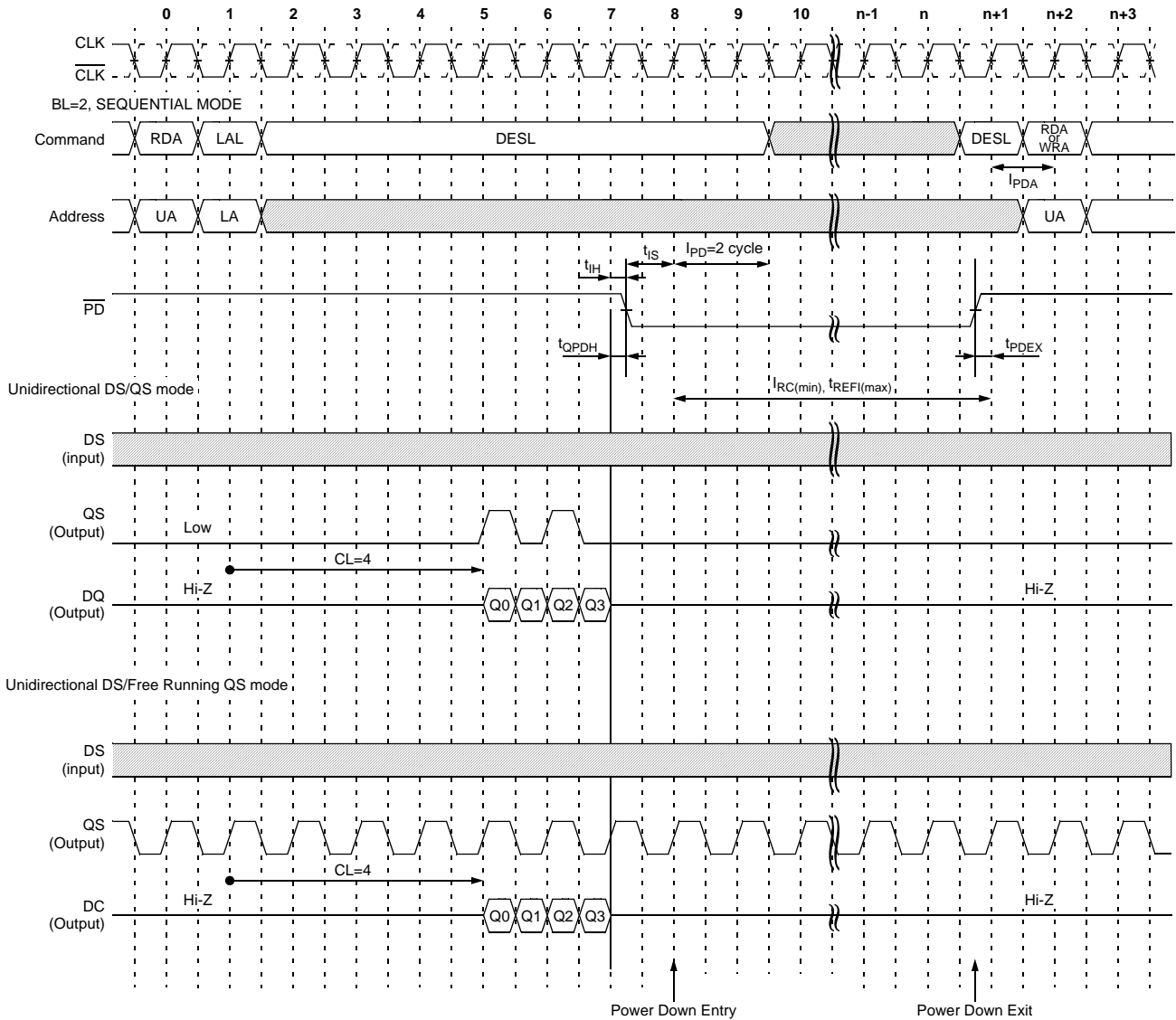


Note : DS input must be continued till end of burst count even if some of later data is masked.

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Power Down Timing (CL=4, BL=4)

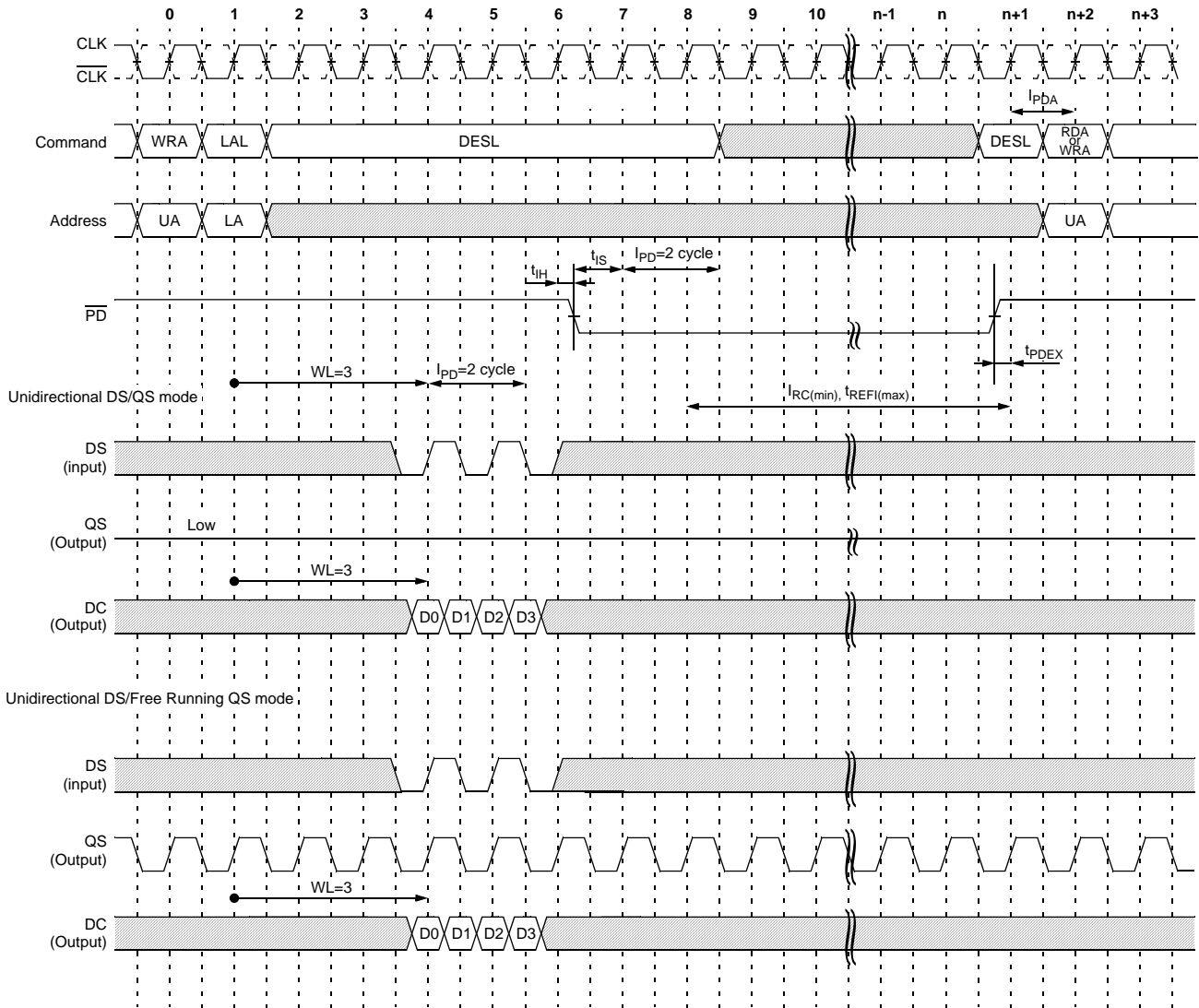
Read cycle to Power Down Mode



Note: \overline{PD} must be kept "High" level until end of Burst data output.
 \overline{PD} should be brought to "High" within $t_{REFI(max)}$ to maintain the data written into cell.
 In Power Down Mode, \overline{PD} "Low" and a stable clock signal must be maintained.
 When \overline{PD} is brought to "High", a valid executable command may be applied I_{PDA} cycles later.

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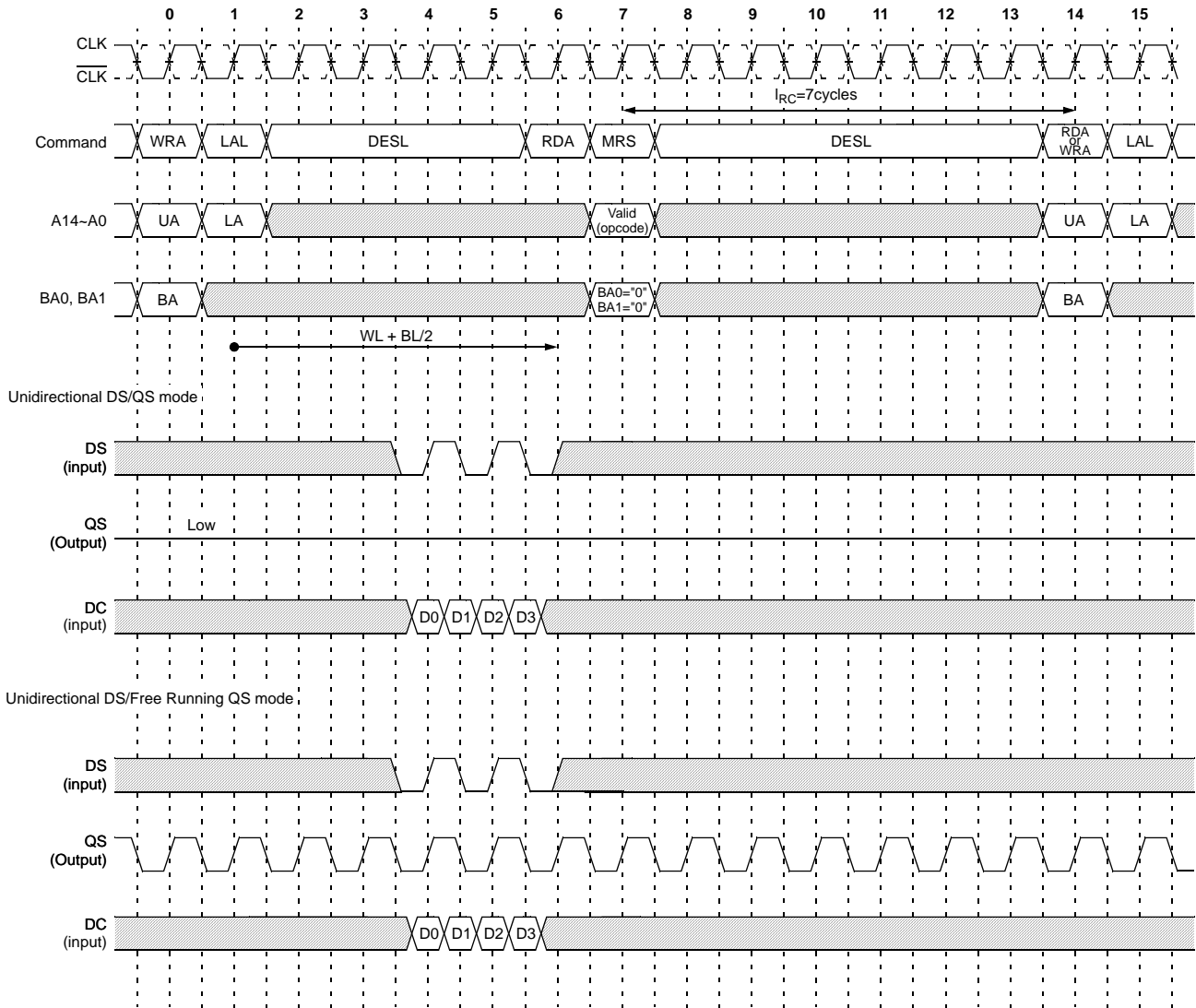
Power Down Timing (CL=4, BL=4) Write cycle to Power Down Mode



Note : \overline{PD} must be kept "High" level until end of Burst data output.
 \overline{PD} should be brought to "High" within $t_{REFI(max)}$ to maintain the data written into cell.
 In Power Down Mode, \overline{PD} "Low" and a stable clock signal must be maintained.
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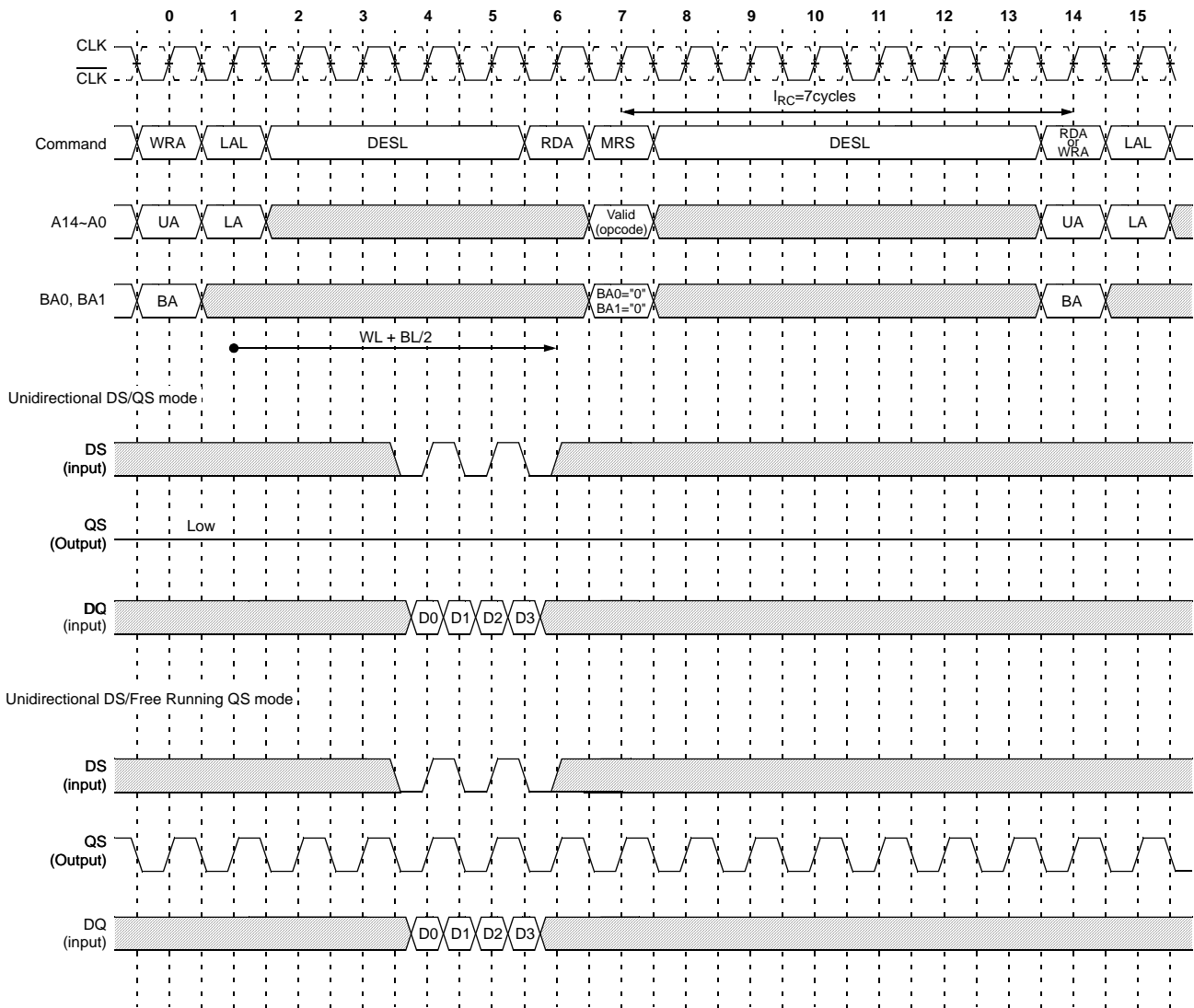
Mode Register Set Timing (CL=4, BL=4) From Write operation to Mode Register Set operation



Note : Minimum delay from LAL following WRA to RDA of MRS operation is $WL+BL/2$.

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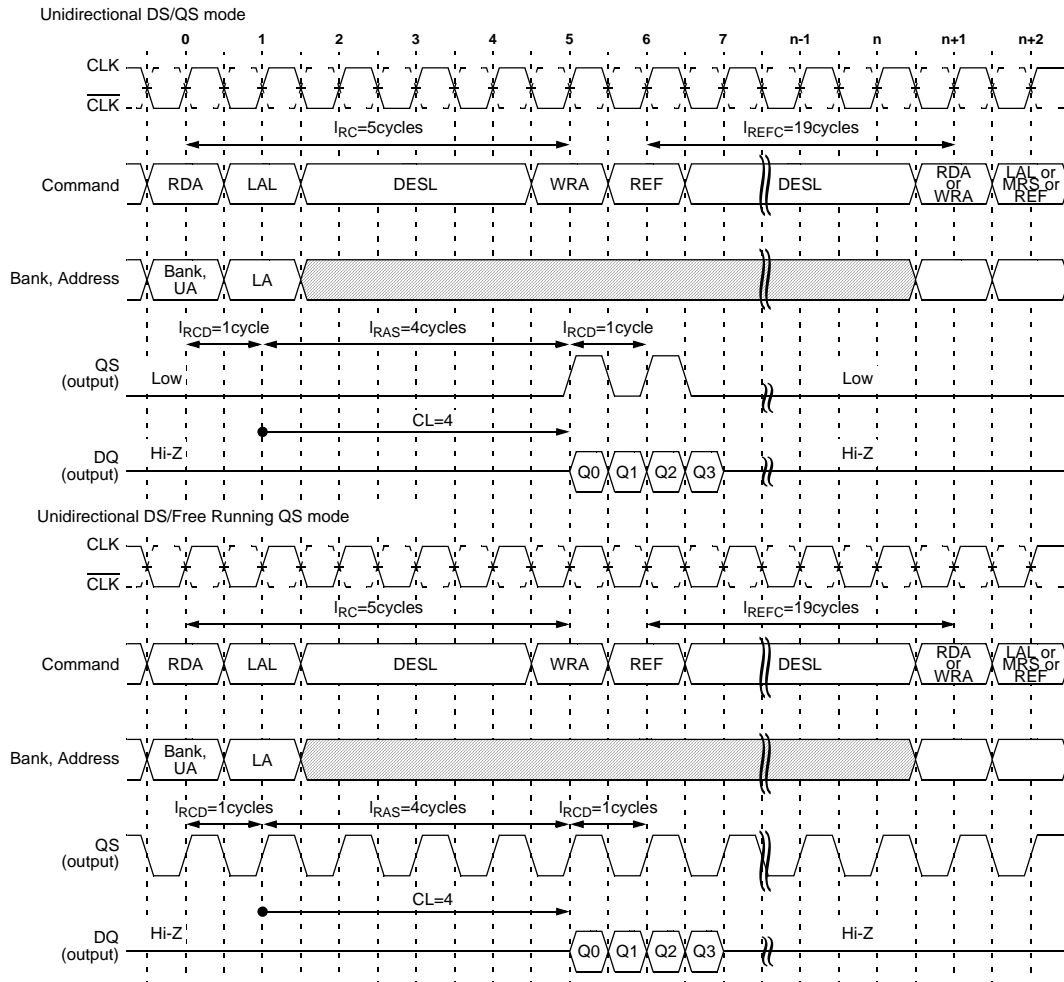
Extended Mode Register Set Timing (CL=4, BL=4) From Write operation to Extended Mode Register Set operation



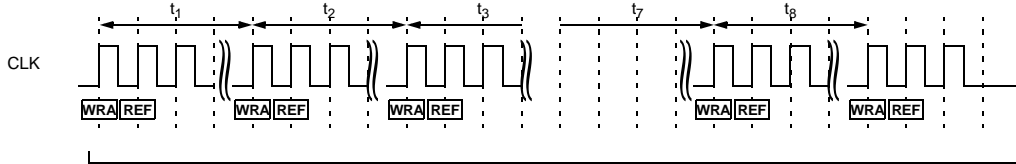
Note : When DQ strobe mode is changed by EMRS, QS output is invalid for I_{RSC} period.
 DLL switch in Extended Mode Register must be set to enable mode for normal operation.
 DLL lock-on time is needed after initial EMRS operation. See Power Up Sequence.
 Minimum delay from LAL following WRA to RDA of EMRS operation is WL+BL/2.

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Auto-Refresh Timing (CL=4, BL=4)



Note : In case of CL=4, t_{REFC} must be meet 19 clock cycles.
 When the Auto-Refresh operation is performed, the synthetic average interval of Auto-Refresh command specified by t_{REFI} must be satisfied.
 t_{REFI} is average interval time in 8 Refresh cycles that is sampled randomly.



8 Refresh cycle

$$t_{REFI} = \frac{\text{Total time of 8 Refresh cycle}}{8} = \frac{t_1+t_2+t_3+t_4+t_5+t_6+t_7+t_8}{8}$$

t_{REFI} is specified to avoid partly concentrated current of Refresh operation that is activated larger are than Read/Write operation.

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Function Description

Network - DRAM

Network - DRAM is an acronym of Double Data Rate Network - DRAM.
Network - DRAM is competent to perform fast random core access, low latency and high-speed data transfer.

Pin Functions

Clock Inputs : CLK & $\overline{\text{CLK}}$

The CLK and $\overline{\text{CLK}}$ inputs are used as the reference for synchronous operation. CLK is master clock input. The $\overline{\text{CS}}$, FN and all address input signals are sampled on the crossing of the positive edge of CLK and the negative edge of $\overline{\text{CLK}}$. The QS and DQ output data are aligned to the crossing point of CLK and $\overline{\text{CLK}}$. The timing reference point for the differential clock is when the CLK and $\overline{\text{CLK}}$ signals cross during a transition.

Power Down : $\overline{\text{PD}}$

The $\overline{\text{PD}}$ input controls the entry to the Power Down or Self-Refresh modes. The $\overline{\text{PD}}$ input does not have a Clock Suspend function like a CKE input of a standard SDRAMs, therefore it is illegal to bring $\overline{\text{PD}}$ pin into low state if any Read or Write operation is being performed.

Chip Select & Function Control : $\overline{\text{CS}}$ & FN

The $\overline{\text{CS}}$ and FN inputs are a control signal for forming the operation commands on Network-DRAM. Each operation mode is decided by the combination of the two consecutive operation commands using the CS and FN inputs.

Bank Addresses : BA0 & BA1

The BA0 and BA1 inputs are latched at the time of assertion of the RDA or WRA command and are selected the bank to be used for the operation. BA0 and BA1 also define which mode register is loaded during the Mode Register Set command (MRS or EMRS).

| | BA0 | BA1 |
|---------|-----|-----|
| Bank #0 | 0 | 0 |
| Bank #1 | 1 | 0 |
| Bank #2 | 0 | 1 |
| Bank #3 | 1 | 1 |

Address Inputs : A0 to A14

Address inputs are used to access the arbitrary address of the memory cell array within each bank. The Upper Addresses with Bank address are latched at the RDA or WRA command and the Lower Addresses are latched at the LAL command. The A0 to A14 inputs are also used for setting the data in the Regular or Extended Mode Register set cycle.

| | Upper Address | Lower Address |
|------------|---------------|---------------|
| K4C89183AF | A0 to A14 | A0 to A6 |

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Functional Description (Continued)

Data Input/Output : DQ0 ~ DQ17

The input data of DQ0 to DQ17 are taken in synchronizing with the both edges of DS input signal.
The output data of DQ0 to DQ17 are outputted synchronizing with the both edges of QS output signal.

Data Strobe : DS or QS

Method of data strobe is chosen by Extended mode register.

(1) Unidirectional DS/QS mode

DS is input signal and QS is output signal. Both edges of DS are used to sample all DQs at Write operation. Both edges of QS are used for trigger signal of all DQs at Read operation. During Write, Auto-Refresh and NOP cycle, QS assert always "Low" level. QS is Hi-Z in Self-Refresh mode.

(2) Unidirectional DS/Free running QS mode

DS is input signal and QS is output signal. Both edges of DS are used to sample all DQs at Write operation. Both edges of QS are used for trigger signal of all DQs at Read operation. QS assert always toggle signal except Self-Refresh mode. This strobe type is easy to use for pin to pin connect application.

Power Supply : V_{DD} , V_{DDQ} , V_{SS} , V_{SSQ}

V_{DD} and V_{SS} are supply pins for memory core and peripheral circuits.

V_{DDQ} and V_{SSQ} are power supply pins for the output buffer.

Reference Voltage : V_{REF}

V_{REF} is reference voltage for all input signals.

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Command Functions and Operations

K4C89093AF is introduced the two consecutive command input method. Therefore, except for Power Down mode, each operation mode decided by the combination of the first command and the second command from stand-by states of the bank to be accessed.

Read Operation (1st command + 2nd command = RDA + LAL)

Issuing the RDA command with Bank Addresses and Upper Addresses to the idle bank puts the bank designated by Bank Address in a read mode. When the LAL command with Lower Addresses is issued at the next clock of the RDA command, the data is read out sequentially synchronizing with the both edges of QS output signal (Burst Read Operation). The initial valid read data appears after CAS latency, the burst length of read data and the burst type must be set in the Mode Register beforehand. The read operated bank goes back automatically to the idle state after I_{RC} .

Write Operation (1st command + 2nd command = WRA + LAL)

Issuing the WRA command with Bank Addresses and Upper Addresses to the idle bank puts the bank designated by Bank Address in a write mode. When the LAL command with Lower Addresses is issued at the next clock of the WRA command, the input data is latched sequentially synchronizing with the both edges of DS input signal (Burst Write Operation). The data and DS inputs have to be asserted in keeping with clock input after \overline{CAS} latency-1 from the issuing of the LAL command. The DS have to be provided for a burst length. The CAS latency and the burst type must be set in the Mode Register beforehand. The write operated bank goes back automatically to the idle state after I_{RC} . Write Burst Length is controlled by VW0 and VW1 inputs with LAL command. See VW truth table.

Auto-Refresh Operation (1st command + 2nd command = WRA + REF)

K4C89093AF is required to refresh like a standard SDRAM. The Auto-Refresh operation is begun with the REF command following to the WRA command. The Auto-Refresh mode can be effective only when all banks are in the idle state and all DQ are in Hi-Z states. In a point to notice, the write mode started with the WRA command is canceled by the REF command having gone into the next clock of the WRA command instead of the LAL command. The minimum period between the Auto-Refresh command and the next command is specified by I_{REFC} . However, about a synthetic average interval of Auto-Refresh command, it must be careful. In case of equally distributed refresh, Auto-Refresh command has to be issued within once for every 3.9 us by the maximum. In case of burst refresh or random distributed refresh, the average interval of eight consecutive Auto-Refresh command has to be more than 400ns always. In other words, the number of Auto-Refresh cycles which can be performed within 3.2 us ($8 \times 400ns$) is to 8 times in the maximum.

Power Down Mode($\overline{PD} = "L"$)

When all banks are in the idle state and all DQ outputs are in Hi-Z states, the K4C89183AF become Power Down Mode by asserting \overline{PD} is "Low". When the device enters the Power Down Mode, all input and output buffers except for \overline{PD} , CLK, \overline{CLK} and QS. Therefore, the power dissipation lowers. To exit the Power Down Mode, \overline{PD} has to be brought to "High" and the DESL command has to be issued for I_{PDA} cycle after \overline{PD} goes high. The Power Down exit function is asynchronous operation.

Mode Register Set (1st command + 2nd command = RDA + MRS)

When all banks are in the idle state, issuing the MRS command following to the RDA command can program the Mode Register. In a point to notice, the read mode started with the RDA command is canceled by the MRS command having gone into the next clock of the RDA command instead of the LAL command. The data to be set in the Mode Register is transferred using A0 to A14, BA0 and BA1 address inputs. The K4C89183AF have two mode registers. These are Regular and Extended Mode Register. The Regular or Extended Mode Register is chosen by BA0 and BA1 in the MRS command. The Regular Mode Register designates the operation mode for a read or write cycle. The Regular Mode Register has four function fields.

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The four fields are as follows :

- (R-1) Burst Length field to set the length of burst data
- (R-2) Burst Type field to designate the lower address access sequence in a burst cycle
- (R-3) $\overline{\text{CAS}}$ Latency field to set the access time in clock cycle
- (R-4) Test Mode field to use for supplier only.

The Extended Mode Register has two function fields.

The two fields are as follows:

- (E-1) DLL Switch field to choose either DLL enable or DLL disable
- (E-2) Output Driver Impedance Control field.
- (E-3) Data Strobe Select

Once these fields in the Mode Register are set up, the register contents are maintained until the Mode Register is set up again by another MRS command or power supply is lost. The initial value of the Regular or Extended Mode Register after power-up is undefined, therefore the Mode Register Set command must be issued before proper operation.

- Regular Mode Register/Extended Mode Register change bits (BA0, BA1)

These bits are used to choose either Regular MRS or Extended MRS

| BA1 | BA0 | A14~A0 |
|-----|-----|--------------------|
| 0 | 0 | Regular MRS cycle |
| 0 | 1 | Extended MRS cycle |
| 1 | X | Reserved |

Regular Mode Register Fields

(R-1) Burst Length field (A2 to A0)

This field specifies the data length for column access using the A2 to A0 pins and sets the Burst Length to be 4 words.

| A2 | A1 | A0 | Burst Length |
|----|----|----|--------------|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 4 words |
| 0 | 1 | 1 | Reserved |
| 1 | X | X | Reserved |

(R-2) Burst Type field (A3)

This Burst Type can be chosen Interleave mode or Sequential mode. When the A3 bit is "0", Sequential mode is selected. When the A3 bit is "1", Interleave mode is selected. Both burst types support burst length of 2 and 4 words.

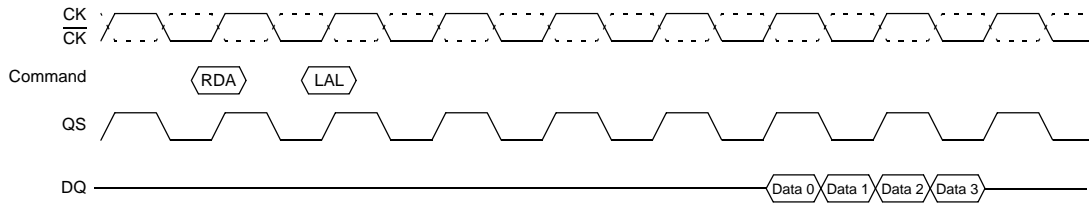
| A3 | Burst Type |
|----|------------|
| 0 | Sequential |
| 1 | Interleave |

- Addressing sequence of Sequential mode (A3)

A column access is started from the inputted lower address and is performed by incrementing the lower address input to the device.

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CAS Latency = 4 (Free Running QS mode)



Addressing sequence for Sequential mode

| Data | Access Address | Burst Length |
|--------|----------------|--|
| Data 0 | n | 4 words (Address bits is LA1, LA0) not carried from LA1~LA2 |
| Data 1 | n + 1 | |
| Data 2 | n + 2 | |
| Data 3 | n + 3 | |

Functional Description (Continued)

- Addressing sequence of Interleave mode

A column access is started from the inputted lower address and is performed by interleaving the address bits in the sequence shown as the following.

Addressing sequence for Interleave mode

| Data | Access Address | Burst Length |
|--------|--|--------------|
| Data 0 | ...A8 A7 A6 A5 A4 A3 A2 A1 A0 | 4 words |
| Data 1 | ...A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$ | |
| Data 2 | ...A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0 | |
| Data 3 | ...A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$ | |

(R-3) CAS Latency field (A6 to A4)

This field specifies the number of clock cycles from the assertion of the LAL command following the RDA command to the first data read. The minimum values of CAS Latency depends on the frequency of CLK. In a write mode, the place of clock which should input write data is CAS Latency cycles - 1.

Addressing sequence for Interleave mode

| A6 | A5 | A4 | CAS Latency |
|----|----|----|-------------|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

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(R-4) Test Mode field (A7)

This bit is used to enter Test Mode for supplier only and must be set to "0" for normal operation.

(R-5) Reserved field in the Regular Mode Register

• Reserved bits (A8 to A14)

These bits are reserved for future operations. They must be set to "0" for normal operation.

Extended Mode Register Fields

(E-1) DLL Switch field (A0)

This bit is used to enable DLL. When the A0 bit is set "0", DLL is enabled.

(E-2) Output Driver Impedance Control field (A1 to A4)

This field is used to choose Output Driver Strength. Four types of Driver Strength are supported. QS and DQ Driver Strength can be chosen separately. A2-A1 specified the DQ Driver Strength. A4-A3 specified the QS Driver Strength.

| QS | | DQ | | Output Driver Impedance Control |
|----|----|----|----|---------------------------------|
| A4 | A3 | A2 | A1 | |
| 0 | 0 | 0 | 0 | Normal Output Driver |
| 0 | 1 | 0 | 1 | Strong Output Driver |
| 1 | 0 | 1 | 0 | Weaker Output Driver |
| 1 | 1 | 1 | 1 | Reserved |

(E-3) Strobe Select (A6/A5)

Two types of strobe are supported. This field is used to choose the type of data strobe.

(1) Unidirectional DS/QS mode

Data strobe is separated DS for write strobe and QS for read strobe.

DS is used to sample write data at write operation. QS is aligned with read data at Read operation.

(2) Unidirectional DS/Free running QS mode

Data strobe is separated DS for write strobe and QS for read strobe.

DS is used to sample write data at write operation. QS is aligned with read data and always clocking

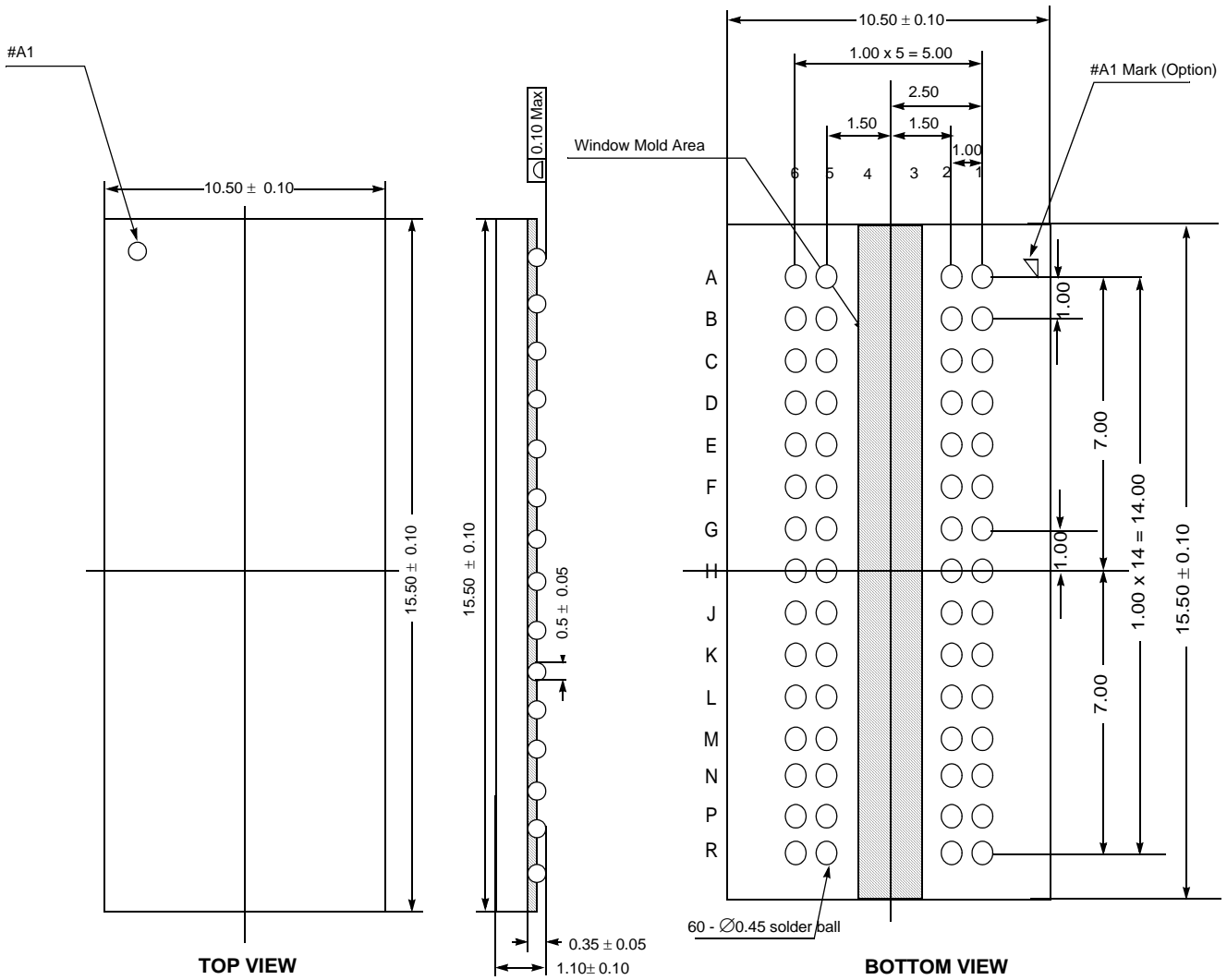
| A6 | A5 | Strobe Select |
|----|----|--|
| 0 | 0 | Reserved |
| 0 | 1 | Reserved |
| 1 | 0 | Unidirectional DS/QS mode |
| 1 | 1 | Unidirectional DS/Free running QS mode |

(E-4)Reserved field (A7 to A14)

These bits are reserved for future operations and must be set to "0" for normal operation.

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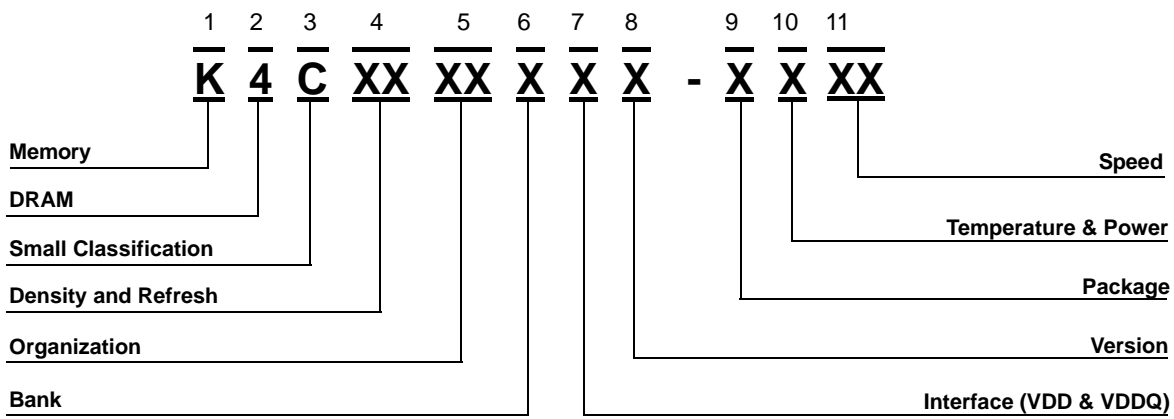
Package Outline Drawing (FBGA 60ball, 1.0 x 1.0 mm)



K4C89183AF

General Information

| Organization | F6 (667Mbps@CL6) | FB (600Mbps@CL6) | F5 (500Mbps@CL6) |
|--------------|------------------|-------------------|--------------------|
| 288M(x9) | K4C89093AF-ACF6 | K4C89093AF-ACFB | K4C89093AF-AC(I)F5 |
| 288M(x18) | K4C89183AF-ACF6 | K4C89183AF-ACFB | K4C89183AF-AC(I)F5 |
| 288M(x36) | K4C89363AF-GCF6 | K4C89363AF-GCFB | K4C89363AF-GC(I)F5 |



1. SAMSUNG Memory : K

2. DRAM : 4

3. Small Classification
C : Network-DRAM

4. Density & Refresh
89 : 288M 8K/32ms

5. Organization

08 : x8
09 : x9
16 : x16
18 : x18

6. Bank

3 : 4 Bank

7. Interface (VDD & VDDQ)

A: SSTL-2(2.5V, 1.8V)

8. Version

F : 7th Generation

9. Package

A : 60 FBGA
G : 144 FBGA

10. Temperature & Power

C : (Commercial, Normal)
I : (Industrial, Normal)

11. Speed

F6 : 667Mbps/pin (333MHz, CL=6)
FB : 600Mbps/pin (300MHz, CL=6)
F5 : 500Mbps/pin (250MHz, CL=6)