R8800

16-Bit RISC Microcontroller User's Manual

RDC ***RISC DSP Controller***

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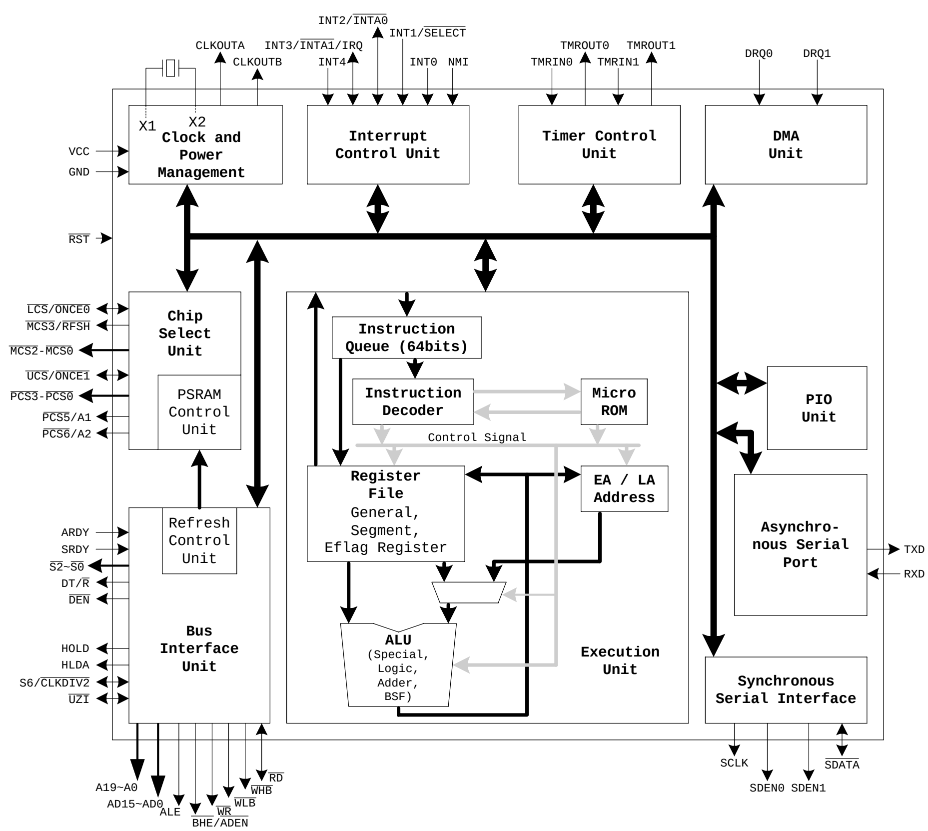
16-Bit Microcontroller with 16-bit external data bus

Features

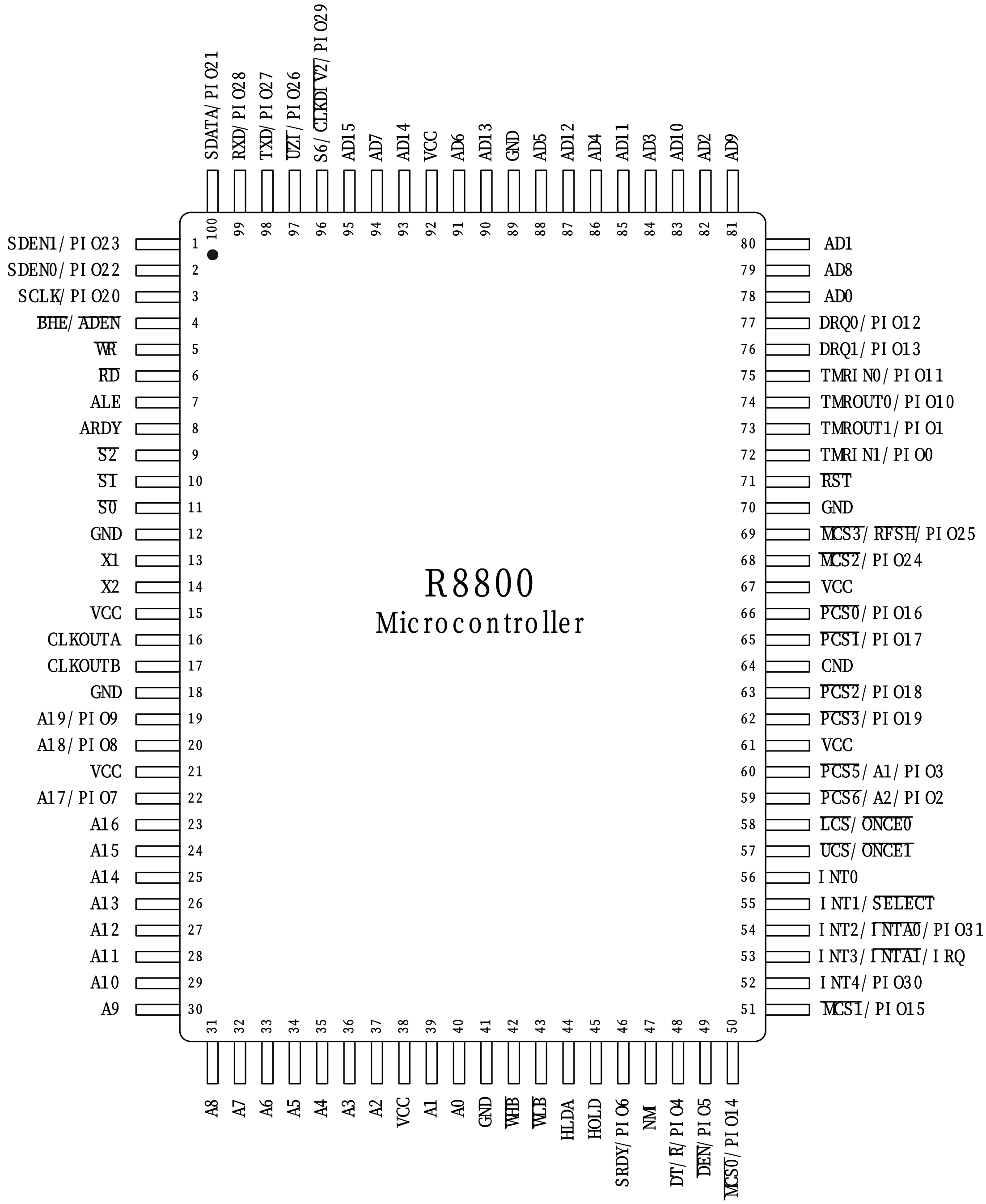
- Five-stage pipelines
- RISC architecture
- Static design & Synthesizable design
- Bus interface
  - Multiplexed address and data bus which is compatible with 80C186 microprocessor
  - Supports nonmultiplexed address bus [A19 : A0]
  - 1MByte memory address space
  - 64K byte I/O space
- Software is compatible with the 80C186 microprocessor
- Support one Asynchronous serial channel & one Synchronous serial channel
- Supports 32 PIO pins
- PSRAM (Pseudo static RAM) interface with auto-refresh control
- Three independent 16-bit timers and Timer 1 can be programmed as a watchdog timer
- The Interrupt controller with five maskable external interrupts and one nonmaskable external interrupt
- Two independent DMA channels
- Programmable chip-select logic for Memory or I/O bus cycle decoder
- Programmable wait-state generator
- Support CPU ID

Block Diagram

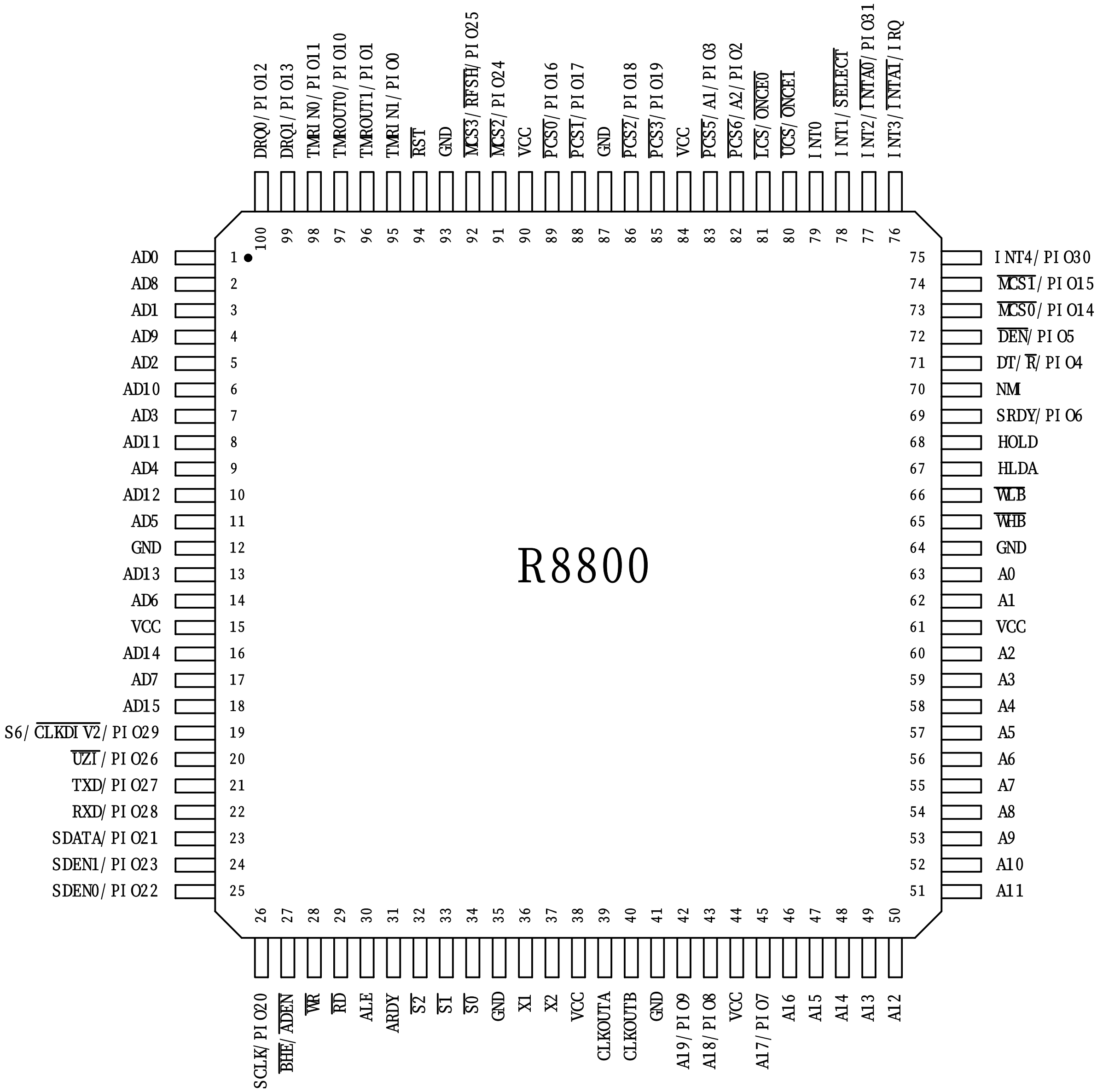


Pin Configuration

(PQFP)



(LQFP)



R8800 PQFP and LQFP Pin-Out table

Pin name	LQFP Pin No.	PQFP Pin No.	Pin name	LQFP Pin No.	PQFP Pin No.
AD0	1	78	A11	51	28
AD8	2	79	A10	52	29
AD1	3	80	A9	53	30
AD9	4	81	A8	54	31
AD2	5	82	A7	55	32
AD10	6	83	A6	56	33
AD3	7	84	A5	57	34
AD11	8	85	A4	58	35
AD4	9	86	A3	59	36
AD12	10	87	A2	60	37
AD5	11	88	VCC	61	38
GND	12	89	A1	62	39
AD13	13	90	A0	63	40
AD6	14	91	GND	64	41
VCC	15	92	$\overline{WHB}$	65	42
AD14	16	93	$\overline{WLB}$	66	43
AD7	17	94	HLDA	67	44
AD15	18	95	HOLD	68	45
S6/ $\overline{UZI}$ /PIO29	19	96	SRDY/PIO6	69	46
$\overline{UZI}$/PIO26	20	97	NMI	70	47
TXD/PIO27	21	98	DT/ $\overline{R}$ /PIO4	70	48
RXD/PIO28	22	99	$\overline{DEN}$ /PIO5	72	49
SDATA/PIO21	23	100	$\overline{MCS0}$/PIO14	73	50
SDEN1/PIO23	24	1	$\overline{MCS1}$/PIO15	74	51
SDEN0/PIO22	25	2	I NT4/ PIO30	75	52
SCLK/PIO20	26	3	I NT3/$\overline{INTA1}$/I RQ	76	53
$\overline{BHE}$ / $\overline{ADEN}$	27	4	I NT2/$\overline{INTA0}$/PIO31	77	54
$\overline{WR}$	28	5	I NT1/$\overline{SELECT}$	78	55
$\overline{RD}$	29	6	I NT0	79	56
ALE	30	7	$\overline{UCS}$/$\overline{CNCE1}$	80	57
ARDY	31	8	$\overline{LCS}$/$\overline{CNCE0}$	81	58
$\overline{S2}$	32	9	$\overline{PCS6}$ /A2/PIO2	82	59
$\overline{S1}$	33	10	$\overline{PCS5}$ /A1/PIO3	83	60
$\overline{S0}$	34	11	VCC	84	31
GND	35	12	$\overline{PCS3}$/PIO19	85	62
X1	36	13	$\overline{PCS2}$/PIO18	86	63
X2	37	14	GND	87	64
VCC	38	15	$\overline{PCS1}$/PIO17	88	65
CLKOUTA	39	16	$\overline{PCS0}$/PIO16	89	66
CLKOUTB	40	17	VCC	90	67
GND	41	18	$\overline{MCS2}$ /PI O24	91	68
A19/PIO9	42	19	$\overline{MCS3}$/ $\overline{RFSH}$/PIO25	92	69
A18/PIO8	43	20	GND	93	70
VCC	44	21	$\overline{RST}$	94	71
A17/PIO7	45	22	TMRI N1/PIO0	95	72
A16	46	23	TMROUT1/PIO1	96	73
A15	47	24	TMROUT0/PIO10	97	74
A14	48	25	TMRI N0/PIO11	98	75
A13	49	26	DRQ1/PIO13	99	76
A12	50	27	DRQ0/PIO12	100	77

Pin Description

Pin No.(PQFP)	Symbol	Type	Description
15, 21, 38, 61, 67, 92	VCC	Input	System power: +5 volt power supply.
12, 18, 41, 64, 70, 89	GND	Input	System ground.
71	$\overline{RST}$	Input*	Reset input. When $\overline{RST}$ is asserted, the CPU immediately terminate all operations, clears the internal registers & logic, and the address transfers to the reset address FFFF0h.
13	X1	Input	Input to the oscillator amplifier.
14	X2	Output	Output from the inverted oscillator amplifier.
16	CLKOUTA	Output	Clock output A. The CLKOUTA operation is the same as crystal input frequency (X1). CLKOUTA remains active during reset and bus hold conditions.
17	CLKOUTB	Output	Clock output B. The CLKOUTB operation is the same as crystal input frequency (X1). CLKOUTB remains active during reset and bus hold conditions.
Synchronous Serial Port Interface			
1 2	SDEN1/PIO23 SDEN0/PIO22	Output/Input	Serial data enables. Active-high. These pins enable data transfers of the synchronous serial interface. SDEN1 for port1, SDEN0 for port0.
3	SCLK/PIO20	Output/Input	Synchronous serial data clock. This pin provides the shift clock to an external device. SCLK=X1/2, 4, 8 or 16 depending on register setting. This pin held high during the UART inactive.
100	SDATA/PIO21	Input/Output	Synchronous serial data. This pin provides the shift data to or receives a serial data from an external device.
Asynchronous Serial Port Interface			
98	TXD/PIO27	Output/Input	Transmit data. This pin transmits asynchronous serial data from the UART of the microcontroller.
99	RXD	Input	Receive data. This pin receives asynchronous serial data.
Bus Interface			
4	$\overline{BHE}$ / $\overline{ADEN}$	Output/Input	Bus high enable/address enable. During a memory access, the $\overline{BHE}$ and (AD0 or A0) encodings indicate what type of the bus cycle. $\overline{BHE}$ is asserted during T1 and keeps the asserted to T3 and Tw. This pin is floating during bus hold and reset. $\overline{BHE}$ and (AD0 or A0) Encodings $\overline{BHE}$ / AD0 or A0 / Type of Bus Cycle 0 / 0 / Word transfer 0 / 1 / High byte transfer (D15-D8) 1 / 0 / Low byte transfer (D7-D0) 1 / 1 / Refresh The address portion of the AD bus can be enabled or disabled by DA bit in the LMCS and UMCS register during LCS or UCS bus cycle access, if $\overline{BHE}$ / $\overline{ADEN}$ is held high during power-on reset. The $\overline{BHE}$ / $\overline{ADEN}$ with an internal weak pull-up register, so no external pull-up register is required. The AD bus always drives both address and data during LCS or UCS bus cycle access, if the $\overline{BHE}$ / $\overline{ADEN}$ pin with external pull-low resister during reset.
5	$\overline{WR}$	Output	Write strobe. This pin indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active during T2, T3 and Tw of any write cycle, floats during a bus hold or

<table>
<tr><td></td><td></td><td></td><td>reset.</td></tr>
<tr><td>6</td><td>$\overline{RD}$</td><td>Output</td><td>Read Strobe. Active low signal which indicates that the microcontroller is performing a memory or I/O read cycle. $\overline{RD}$ floats during bus hold or reset.</td></tr>
<tr><td>7</td><td>ALE</td><td>Output</td><td>Address latch enable. Active high. This pin indicates that an address output on the AD bus. Address is guaranteed to be valid on the trailing edge of ALE. This pin is tri-stated during ONCE mode and is never floating during a bus hold or reset.</td></tr>
<tr><td>8</td><td>ARDY</td><td>Input</td><td>Asynchronous ready. This pin performs the microcontroller that the address memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUTA and is active high. The falling edge of ARDY must be synchronized to CLKOUTA. Tie ARDY high, the microcontroller is always asserted in the ready condition. If the ARDY is not used, tie this pin low to yield control to SRDY.
Both SRDY and ARDY should be tied to high if the system need not assert wait state by externality.</td></tr>
<tr><td>9
10
11</td><td>$\overline{S2}$
$\overline{S1}$
$\overline{S0}$</td><td>Output</td><td>Bus cycle status. These pins are encoded to indicate the bus status. $\overline{S2}$ can be used as memory or I/O indicator. $\overline{S1}$ can be used as DT/$\overline{R}$ indicator. These pins are floating during hold and reset.
<table>
<tr><th colspan="4">Bus Cycle Encoding Description</th></tr>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Bus Cycle</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read data from I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write data to I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read data from memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write data to memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table></td></tr>
<tr><td>19
20
22
23-37
39, 40</td><td>A19/PIO9
A18/PIO8
A17/PIO7
A16-A2
A1 , A0</td><td>Output/Input</td><td>Address bus. Non-multiplexed memory or I/O address. The A bus is one-half of a CLKOUTA period earlier than the AD bus. These pins are high-impedance during bus hold or reset.</td></tr>
<tr><td>78,80,82,84,86,88
91,94
79,81,83,85,87,90
93,95</td><td>AD0-AD7

AD8-AD15</td><td>Input/Output</td><td>The multiplexed address and data bus for memory or I/O accessing. The address is present during the t1 clock phase, and the data bus phase is in t2-t4 cycle.
The address phase of the AD bus can be disabled when the $\overline{BHE}$ / $\overline{ADEN}$ pin with external pull-low resister during reset.
The AD bus is in high-impedance state during bus hold or reset condition and this bus also be used to load system configuration information (with pull-up or pull-Low resister) into the F6h register when the reset input from low go high.</td></tr>
<tr><td>42</td><td>$\overline{WHB}$</td><td>Output</td><td>Write high byte. This pin indicates the high byte data (AD15-AD8) on the bus is to be written to a memory or I/O device.
This pin is floating during reset or bus hold.</td></tr>
<tr><td>43</td><td>$\overline{WLB}$</td><td>Output</td><td>Write low byte. This pin indicates the low byte data (AD7-AD0) on the bus is to be written to a memory or I/O device.</td></tr>
</table>

			This pin is floating during reset or bus hold.
44	HLDA	Output	Bus hold acknowledge. Active high. The microcontroller will issue an HLDA in response to a HOLD request by external bus master at the end of T4 or Ti. When the microcontroller is in hold status (HLDA is high), the AD15-AD0, A19-A0, $\overline{WR}$, $\overline{RD}$, $\overline{DEN}$, $\overline{S0}$ - $\overline{S1}$, $\overline{S6}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{WHB}$ and $\overline{WLB}$ are floating, and the $\overline{UCS}$, $\overline{LCS}$, $\overline{PCS6}$ - $\overline{PCS5}$, $\overline{MCS3}$ - $\overline{MCS0}$ and $\overline{PCS3}$ - $\overline{PCS0}$ will be drive high. After HOLD is detected as being low, the microcontroller will lower HLDA.
45	HOLD	Input	Bus Hold request. Active high. This pin indicates that another bus master is requesting the local bus.
46	SRDY/PIO6	Input/Output	Synchronous ready. This pin performs the microcontroller that the address memory space or I/O device will complete a data transfer. The SRDY pin accepts a falling edge that is asynchronous to CLKOUTA and is active high. SRDY is accomplished by elimination of the one-half clock period required to internally synchronize ARDY. Tie SRDY high the microcontroller is always assert in the ready condition. If the SRDY is not used, tie this pin low to yield control to ARDY. Both SRDY and ARDY should be tied to high if the system need not assert wait state by externality.
48	DT/$\overline{R}$ /PIO4	Output/Input	Data transmit or receive. This pin indicates the direction of data flow through an external data-bus transceiver. DT/$\overline{R}$ low, the microcontroller receives data. When DT/R is asserted high, the microcontroller writes data to the data bus.
49	$\overline{DEN}$ /PIO5	Output/Input	Data enable. This pin is provided as a data bus transceiver output enable. $\overline{DEN}$ is asserted during memory and I/O access. $\overline{DEN}$ is drived high when DT/$\overline{R}$ changes state. It is floating during bus hold or reset condition.
96	S6/$\overline{CLKDIV2}$ /PIO29	Output/Input	Bus cycle status bit6/clock divided by 2. For S6 feature, this pin is low to indicate a microcontroller-initiated bus cycle or high to indicate a DMA-initiated bus cycle during T2, T3, Tw and T4. For $\overline{CLKDIV2}$ feature. The internal clock of microcontroller is the external clock be divided by 2. (CLKOUTA, CLKOUTB=X1/2), if this pin held low during power-on reset. The pin is sampled on the rising edge of $\overline{RST}$.
97	$\overline{UZI}$ /PIO26	Output/Input	Upper zero indicate. This pin is the logical OR of the inverted A19-A16. It asserts in the T1 and is held throughout the cycle.
Chip Select Unit Interface			
50 51 68 69	$\overline{MCS0}$ /PIO14 $\overline{MCS1}$ /PIO15 $\overline{MCS2}$ /PIO24 $\overline{MCS3}$ / $\overline{RFSH}$ /PIO25	Output/Input	Midrange memory chip selects. For $\overline{MCS}$ feature, these pins are active low when enable the MMCS(A6h) register to access a memory. The address ranges are programmable. $\overline{MCS3}$ - $\overline{MCS0}$ are held high during bus hold. When programming LMCS(A6h) register, pin69 is as a $\overline{RFSH}$ pin to auto refresh the PSRAM.
57	$\overline{UCS}$ / $\overline{ONCE1}$	Output/Input	Upper memory chip select/ONCE mode request 1. For $\overline{UCS}$ feature, this pin acts low when system accesses the defined portion memory block of the upper 512K bytes (80000h-FFFFFh) memory region. $\overline{UCS}$ default acted address region is from F0000h to FFFFFh after power-on reset.

			The address range acting $\overline{UCS}$ is programmed by software. For $\overline{ONCE1}$ feature. If $\overline{ONCE0}$ and $\overline{ONCE1}$ are sampled low on the rising edge of $\overline{RST}$. The microcontroller enters ONCE mode. In ONCE mode, all pins are high-impedance. This pin incorporates weakly pull-up resistor.
58	$\overline{LCS}$ / $\overline{ONCE0}$	Output/Input	Lower memory chip select/ONCE mode request 0. For $\overline{LCS}$ feature, this pin acts low when the microcontroller accesses the defined portion memory block of the lower 512K (00000h-7FFFFh) memory region. The address range acting $\overline{LCS}$ is programmed by software. For $\overline{ONCE0}$ feature, see $\overline{UCS}$ / $\overline{ONCE1}$ description. This pin incorporates weakly pull-up register.
59 60	$\overline{PCS6}$ /A2/PIO2 $\overline{PCS5}$ /A1/PIO3	Output/Input	Peripheral chip selects/latched address bit. For $\overline{PCS}$ feature, these pins act low when the microcontroller accesses the fifth or sixth region of the peripheral memory (I/O or memory space). The base address of $\overline{PCS}$ is programmable. These pins assert with the AD address bus and are not float during bus hold. For latched address bit feature. These pins output the latched address A2, A1 when cleared the EX bit in the $\overline{MCS}$ and $\overline{PCS}$ auxiliary register. The A2, A1 retains previous latched data during bus hold.
62 63 65 66	$\overline{PCS3}$ /PIO19 $\overline{PCS2}$ /PIO18 $\overline{PCS1}$ /PIO17 $\overline{PCS0}$ /PIO16	Output/Input	Peripheral chip selects. These pins act low when the microcontroller accesses the defined memory area of the peripheral memory block (I/O or memory address). For I/O accessed, the base address can be programmed in the region 00000h to 0FFFFh. For memory address access, the base address can be located in the 1M byte memory address region. These pins assert with the multiplexed AD address bus and are not float during bus hold.
Interrupt Control Unit Interface			
47	NMI	Input	Nonmaskable Interrupt. The NMI is the highest priority hardware interrupt and is nonmaskable. When this pin is asserted (NMI transition from low to high), the microcontroller always transfers the address bus to the location specified by the nonmaskable interrupt vector in the microcontroller interrupt vector table. The NMI pin must be asserted for at least one CLKOUTA period to guarantee that the interrupt is recognized.
52	INT4/PIO30	Input/Output	Maskable interrupt request 4. Act high. This pin indicates that an interrupt request has occurred. The microcontroller will jump to the INT4 address vector to execute the service routine if the INT4 is enable. The interrupt input can be configured to be either edge- or level-triggered. The requesting device must holt the INT4 until the request is acknowledged to guarantee interrupt recognition.
53	INT3/ $\overline{INTA1}$ /IRQ	Input/Output	Maskable interrupt request 3/interrupt acknowledge 1/slave interrupt request. For INT3 feature, except the difference interrupt line and interrupt address vector, the function of INT3 is the same as INT4. For $\overline{INTA1}$ feature, in cascade mode or special fully-nested mode, this pin corresponds the INT1. For IRQ feature, when the microcontroller is as a slave device, this pin issues an interrupt request to the master interrupt

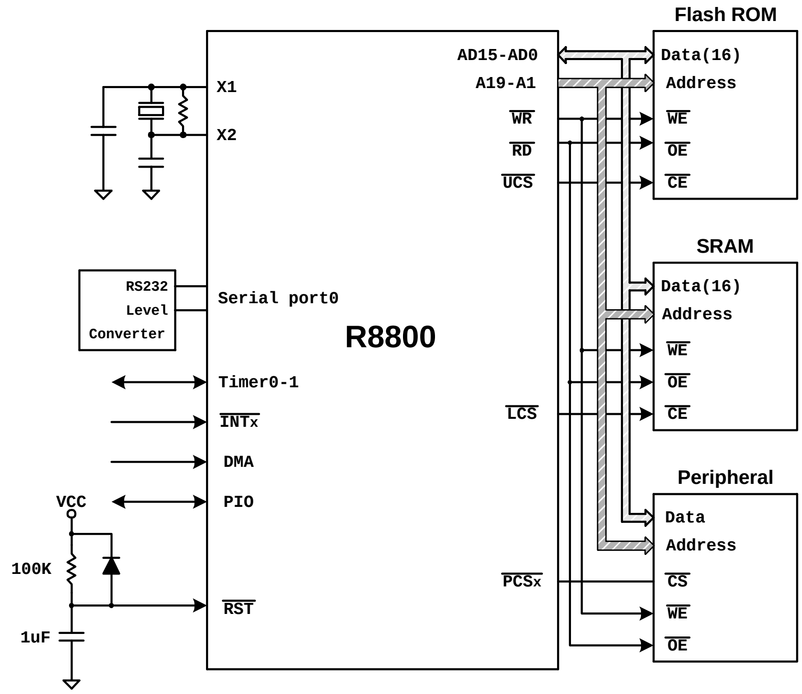
			controller.
54	INT2/ $\overline{\text{INTA0}}$ /PIO31	Input/Output	Maskable interrupt request 2/interrupt acknowledge 0. For INT2 feature, except the difference interrupt line and interrupt address vector, the function of INT2 is the same as INT4. For $\overline{\text{INTA0}}$ feature, in cascade mode or special fully-nested mode, this pin corresponds the INT0.
55	INT1/ $\overline{\text{SELECT}}$	Input/Output	Maskable interrupt request 1/slave select. For INT1 feature, except the difference interrupt line and interrupt address vector, the function of INT1 is the same as INT4. For $\overline{\text{SELECT}}$ feature, when the microcontroller is as a slave device, this pin is drived from the master interrupt controller decoding. This pin acts to indicate that an interrupt appears on the address and data bus. The INT0 must act before $\overline{\text{SELECT}}$ acts when the interrupt type appears on the bus.
56	INT0	Input	Maskable interrupt request 0. Except the interrupt line and interrupt address vector, the function of INT0 is the same as INT4.
Timer Control Unit Interface			
72 75	TMRIN1/PIO0 TMRIN0/PIO11	Input/Output	Timer input. These pins can be as clock or control signal input, which depend upon the programmed timer mode. After internally synchronizing low to high transitions on TMRIN, the timer controller increments. These pins must be pull-up if not being used.
73 74	TMROUT1/PIO1 TMROUT0/PIO10	Output/Input	Timer output. Depending on timer mode select these pins provide single pulse or continuous waveform. The duty cycle of the waveform can be programmable. These pins are floated during a bus hold or reset.
DMA Unit Interface			
76 77	DRQ1/PIO13 DRQ0/PIO12	Input/Output	DMA request. These pins are asserted high by an external device when the device is ready for DMA channel 1 or channel 0 to perform a transfer. These pins are level-triggered and internally synchronized. The DRQ signals must remain act until finish serviced and are not latched.

Notes:

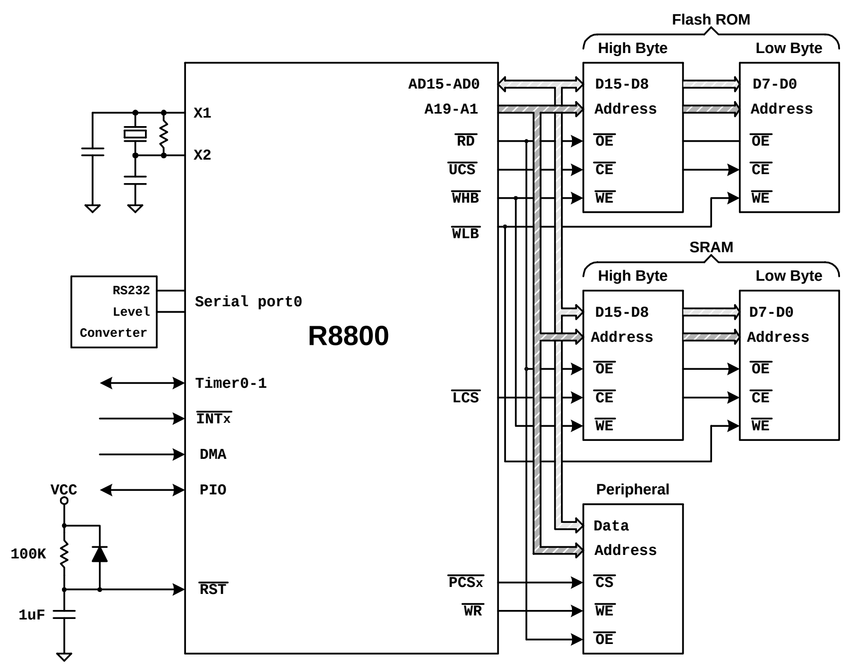
1.When enable the PIO Data register, there are 32 MUX definition pins can be as a PIO pin. For example, the DRD1/PIO13 (pin76) can be as a PIO13 when enable the PIO Data register.

2.The PIO status during Power-On reset : PIO1, PIO10, PIO22, PIO23 are input with pull-down, PIO4 to PIO9 are normal operation and the others are input with pull-up.

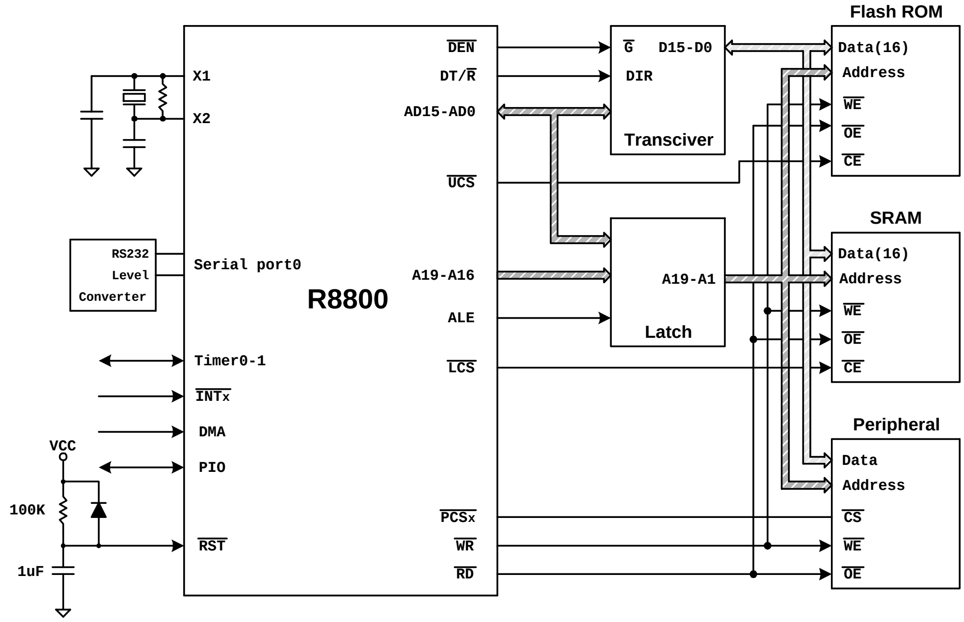
Basic Application System Block



BASIC APPLICATION SYSTEM BLOCK (A)

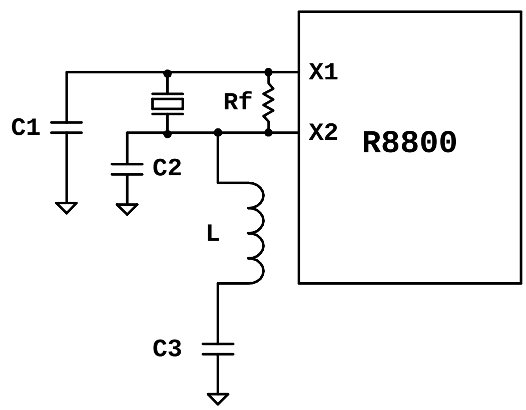


BASIC APPLICATION SYSTEM BLOCK (B)



BASIC APPLICATION SYSTEM BLOCK (C)

Oscillator Characteristics



For fundamental -mode crystal:

Reference valve

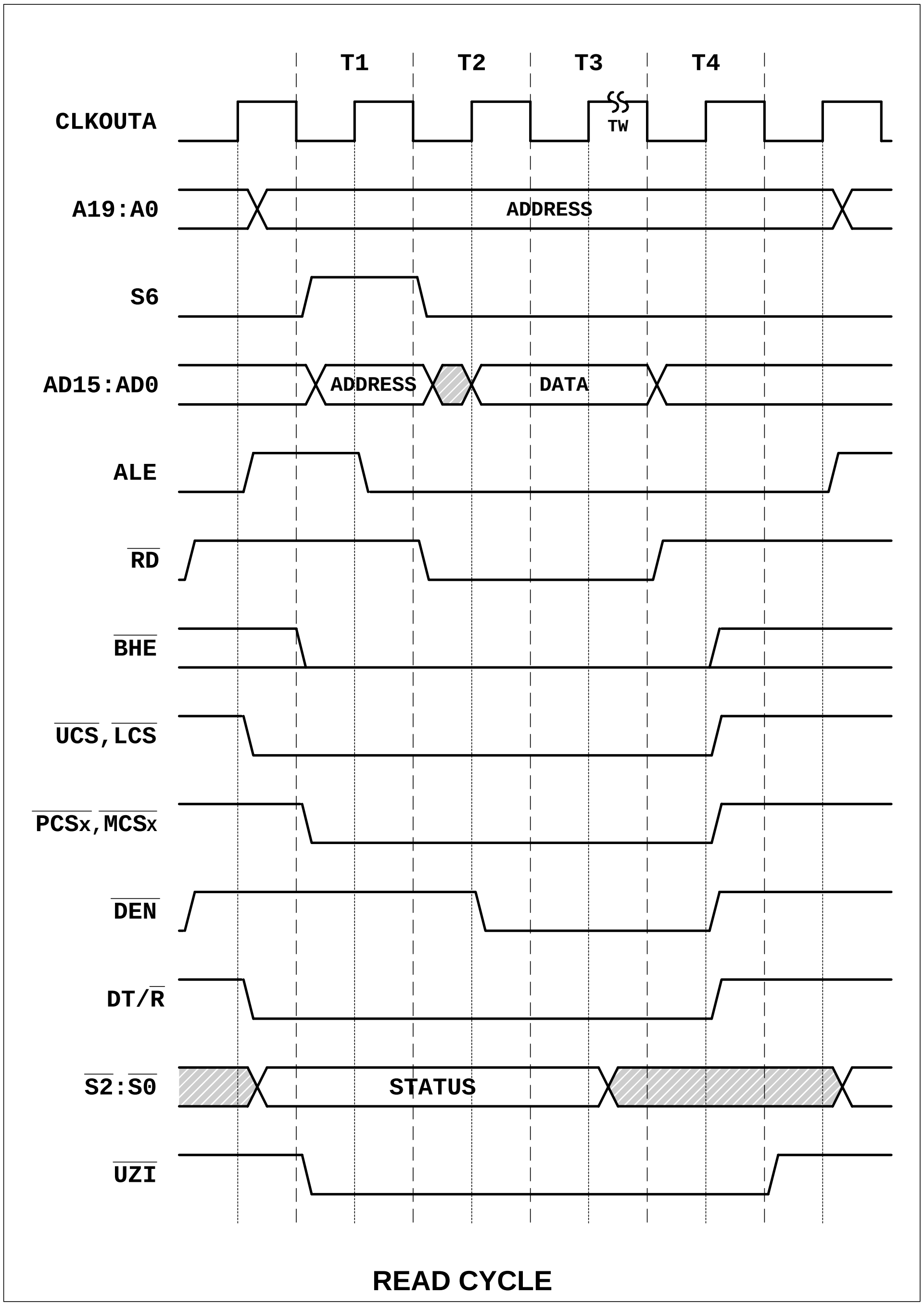
Frequency	10.8288M Hz	19.66M Hz	30M Hz	33M Hz	40M Hz
Rf	None	None	None	None	None
C1	10Pf	10Pf	None	None	None
C2	10Pf	10Pf	10Pf	10Pf	10Pf
C3	None	None	None	None	None
L	None	None	None	None	None

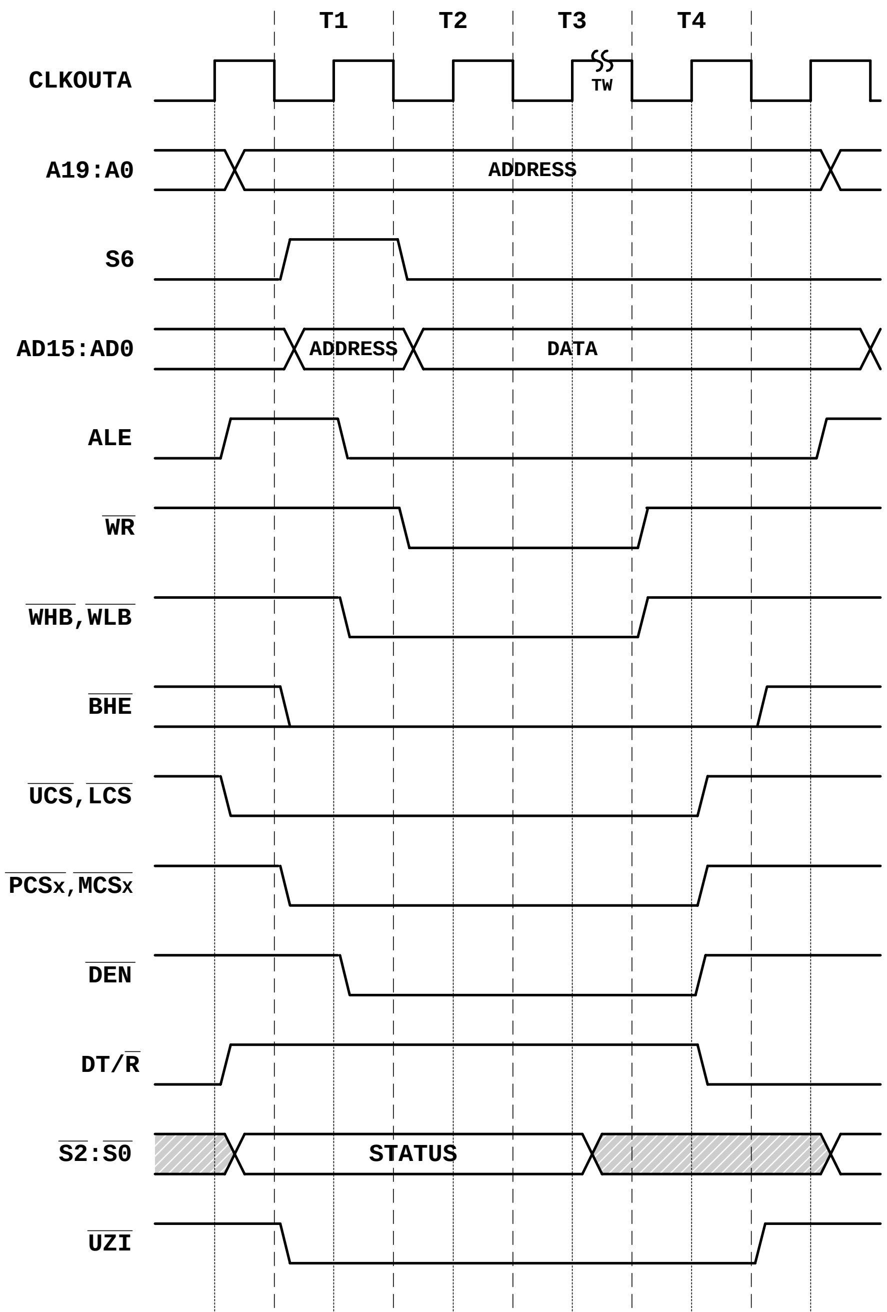
For third-overtone mode crystal:

Reference valve

Frequency	22.1184M Hz	28.322M Hz	33.177M Hz	40M Hz	44.1M Hz
Rf	1M	1.5M	1.5M	1.5M	1.5M
C1	15Pf	15Pf	15Pf	15Pf	15Pf
C2	30Pf	30Pf	30Pf	30Pf	30Pf
C3		220Pf	220Pf	220Pf	120Pf
L		10uL	4.7uL	2.7uL	2.7uL

Read/Write timing Diagram




T1
T2
T3
T4
CLKOUTA
TW
A19:A0
ADDRESS
S6
AD15:AD0
ADDRESS
DATA
ALE
WR
WHB,WLB
BHE
UCS,LCS
PCSx,MCSx
DEN
DT/R
S2:S0
STATUS
UZI

WRITE CYCLE

Execution Unit

General Register

The R8800 has eight 16-bit general registers. And the AX,BX,CX,DX can be subdivided into two 8-bit register (AH,AL,BH, BL,CH,CL,DH,DL). Tthe functions of these registers are described as follows.

AX : Word Divide , Word Multiply, Word I/O operation.

AH : Byte Divide , Byte Multiply, Byte I/O , Decimal Arithmetic, Translate operation.

AL : Byte Divide , Byte Multiply operation.

BX : Translate operation.

CX : Loops, String operation

CL : Variable Shift and Rotate operation.

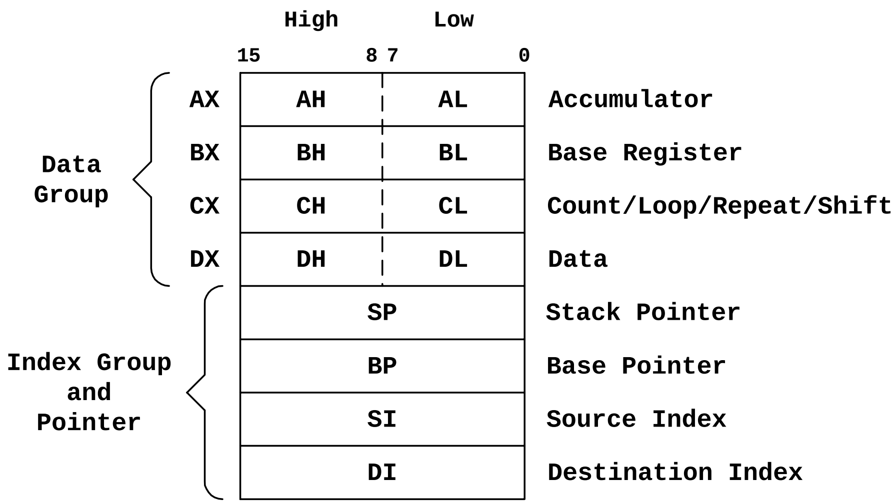
DX : Word Divide , Word Multiply, Indirect I/O operation

SP : Stack operations (POP, POPA, POPF, PUSH, PUSHA, PUSHF)

BP : General-purpose register which can be used to determine offset address of operands in Memory.

SI : String operations

DI : String operations



GENERAL REGISTERS

Segment Register

R8800 has four 16-bit segment registers, CS, DS, SS, ES. The segment registers contain the base addresses (starting location) of these memory segments, and they are immediately addressable for code (CS), data (DS & ES), and stack (SS) memory.

CS (Code Segment) : The CS register points to the current code segment, which contains instruction to be fetched. The default location memory space for all instruction is 64K. The initial value of CS register is 0FFFFh.

DS (Data Segment) : The DS register points to the current data segment, which generally contains program variables. The DS register initialize to 0000H.

SS (Stack Segment) : The SS register points to the current stack segment, which is for all stack operations, such as pushes and pops. The stack segment is used for temporary space. The SS register initialize to 0000H.

ES (Extra Segment) : The ES register points to the current extra segment which is typically for data storage, such as large string operations and large data structures. The DS register initialize to 0000H.

15 8 7 0	
CS	Code Segment
DS	Data Segment
SS	Stack Segment
ES	Extra Segment

SEGMENT REGISTERS

Instruction Pointer and Status Flags Register

IP (Instruction Pointer) : The IP is a 16-bit register and it contains the offset of the next instruction to be fetched. Software can not to direct access the IP register and this register is updated by the Bus Interface Unit. It can change, be saved or be restored as a result of program execution. The IP register initialize to 0000H and the CS:IP starting execution address is at 0FFFF0H.

Processor Status Flags Registers

FLAGS
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				OF	DF	IF	TF	SF	ZF	Res	AF	Res	PF	Res	CF

These flags reflect the status after the Execution Unit is executed.

Bit 15-12 : Reserved

Bit 11: OF, Overflow Flag. An arithmetic overflow has occurred, this flag will be set.

Bit 10 : DF, Direction Flag. If this flag is set, the string instructions are increment address process. If DF is cleared, the string instructions are decrement address process. Refer the STD and CLD instructions for how to set and clear the DF flag.

Bit 9 : IF, Interrupt-Enable Flag. Refer the STI and CLI instructions for how to set and clear the IF flag.

Set to 1 : The CPU enables the maskable interrupt request.

Set to 0 : The CPU disables the maskable interrupt request.

Bit 8: TF, Trace Flag. Set to enable single-step mode for debugging; Clear to disable the single-step mode. If an application program sets the TF flag using POPF or IRET instruction, a debug exception is generated after the instruction (The CPU automatically generates an interrupt after each instruction) that follows the POPF or IRET instruction.

Bit 7: SF, Sign Flag. If this flag is set, the high-order bit of the result of an operation is 1,indicating it is negative.

Bit 6: ZF, Zero Flag. The result of operation is zero, this flag is set.

Bit 5: Reserved

Bit 4: AF, Auxiliary Flag. If this flag is set, there has been a carry from the low nibble to the high or a borrow from the high nibble to the low nibble of the AL general-purpose register. Used in BCD operation.

Bit 3: Reserved.

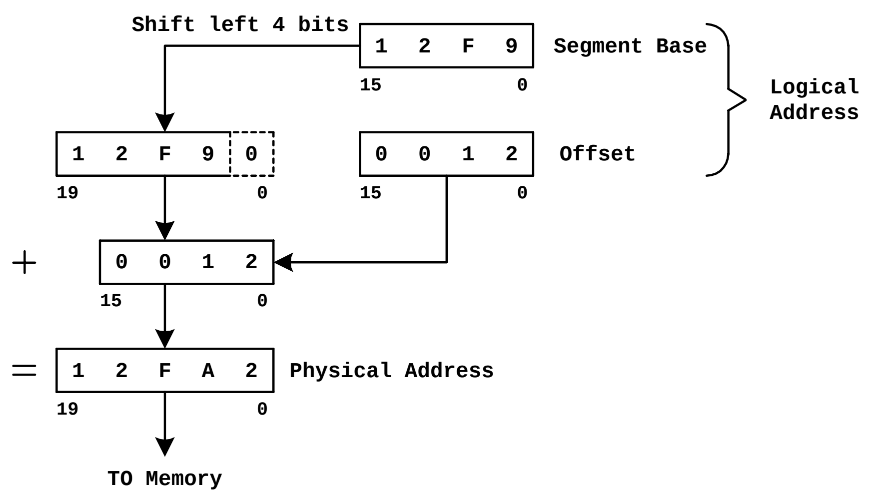
Bit 2: PF, Parity Flag. The result of low-order 8 bits operation has even parity, this flag is set.

Bit 1: Reserved

Bit 0: CF, Carry Flag. If CF is set, there has been a carry out or a borrow into the high-order bit of the instruction result.

Address generation

The Execution Unit generates a 20-bit physical address to Bus Interface Unit by the Address Generation. Memory is organized in sets of segments. Each segment contains a 16 bits value. Memory is addressed using a two-component address that consists of a 16-bit segment and 16-bit offset. The Physical Address Generation figure describes how the logical address transfers to the physical address.



Physical Address Generation

Peripheral Control Block Register

The peripheral control block can be mapped into either memory or I/O space which is to program the FEh register. And it starts at FF00h in I/O space when reset the microprocessor.

The following table is the definition of all the peripheral Control Block Register , and the detail description will arrange on the relation Block Unit.

Offset (HEX)	Register Name	Page	Offset (HEX)	Register Name	Page
FE	Peripheral Control Block Relocation Register	21	66	Timer 2 Mode / Control Register	61
F6	Reset Configuration Register	24	62	Timer 2 Maxcount Compare A Register	62
F4	Processor Release Level Register	21	60	Timer 2 Count Register	62
F0	PDCON Register	22	5E	Timer 1 Mode / Control Register	59
E4	Enable RCU Register	75	5C	Timer 1 Maxcount Compare B Register	61
E2	Clock Prescaler Register	75	5A	Timer 1 Maxcount Compare A Register	61
E0	Memory Partition Register	75	58	Timer 1 Count Register	61
DA	DMA 1 Control Register	53	56	Timer 0 Mode / Control Register	58
D8	DMA 1 Transfer Count Register	55	54	Timer 0 Maxcount Compare B Register	59
D6	DMA 1 Destination Address High Register	55	52	Timer 0 Maxcount Compare A Register	59
D4	DMA 1 Destination Address Low Register	56	50	Timer 0 Count Register	58
D2	DMA 1 Source Address High Register	56	44	Serial Port Interrupt Control Register	38
D0	DMA 1 Source Address Low Register	56	42	Watchdog Timer Control Register	62
CA	DMA 0 Control Register	52	40	INT4 Control Register	39
C8	DMA 0 Transfer Count Register	52	3E	INT3 Control Register	39
C6	DMA 0 Destination Address High Register	52	3C	INT2 Control Register	40
C4	DMA 0 Destination Address Low Register	53	3A	INT1 Control Register	40
C2	DMA 0 Source Address High Register	53	38	INT0 Control Register	41
C0	DMA 0 Source Address Low Register	53	36	DMA 1 Interrupt Control Register	42
A8	$\overline{\text{PCS}}$ and $\overline{\text{MCS}}$ Auxiliary Register	32	34	DMA 0 Interrupt Control Register	43
A6	Midrange Memory Chip Select Register	31	32	Timer Interrupt Control Register	43
A4	Peripheral Chip Select Register	33	30	Interrupt Status Register	44
A2	Low Memory Chip Select Register	30	2E	Interrupt Request Register	44
A0	Upper Memory Chip Select Register	29	2C	In-service Register	45
88	Serial Port Baud Rate Divisor Register	67	2A	Priority Mask Register	47
86	Serial Port Receive Register	66	28	Interrupt Mask Register	48
84	Serial Port Transmit Register	66	26	Poll Status Register	48
82	Serial Port Status Register	65	24	Poll Register	49
80	Serial Port Control Register	64	22	End-of-Interrupt	49
7A	PIO Data 1 Register	73	20	Interrupt Vector Register	50
78	PIO Direction 1 Register	73	18	Synchronous Serial Receive Register	69
76	PIO Mode 1 Register	73	16	Synchronous Serial Transmit 0 Register	69
74	PIO Data 0 Register	74	14	Synchronous Serial Transmit 1 Register	69
72	PIO Direction 0 Register	74	12	Synchronous Serial Enable Register	68
70	PIO Mode 0 Register	74	10	Synchronous Serial Status Register	68

Peripheral Control Block Relocation Register:

Offset : FEh
Reset Value : 20FFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	S/$\overline{M}$	Res	M/$\overline{IO}$	R19 - R8											

The peripheral control block is mapped into either memory or I/O space by programming this register. When the other chip selects ($\overline{PCSx}$ or $\overline{MCSx}$) are programmed to zero wait states and ignore the external ready, the $\overline{PCSx}$ or $\overline{MCSx}$ can overlap the control block.

Bit 15: Reserved

Bit 14: **S/$\overline{M}$** , Slave/Master – Configures the interrupt controller

set 0 : Master mode, **set 1:** Slaved mode

Bit 13 : Reserved

Bit 12: **M/$\overline{IO}$** , Memory/IO space. At reset, this bit is set to 0 and the PCB map start at FF00h in I/O space.

set 1- The peripheral control block (PCB) is located in memory space.

set 0- The PCB is located in I/O space.

Bit 11-0 : **R19-R8** , Relocation Address Bits

The upper address bits of the PCB base address. The lower eight bits default to 00h. When the PCB is mapped to I/O space, the R19-R16 must be programmed to 0000b.

Processor Release Level Register

Offset : F4h
Reset Value : −D9h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRL								1	1	0	1	1	0	0	1

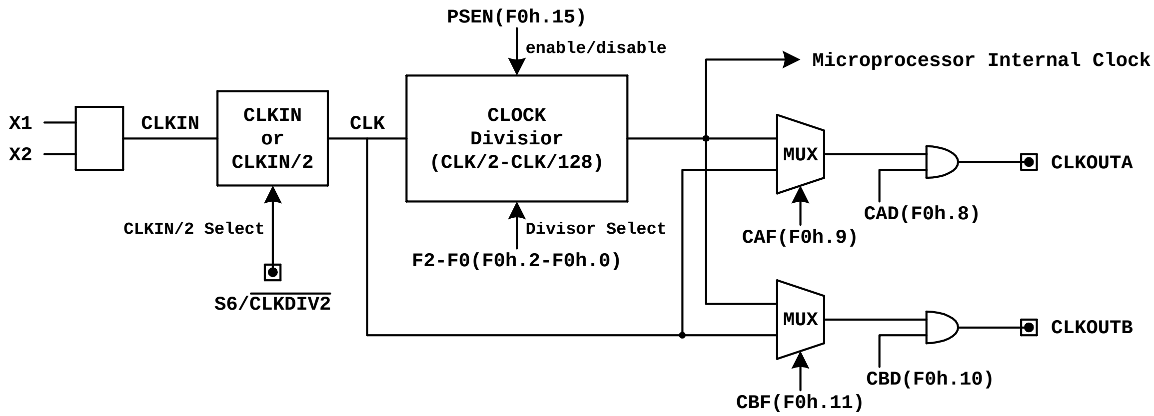
Read only register that specifies the processor release version and RDC identify number

Bit 15-8 : Processor version

01h : version A , 02h : version B, 03h : version C, 04h : version D

Bit 7-0 : RDC identify number - D9h

System Clock Block



System Clock

Power-Save Control Register

Offset : F0h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSEN	0	0	0	CBF	CBD	CAF	CAD	0	0	0	0	0	F2	F1	F0

Bit 15: **PSEN** , Enable Power-save Mode. This bit is cleared by hardware when an external interrupt occurs. This bit does not be changed when software interrupts (INT instruction) and exceptions occurs.

Set 1: enable power-save mode and divides the internal operating clock by the value in F2-F0.

Bit14-12: Reserved

Bit 11: **CBF**, CLKOUTB Output Frequency selection.

Set 1: CLKOUTB output frequency is same as crystal input frequency.

Set 0 : CLKOUTB output frequency is from the clock divisor, which frequency is same as that of microprocessor internal clock.

Bit 10 : CBD, CLKOUTB Drive Disable

Set 1: Disable the CLKOUTB. This pin will be three-state.

Set 0 : Enable the CLKOUTB.

Bit 9: CAF, CLKOUTA Output Frequency selection.

Set 1: CLKOUTA output frequency is same as crystal input frequency.

Set 0 : CLKOUTB output frequency is from the clock divisor, which frequency is same as that of microprocessor internal clock .

Bit 8: CAD, CLKOUTA Drive Disable.

Set 1: Disable the CLKOUTA. This pin will be three-state.

Set 0 : Enable the CLKOUTA.

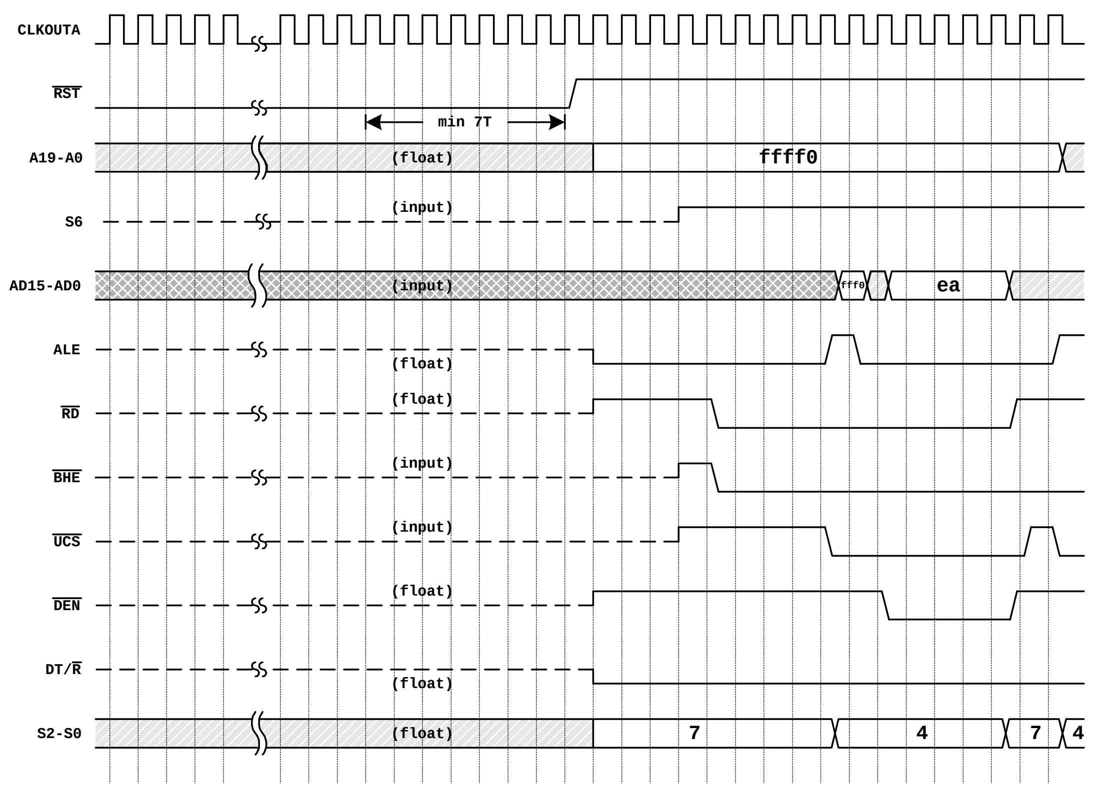
Bit 7-3 : Reserved

Bit 2-0: F2- F0, Clock Divisor Select.

F2,	**F1,**	**F0**	**-----**	**Divider Factor**
0,	0,	0	----	Divide by 1
0,	0,	1	----	Divide by 2
0,	1,	0	----	Divide by 4
0,	1,	1	----	Divide by 8
1,	0,	0	----	Divide by 16
1,	0,	1	----	Divide by 32
1,	1,	0	----	Divide by 64
1,	1,	1	----	Divide by 128

Reset

Processor initialization is accomplished with activation of the $\overline{RST}$ pin. To reset the processor, this pin should be held low for at least seven oscillator periods. The Reset Status Figure shows the status of the $\overline{RST}$ pin and others relation pins. When $\overline{RST}$ from low go high , the state of input pin (with weakly pull-up or pull-down) will be latched , and each pin will perform the individual function. The AD15-AD0 will be latched into the register F6h. $\overline{UCS}/\overline{ONCE1}$, $\overline{LCS}/\overline{ONCE0}$ will enter ONCE mode (All of the pins will floating except X1 , X2) when with pull-low resisters. The input clock will divide by 2 when S6/ $\overline{CLKDIV2}$ with pull-low resister. The AD15-AD0 bus will not drive the address phase during $\overline{UCS}$, $\overline{LCS}$ cycle if $\overline{BHE}/\overline{ADEN}$ with pull-low resister



Reset Status

Reset Configuration Register

Offset : F6h

Reset Value : AD15-AD0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RC															

Bit 15- 0 : **RC** ,Reset Configuration AD15 – AD0.

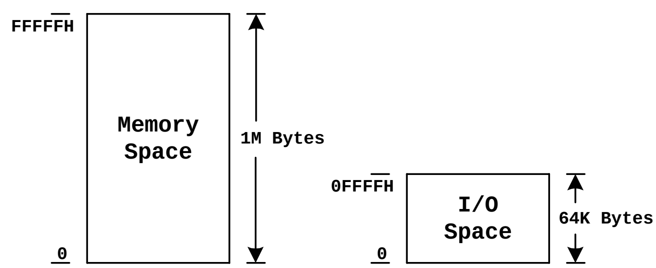
The AD15 to AD0 must with weakly pull-up or pull-down resistors to correspond the contents when AD15-AD0 be latched into this register during the $\overline{\text{RST}}$ pin from low go high. And the value of the reset configuration register provides the system information when software read this register. This register is read only and the contents remain valid until the next processor reset.

Bus Interface Unit

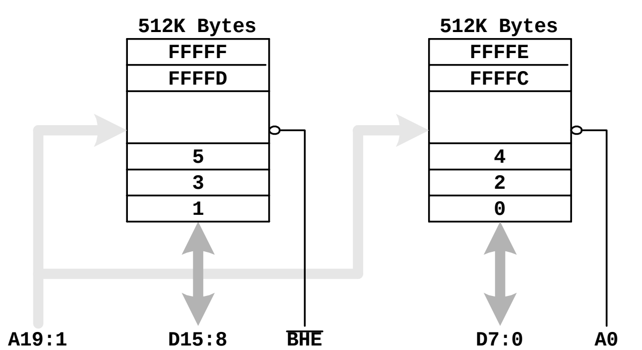
The bus interface unit drives address, data, status and control information to define a bus cycle. The bus A19-A0 are non-multiplex memory or I/O address. The AD15-AD0 are multiplexed address and data bus for memory or I/O accessing. The $\overline{S2}$ - $\overline{S1}$ are encoded to indicate the bus status, which is described in the Pin Description table in page 5. The Basic Application System Block (page 10) and Read/Write Timing Diagram (page 12) describe the basic bus operation.

Memory and I/O interface

The memory space consists of 1M bytes (512k 16-bit port) and the I/O space consists of 64k bytes (32k 16-bit port). Memory devices exchange information with the CPU during memory read, memory write and instruction fetch bus cycles. I/O read and I/O write bus cycles use a separate I/O address space. Only IN/OUT instruction can access I/O address space, and information must be transferred between the peripheral device and the AX register. The first 256 bytes of I/O space can be accessed directly by the I/O instructions. The entire 64k bytes I/O address space can be accessed indirectly, through the DX register. I/O instructions always force address A19-A16 to low level.



Memory and I/O Space

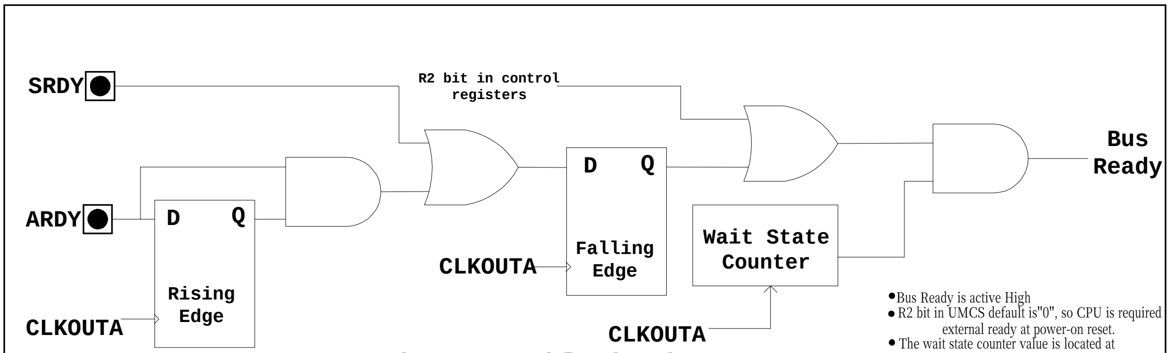


Physical Data Bus Models

Data Bus

The memory address space data bus is physically implemented by dividing the address space into two banks of up to 512k bytes. Each one bank connects to the lower half of the data bus and contains the even-addressed bytes (A0=0). The other bank connects to the upper half of the data bus and contains odd-addressed bytes (A0=1). A0 and BHE determine whether one bank or both banks participate in the data transfer.

Wait States



Wait-state block Diagram

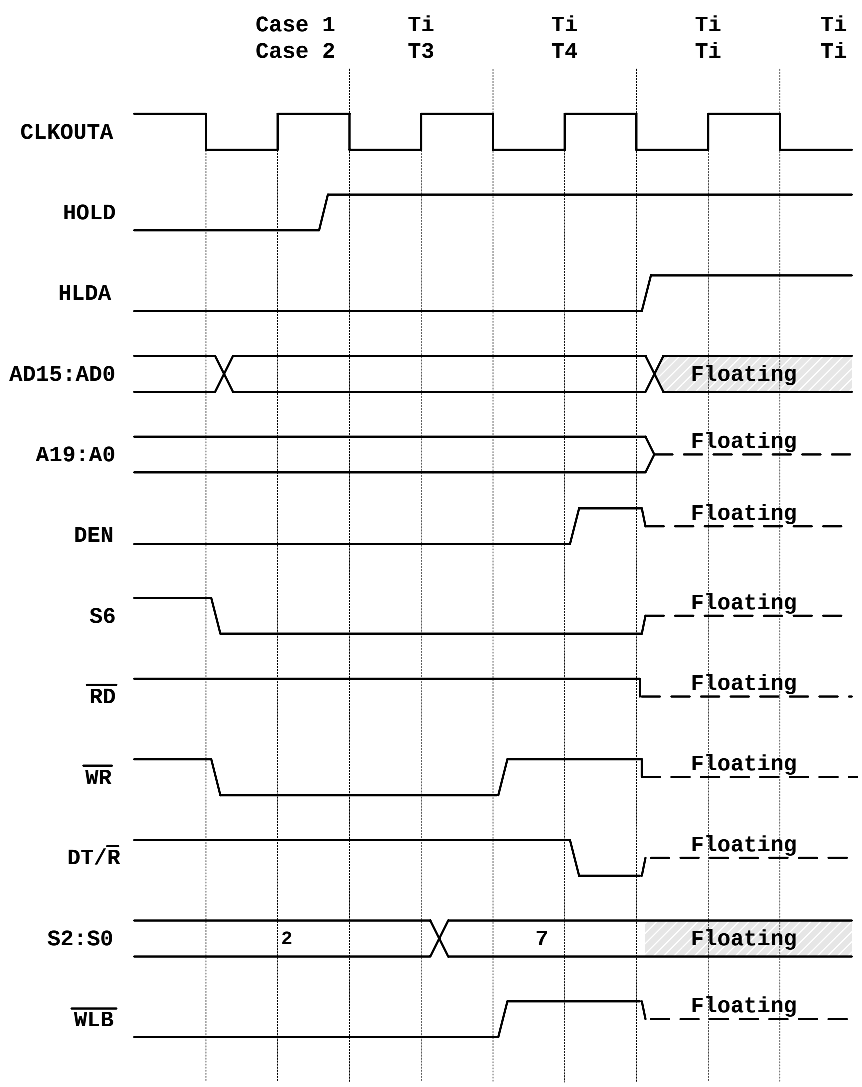
Wait states extend the data phase of the bus cycle. The ARDY or SRDY input with low level will insert wait states. If R2 bit=0, The user also can inserts wait state by programmed the internal chip select registers.

The R2 bit of UMCS (offset 0A0h) default is low, so each one of the ARDY or SRDY should in ready state (with pull high resistor) when at power on reset or external reset.

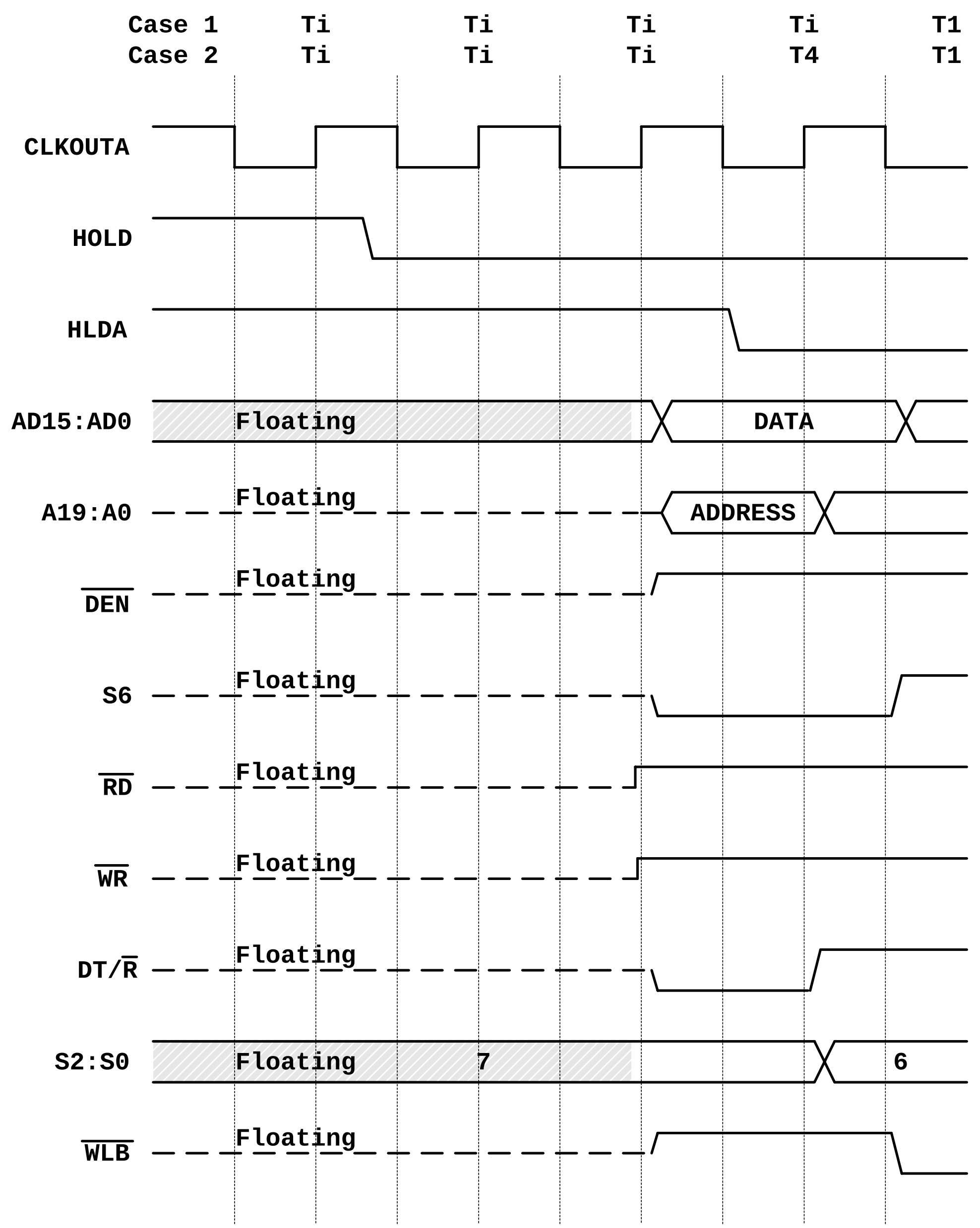
The wait state counter value is decided by the R3, R1,R0 bits in each chip select register. There are five group R3,R1,R0 bits in the registers offset A0h, A2h, A4h, A6h, A8h. Each group is independent.

Bus Hold

When the bus hold requested (HOLD pin active high) by the another bus master, the microprocessor will issue a HLDA in response to a HOLD request at the end of T4 or Ti. When the microprocessor is in hold status (HLDA is high), the AD15-AD0, A19-A0, $\overline{WR}$, $\overline{RD}$, $\overline{DEN}$, $\overline{S1}-\overline{S0}$, $\overline{S6}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{WHB}$ and $\overline{WLB}$ are floating, and the $\overline{UCS}$, $\overline{LCS}$, $\overline{PCS6}-\overline{PCS5}$, $\overline{MCS3}-\overline{MCS0}$ and $\overline{PCS3}-\overline{PCS0}$ will be drive high. After HOLD is detected as being low, the microprocessor will lower the HLDA.



BUS HOLD ENTER WAVEFORM



BUS HOLD LEAVE WAVEFORM

Chip Select Unit

The Chip Select Unit provides 12 programmable chip select pins to access a specific memory or peripheral device. The chip selects are programmed through five peripheral control registers (A0h, A2h, A4h, A6h, A8h). And all of the chip selects can be insert wait states by programmed the peripheral control register.

$\overline{\text{UCS}}$

The $\overline{\text{UCS}}$ default to active on reset for program code access. The memory active range is upper 512k (80000h – FFFFFh), which is programmable. And the default memory active range of $\overline{\text{UCS}}$ is 64k (F0000h – FFFFFh).
The $\overline{\text{UCS}}$ active to drive low four CLKOUTA oscillators if no wait state inserts. There are three wait-states insert to $\overline{\text{UCS}}$ active cycle on reset.

Upper Memory Chip Select Register

Offset : A0h
Reset Value :F03Bh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	LB2 - LB0			0	0	0	0	DA	0	1	1	1	R2	R1	R0

Bit 15 : Reserved

Bit 14-12 : LB2-LB0, Memory block size selection for $\overline{\text{UCS}}$ chip select pin.

The $\overline{\text{UCS}}$ chip select pin active region can be configured by the LB2-LB0.

The default memory block size is from F0000h to FFFFFh.

LB2, LB1, LB0	----	**Memory Block size**	**Start address**	**End Address**
1 , 1 , 1	----	64k	, F0000h	, FFFFFh
1 , 1 , 0	----	128k	, E0000h	, FFFFFh
1 , 0 , 0	----	256k	, C0000h	, FFFFFh
0 , 0 , 0	----	512k	, 80000h	, FFFFFh

Bit 11-8 : Reserved

Bit 7 : DA , Disable Address. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held high on the rising edge of $\overline{\text{RST}}$, then the DA bit is valid to enable/disable the address phase of the AD bus. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held low on the rising edge of $\overline{\text{RST}}$, the AD bus always drive the address and data.

Set 1 : Disable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{UCS}}$ is asserted.

Set 0 : Enable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{UCS}}$ is asserted.

Bit 6-3: Reserved

Bit 2 : R2, Ready Mode. This bit is used to configure the ready mode for $\overline{\text{UCS}}$ chip select.

Set 1: external ready is ignored.

Set 0: external ready is required.

Bit 1-0 : R1-R0, Wait-State value. When R2 is set to 0, it can inserted wait-state into an access to the $\overline{\text{UCS}}$ memory area.

(R1,R0) = (0,0) -- 0 wait-state ; (R1,R0) = (0,1) -- 1 wait-state

(R1,R0) = (1,0) -- 2 wait-state ; (R1,R0) = (1,1) -- 3 wait-state

---

$\overline{\text{LCS}}$

The lower 512k bytes (00000h-9FFFFh) memory region chip selects. The memory active range is programmable, which has no default size on reset. So the A2h register must be programmed first before to access the target memory range. The $\overline{\text{LCS}}$ pin is not active on reset, but any read or write access to the A2h register activates this pin.

Low Memory Chip Select Register

Offset : A2h

Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	UB2 - UB0			1	1	1	1	DA	PSE	1	1	1	R2	R1	R0

Bit 15: Reserved

Bit 14-12 : UB2-UB0, Memory block size selection for $\overline{\text{LCS}}$ chip select pin

The $\overline{\text{LCS}}$ chip select pin active region can be configured by the UB2-UB0.

The $\overline{\text{LCS}}$ pin is not active on reset, but any read or write access to the A2h (LMCS) register activates this pin.

UB2, UB1, UB0 ---- <u>Memory Block size</u> , <u>Start address</u>, <u>End Address</u>

UB2	UB1	UB0	Memory Block size	Start address	End Address
0	0	0	64k	00000h	0FFFFh
0	0	1	128k	00000h	1FFFFh
0	1	1	256k	00000h	3FFFFh
1	1	1	512k	00000h	7FFFFh

Bit 11-8 : Reserved

Bit 7 : DA , Disable Address. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held high on the rising edge of $\overline{\text{RST}}$, then the DA bit is valid to enable/disable the address phase of the AD bus. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held high on the rising edge of $\overline{\text{RST}}$, the AD bus always drive the address and data.

Set 1 : Disable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{LCS}}$ is asserted.

Set 0 : Enable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{LCS}}$ is asserted.

Bit 6 : PSE, PSRAM Mode Enable. This bit is used to enable PSRAM support for the $\overline{\text{LCS}}$ chip select memory space. The refresh control unit registers E0h,E2h,E4h must be configured for auto refresh before PSRAM support is enabled.

PSE set to 1: PSRAM support is enable

PSE set to 0: PSRAM support is disable

Bit 5-3: Reserved

Bit 2 : R2, Ready Mode. This bit is used to configure the ready mode for $\overline{\text{LCS}}$ chip select.

Set 1: external ready is ignored.

Set 0: external ready is required.

Bit 1-0 : R1-R0, Wait-State value. When R2 is set to 0, it can inserted wait-state into an access to the $\overline{\text{LCS}}$ memory area.

(R1,R0) = (0,0) -- 0 wait-state ; (R1,R0) = (0,1) -- 1 wait-state

(R1,R0) = (1,0) -- 2 wait-state ; (R1,R0) = (1,1) -- 3 wait-state

---

$\overline{\text{MCSx}}$

The memory block of $\overline{\text{MCS4}}$ - $\overline{\text{MCS0}}$ can be located anywhere within the 1M bytes memory space, exclusive of the areas associated with the $\overline{\text{UCS}}$ and $\overline{\text{LCS}}$ chip selects. The maximum $\overline{\text{MCSx}}$ active memory range is 512k bytes.

The MCS chip selects are programmed through two registers A6h and A8h, and these select pins are not active on reset. Both A6h and A8h registers must be accessed with a read or write to activate $\overline{\text{MCS4}}$ - $\overline{\text{MCS0}}$. There aren't default value on A6h and A8h registers, so the A6h and A8h must be programmed first before $\overline{\text{MCS4}}$ - $\overline{\text{MCS0}}$ active.

Midranage Memory Chip Select Register

Offset : A6h

Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA19 - BA13									1	1	1	1	R2	R1	R0

Bit 15-7 : BA19-BA13, Base Address. The BA19-BA13 correspond to bits 19-13 of the 1M bytes (20-bits) programmable base address of the $\overline{\text{MCS}}$ chip select block. The bits 12 to 0 of the base address are always 0.

The base address can be set to any integer multiple of the size of the memory block size selected in these bits. For example, if the midrange block is 32Kbytes, only the bits BA19 to BA15 can be programmed. So the block address could be locate at 20000h or 38000h but not in 22000h.

The base address of the $\overline{\text{MCS}}$ chip select can be set to 00000h only if the $\overline{\text{LCS}}$ chip select is not active. And the $\overline{\text{MCS}}$ chip select address range is not allowed to overlap the $\overline{\text{LCS}}$ chip select address range.

The $\overline{\text{MCS}}$ chip select address range also is not allowed to overlap the $\overline{\text{UCS}}$ chip select address range.

Bit 8-3 : Reserved

Bit 2: R2, Ready Mode. This bit is configured to enable/disable the wait states inserted for the $\overline{\text{MCS}}$ chip selects. The R1,R0 bits of this register determine the number of wait state to insert.

set to 1: external ready is ignored

set to 0: external ready is required

Bit 1-0 : R1-R0, Wait-State value. The R1,R0 determines the number of wait states inserted into a $\overline{\text{MCS}}$ access.

(R1,R0) : (1,1) – 3 wait states , (1,0) – 2 wait states, (0,1) – 1 wait states , (0,0) – 0 wait states

PCS and MCS Auxiliary Register

Offset : A8h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	M6 - M0							EX	MS	1	1	1	R2	R1	R0

Bit 15: Reserved

Bit 14-8: M6-M0, MCS Block Size. These bits determines the total block size for the MCS3 - MCS0 chip selects. Each individual chip select is active for one quarter of the total block size. For example, if the block size is 32K bytes and the base address is located at 20000h. The individual active memory address range of MCS3 to MCS0 is MCS0 – 20000h to 21FFF, MCS1 -22000 to 23FFFh, MCS2- 24000h to 25FFFh, MCS3- 26000h to 27FFFh. MCS total block size is defined by M6-M0,

M6-M0	**Total block size**	**MCSx address active range**
0000001b	8k	2k
0000010b	16k	4k
0000100b	32k	8k
0001000b	64k	16k
0010000b	128k	32k
0100000b	256k	64k
1000000b	512k	128k

Bit 7 : EX, Pin Selector. This bit configures the multiplex output which the PCS6 - PCS5 pins as chip selects or A2-A1.

Set 1 : PCS6 , PCS5 are configured as peripheral chip select pins.

Set 0: PCS6 is configured as address bit A2, PCS5 is configured as A1.

Bit 6: MS, Memory or I/O space Selector.

Set 1: The PCSx pins are active for memory bus cycle.

Set 0: The PCSx pins are active for I/O bus cycle.

Bit 5-3 : Reserved

Bit 2 : R2, Ready Mode. This bit is configured to enable/disable the wait states inserted for the PCS5,PCS6 chip selects. The R1,R0 bits of this register determine the number of wait state to insert.

set to 1: external ready is ignored

set to 0: external ready is required

Bit 1-0 : R1-R0, Wait-State value. The R1,R0 determines the number of wait states inserted into a PCS5 - PCS6 access.

(R1,R0) : (1,1) – 3 wait states , (1,0) – 2 wait states, (0,1) – 1 wait states , (0,0) – 0 wait states

PCSx

The peripheral or memory chip selects which are programmed through A4h and A8h register to define these pins.

The base address memory block can be located anywhere within the 1M bytes memory space, exclusive of the areas associated with the MCS4 , LCS and MCS chip elects. If the chip selects are mapped to I/O space, the access range is 64k bytes. PCS6 – PCS5 can be configured from 0 wait-state to 3 wait-states. PCS3 – PCS0 can be configured from 0 wait-state to 15 wait-states.

Peripheral Chip Select Register

Offset : A4h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA19 - BA11									1	1	1	R3	R2	R1	R0

Bit 15-7 : BA19-BA11, Base Address. BA19-BA11 correspond to bit 19-11 of the 1M bytes (20-bits) programmable base address of the PCS chip select block.

When the PCS chip selects are mapped to I/O space, BA19-BA16 must be wrote to 0000b because the I/O address bus in only 64K bytes (16-bits) wide.

PCSx address range:

PCS0	:	Base Address	-	Base Address + FFh
PCS1	:	Base Address + 100h	-	Base Address + 1FFh
PCS2	:	Base Address + 200h	-	Base Address + 2FFh
PCS3	:	Base Address + 300h	-	Base Address + 3FFh
PCS5	:	Base Address + 500h	-	Base Address + 5FFh
PCS6	:	Base Address + 600h	-	Base Address + 6FFh

Bit 6-4: Reserved

Bit 3: R3; **Bit 1-0: R1,R0** ,Wait-State Value. The R3,R1,R0 determines the number of wait-states inserted into a PCS3 - PCS0 access.

R3,	**R1,**	**R0**	**--**	**Wait States**
0,	0,	0	--	0
0,	0,	1	--	1
0,	1,	0	--	2
0,	1,	1	--	3
1,	0,	0	--	5
1,	0,	1	--	7
1,	1,	0	--	9
1,	1,	1	--	15

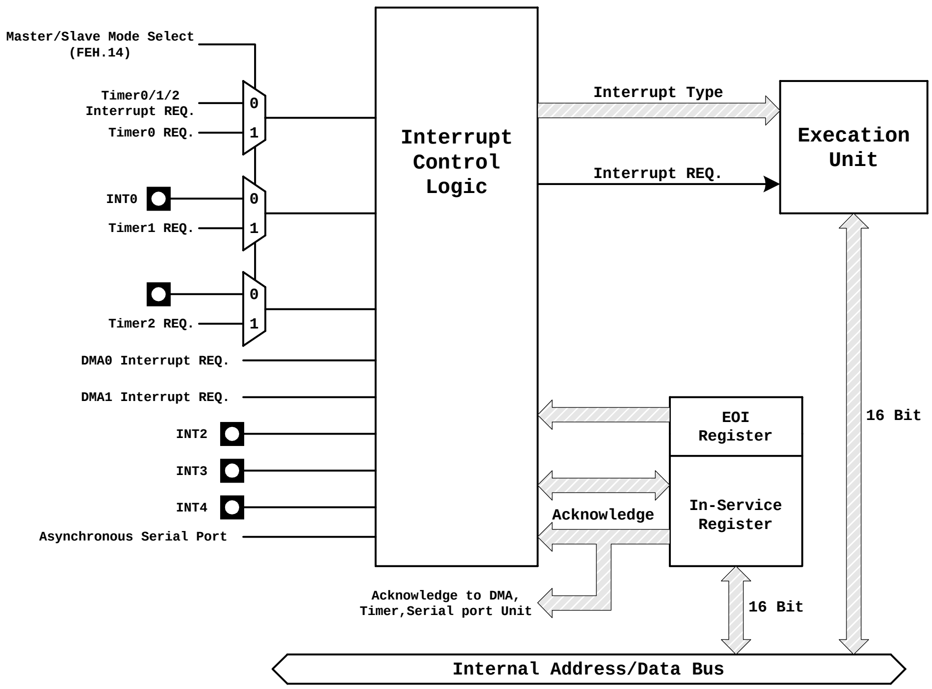
Bit 2 : **R2**, Ready Mode. This bit is configured to enable/disable the wait states inserted for the PCS3 - PCS0 chip selects. The R3,R1,R0 bits determine the number of wait state to insert.

set to 1: external ready is ignored

set to 0: external ready is required

Interrupt Controller Unit

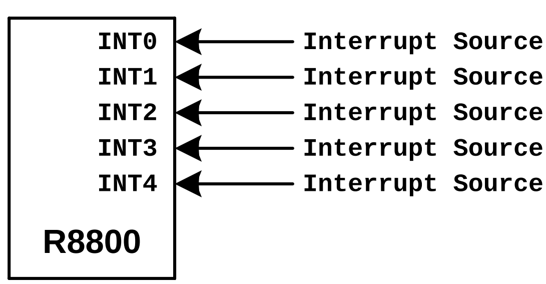
There are twelve interrupt requests source connect to the controller: five maskable interrupt pins (INT0 – INT4); one non-maskable interrupt pin (NMI) ; Six internal unit request source (Timer 0, 1,2 ;DMA 0,1 ; Asynchronous serial unit).



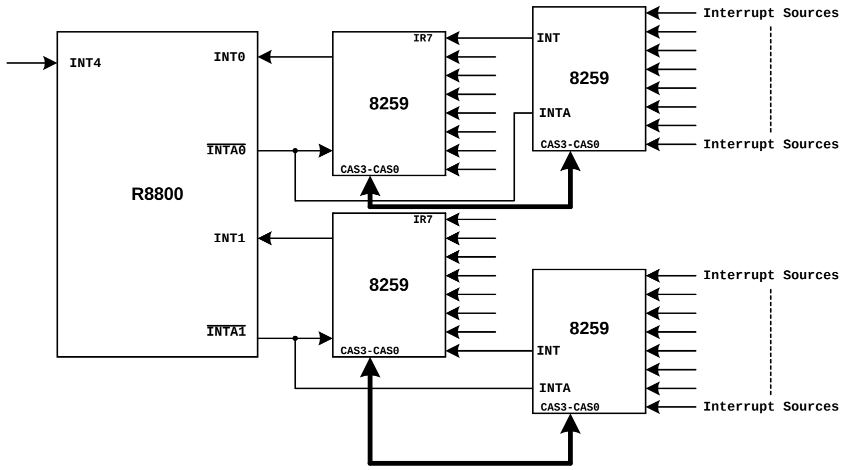
Interrupt Control Unit Block Diagram

Master Mode and Slave Mode

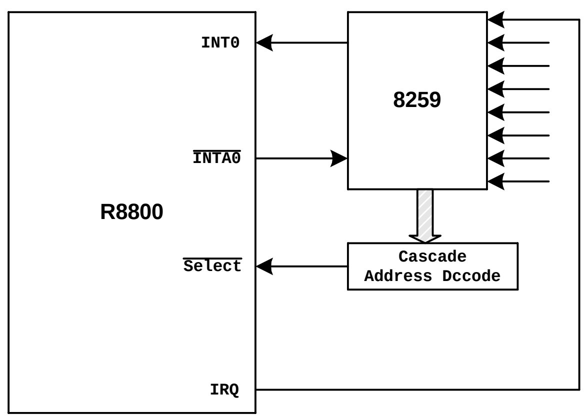
The interrupt controller can be programmed as a master or slave mode. (program FEh , bit 14). The master mode has two connections : Fully Nested Mode connection or Cascade Mode connection.



Fully Nested Mode Connections



Cascade Mode Connection



Slave Mode Connection

Interrupt Vector, Type and Priority

The following table shows the interrupt vector addresses, type and the priority. The maskable interrupt priority can be changed by programmed the priority register. The Vector addresses for each interrupt are fixed.

Interrupt source	Interrupt Type	Vector Address	EOI Type	Priority	Note
Divide Error Exception	00h	00h		1	
Trace interrupt	01h	04h		1-1	*
NMI	02h	08h		1-2	*
Breakpoint Interrupt	03h	0Ch		1	
INTO Detected Over Flow Exception	04h	10h		1	
Array Bounds Exception	05h	14h		1	

Undefined Opcode Exception	06h	18h		1	
ESC Opcode Exception	07h	1Ch		1	
Timer 0	08h	20h	08	2-1	*/**
Reserved	09h				
DMA 0	0Ah	28h	0A	3	**
DMA 1	0Bh	2Ch	0B	4	**
INT0	0Ch	30h	0C	5	
INT1	0Dh	34h	0D	6	
INT2	0Eh	38h	0E	7	
INT3	0Fh	3Ch	0F	8	
INT4	10h	40h	10	9	
Watchdog Timer	11h	44h	11	9	
Timer 1	12h	48h	08	2-2	*/**
Timer 2	13h	4Ch	08	2-3	*/**
Asynchronous Serial port	14h	50h	14	9	
Reserved	15h-1Fh				

Note * : When the interrupt occurs in the same time, the priority is (1-1 > 1-2) ; (2-1> 2-2 > 2-3)

Note **: The interrupt types of these sources are programmable in slave mode.

Interrupt Request

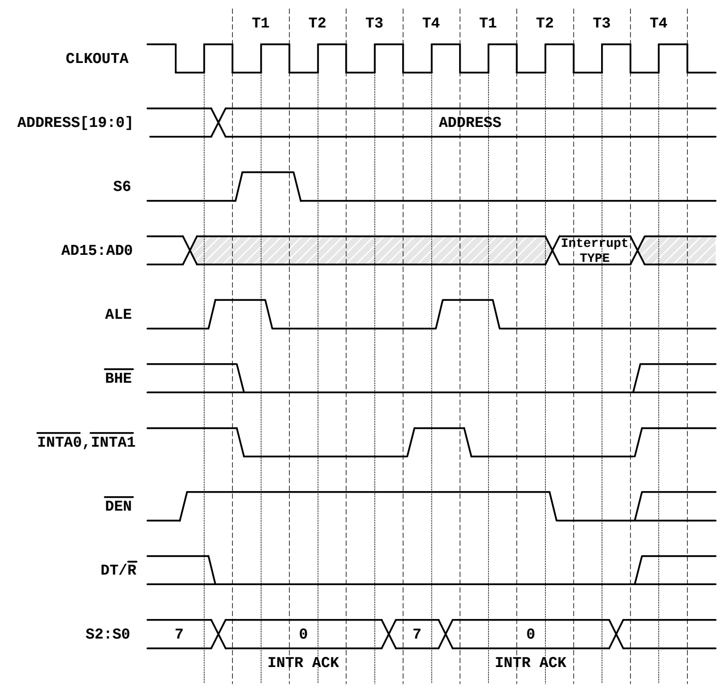
When an interrupt is request, the internal interrupt controller verifies the interrupt is enable (The IF flag is enable, no MSK bit set) and that there are no higher priority interrupt requests being serviced or pending. If the interrupt is granted , the interrupt controller uses the interrupt type to access a vector from the interrupt vector table.

If the external INT is active (level-trigger) to request the interrupt controller service, and the INT pins must hold till the microcontroller enter the interrupt service routine. There is no interrupt-acknowledge output when running in fully nested mode, so it should use PIO pin to simulate the interrupt-acknowledge pin if necessary.

Interrupt Acknowledge

The processor requires the interrupt type as an index into the interrupt table. The internal interrupt can provide the interrupt type or an external controller can provide the interrupt type.

The internal interrupt controller provides the interrupt type to processor without external bus cycles generation. When an external interrupt controller is supplying the interrupt type, the processor generates two acknowledge bus cycles, and the interrupt type is written to the AD7-AD0 lines by the external interrupt controller.



INTERRUPT ACKNOWLEDGE CYCLE
(CASECADE OR SLAVE MODE)

Programming the Registers

Software is programmed through the registers (**Master mode:** 44h, 42h, 40h, 3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 26h, 24h, 22h; **Slave Mode:** 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h,22h, 20h) to define the interrupt controller operation.

Serial Port Interrupt Control Register

Offset : 44h

Reset Value : 001Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											1	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4 : Reserved

Bit 3: MSK, Mask.

Set 1: Mask the interrupt source of the asynchronous serial port.

Set 0: Enable the serial port interrupt.

Bit 2-0 : PR2-PR0, Priority. These bits determine the priority of the serial port relative to the other interrupt signals.

The priority selection:

PR2, **PR1**, **PR0** -- **Priority**

0 , 0 , 0 -- 0 (High)

0 , 0 , 1 -- 1

0 , 1 , 0 -- 2

0 , 1 , 1 -- 3

1 , 0 , 0 -- 4

1 , 0 , 1 -- 5

1 , 1 , 0 -- 6

1 , 1 , 1 -- 7 (Low)

INT4 Control Register

Offset : 40h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Res		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15- 8, bit 6-5 : Reserved

Bit 7 : ETM, Edge trigger mode enable. When this bit set to 1 and Bit 4 set to 0, the Interrupt is triggered by low go high edge. The low go high edge will be latched (one level) till this interrupt is been serviced.

Bit 4: LTM, Level-Triggered Mode.

Set 1: Interrupt is triggered by high active level

Set 0 : Interrupt is triggered by low go high edge.

Bit 3 : MSK, Mask.

Set 1: Mask the interrupt source of the INT4

Set 0: Enable the INT4 interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of 42h

---

INT3 Control Register

Offset : 3Eh
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Res		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15- 8, bit 6-5 : Reserved

Bit 7:ETM, Edge trigger mode enable. When this bit set to 1 and Bit 4 set to 0, the Interrupt is triggered by low go high edge The low go high edge will be latched (one level) till this interrupt is been serviced.

Bit 4: LTM, Level-Triggered Mode.

Set 1: Interrupt is triggered by high active level

Set 0 : Interrupt is triggered by low go high edge.

Bit 3 : MSK, Mask.

Set 1: Mask the interrupt source of the INT3

Set 0: Enable the INT3 interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of 42h

---

INT2 Control Register

Offset : 3Ch
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Res		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-8, bit 6- 5 : Reserved

Bit 7 : ETM, Edge trigger mode enable. When this bit set to 1 and Bit 4 set to 0, the Interrupt is triggered by low go high edge. The low go high edge will be latched (one level) till this interrupt is been serviced.

Bit 4: LTM, Level-Triggered Mode.

Set 1: Interrupt is triggered by high active level

Set 0 : Interrupt is triggered by low go high edge.

Bit 3 : MSK, Mask.

Set 1: Mask the interrupt source of the INT2

Set 0: Enable the INT2 interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of the register 44h

---

INT1 Control Register

Offset : 3Ah
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	C	LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-8 : Reserved

Bit 7 : ETM, Edge trigger mode enable. When this bit set to 1 and Bit 4 set to 0, the Interrupt is triggered by low go high edge. The low go high edge will be latched (one level) till this interrupt is been serviced.

Bit 6: SFNM, Special Fully Nested Mode.

Set 1: Enable the special fully nested mode of INT1

Bit 5: C, Cascade Mode, Set this bit to 1 to enable cascade mode.

Bit 4: LTM, Level-Triggered Mode.

Set 1: Interrupt is triggered by high active level

Set 0 : Interrupt is triggered by low go high edge.

Bit 3 : MSK, Mask.

Set 1: Mask the interrupt source of the INT1

Set 0: Enable the INT1 interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of the register 44h

(Slave Mode), Timer 2 interrupt control register , reset value is 0000h

Bit 15- 4 : Reserved

Bit 3 : MSK, Mask.

Set 1: Mask the interrupt source of the Timer 2

Set 0: Enable the Timer 2 interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of the register 44h

---

INT0 Control Register

Offset : 38h

Reset Value : 000Fh

15-8	7	6	5	4	3	2	1	0
Reserved	ETM	SFNM	C	LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-8 : Reserved

Bit 7 : ETM, Edge trigger mode enable. When this bit set to 1 and Bit 4 set to 0, the Interrupt is triggered by low go high edge. The low go high edge will be latched (one level) till this interrupt is been serviced.

Bit 6: SFNM, Special Fully Nested Mode.

Set 1: Enable the special fully nested mode of INT0.

Bit 5: C, Cascade Mode, Set this bit to 1 to enable cascade mode.

Bit 4: LTM, Level-Triggered Mode.

Set 1: Interrupt is triggered by high active level

Set 0 : Interrupt is triggered by low go high edge.

Bit 3 : MSK, Mask.

Set 1: Mask the interrupt source of the INT0

Set 0: Enable the INT0 interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of the register 44h

(Slave Mode), Timer 1 interrupt control register , reset value is 0000h

Bit 15-4 : Reserved

Bit 3: MSK , Mask.

Set 1: Mask the interrupt source of the timer 1

Set 0: Enable the timer 1 interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of the register 44h

---

DMA 1 Interrupt Control Register

Offset : 36h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4 : Reserved

Bit 3: MSK , Mask.

Set 1: Mask the interrupt source of the DMA 1 controller

Set 0: Enable the DMA 1 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of the register 44h

(Slave Mode), DMA 1 interrupt control register , reset value is 0000h

Bit 15-4 : Reserved

Bit 3: MSK , Mask.

Set 1: Mask the interrupt source of the DMA 1 controller

Set 0: Enable the DMA 1 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of the register 44h

---

DMA 0 Interrupt Control Register

Offset : 34h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4 : Reserved

Bit 3: MSK , Mask.

Set 1: Mask the interrupt source of the DMA 0 controller

Set 0: Enable the DMA 0 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of the register 44h

(Slave Mode), reset value is 0000h

Bit 15-4 : Reserved

Bit 3: MSK , Mask.

Set 1: Mask the interrupt source of the DMA 0 controller

Set 0: Enable the DMA 0 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of the register 44h

---

Timer Interrupt Control Register

Offset : 32h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4 : Reserved

Bit 3: MSK , Mask.

Set 1: Mask the interrupt source of the Timer controller

Set 0: Enable the Timer controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of the register 44h

(Slave Mode), Timer 0 interrupt control register , reset value is 0000h

Bit 15-4 : Reserved

Bit 3: MSK , Mask.

Set 1: Mask the interrupt source of the Timer 0 controller

Set 0: Enable the Timer 0 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bits setting for priority selection is same as bit 2-0 of the register 44h

---

Interrupt Status Register

Offset : 30h

Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DHLT	Reserved												TMR2	TMR1	TMR0

(Master Mode), Reset value undifine

Bit 15 : DHLT, DMA Halt.

Set 1: halts any DMA activity. When non-maskable interrupts occur.

Set 0: When an IRET instruction is excuted.

Bit 14-3 : Reserved.

Bit 2-0 : TMR2-TMR0,

Set 1: indicates the corresponding timer has an interrupt request pending.

(Slave Mode), Reset value is 0000h

Bit 15 : DHLT, DMA Halt.

Set 1: halts any DMA activity. When non-maskable interrupts occur.

Set 0: When an IRET instruction is executed.

Bit 14-3 : Reserved.

Bit 2-0 : TMR2-TMR0,

Set 1: indicates the corresponding timer has an interrupt request pending.

Interrupt Request Register

Offset : 2Eh

Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SPI	WD	I4	I3	I2	I1	I0	D1	D0	Res	TMR

(Master Mode)

The Interrupt Request register is a read-only register. For internal interrupts (SPI, WD, D1, D0, and TMR), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge. For INT4-INT0 external interrupts, the corresponding bit (I4-I0) reflects the current value of the external signal.

Bit 15-11 : Reserved.

Bit 10 : SPI, Serial Port Interrupt Request. Indicates the interrupt state of the serial port.

Bit 9 : WD, Watchdog Timer Interrupt Request.

Set 1: The Watchdog Timer has an interrupt pending.

Bit 8-4 : I4-I0, Interrupt Requests.

Set 1: The corresponding INT pin has an interrupt pending.

Bit 3-2 : D1-D0, DMA Channel Interrupt Request.

Set 1: The corresponding DMA channel has an interrupt pending.

Bit 1: Reserved.

Bit 0 : TMR, Timer Interrupt Request.

Set 1: The timer control unit has an interrupt pending.

Interrupt In - Service Register

Offset : 2Ch

Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SPI	WD	I4	I3	I2	I1	I0	D1	D0	Res	TMR

(Slave Mode)

The Interrupt Request register is a read-only register. For internal interrupts (D1, D0, TMR2, TMR1, and TMR0), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge.

Bit 15-6 : Reserved.

Bit 5-4 : TMR2/TMR1, Timer2/Timer1 Interrupt Request.

Set 1: Indicates the state of any interrupt requests form the associated timer.

Bit 3-2 : D1-D0, DMA Channel Interrupt Request.

Set 1: Indicates the corresponding DMA channel has an interrupt pending.

Bit 1 : Reserved.

Bit 0 : TMR0, Timer 0 Interrupt Request.

Set 1: Indicates the state of an interrupt request from Timer 0.

In - Service Register

Offset : 2Ch
Reset Value : 0000h

15-11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SPI	WD	I4	I3	I2	I1	I0	D1	D0	Res	TMR

(Master Mode)

The bits in the INSERV register are set by the interrupt controller when the interrupt is taken. Each bit in the register is cleared by writing the corresponding interrupt type to the EOI register.

Bit 15-11 : Reserved.

Bit 10 : SPI, Serial Port Interrupt In-Service.

Set 1: the serial port interrupt is currently being serviced.

Bit 9 : WD, Watchdog Timer Interrupt In-Service.

Set 1: the watchdog timer interrupt is currently being serviced.

Bit 8-4 : I4-I0, Interrupt In-Service.

Set 1: the corresponding INT interrupt is currently being serviced.

Bit 3-2 : D1-D0, DMA Channel Interrupt In-Service.

Set 1: the corresponding DMA channel interrupt is currently being serviced.

Bit 1 : Reserved.

Bit 0 : TMR, Timer Interrupt In-Service.

Set 1: the timer interrupt is currently being serviced.

In - Service Register

Offset : 2Ch
Reset Value : 0000h

15-11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SPI	WD	I4	I3	I2	I1	I0	D1	D0	Res	TMR

(Slave Mode)

The bits in the In-Service register are set by the interrupt controller when the interrupt is taken. The in-service bits are cleared by writing to the EOI register.

Bit 15-6 : Reserved.

Bit 5-4 : TMR2-TMR1, Timer2/Timer1 Interrupt In-Service.

Set 1: the corresponding timer interrupt is currently being serviced.

Bit 3-2 : D1-D0, DMA Channel Interrupt In-Service.

Set 1: the corresponding DMA Channel is currently being serviced.

Bit 1 : Reserved.

Bit 0 : TMR0, Timer 0 Interrupt In-Service.

Set 1: the Timer 0 interrupt is currently being serviced.

Priority Mask Register

Offset : 2Ah
Reset Value : 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRM2	PRM1	PRM0

(Master Mode)

Determining the minimum priority level at which maskable interrupts can generate an interrupt.

Bit 15-3 : Reserved.

Bit 2-0 : PRM2-PRM0, Priority Field Mask. Determining the minimum priority that is required in order for a maskable interrupt source to generate an interrupt.

Priority	PR2-PR0
(High) 0	000
1	001
2	010
3	011
4	100
5	101
6	110
(Low) 7	111

(Slave Mode)

Determining the minimum priority level at which maskable interrupts can generate an interrupt.

Bit 15-3 : Reserved.

Bit 2-0 : PRM2-PRM0, Priority Field Mask. Determining the minimum priority that is required in order for a maskable interrupt source to generate an interrupt.

Priority	PR2-PR0
(High) 0	000
1	001
2	010
3	011
4	100
5	101
6	110
(Low) 7	111

Interrupt Mask Register

Offset : 28h
Reset Value : 07FDh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SPI	WD	I4	I3	I2	I1	I0	D1	D0	Res	TMR

(Master Mode)

Bit 15-11 : Reserved.

Bit 10 : SPI, Serial Port Interrupt Mask. The state of the mask bit of the asynchronous serial port interrupt.

Bit 9 : WD, Virtual Watchdog Timer Interrupt Mask. The state of the mask bit of the Watchdog Timer interrupt.

Bit 8-4 : I4-I0, Interrupt Masks. Indicates the state of the mask bit of the corresponding interrupt.

Bit 3-2 : D1-D0, DMA Channel Interrupt Masks. Indicates the state of the mask bit of the corresponding DMA Channel interrupt.

Bit 1: Reserved.

Bit 0 : TMR, Timer Interrupt Mask. The state of the mask bit of the timer control unit .

Interrupt Request Register

Offset : 28h
Reset Value : 003Dh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMR2	TMR1	D1	D0	Res	TMR0

(Slave Mode)

Bit 15-6 : Reserved.

Bit 5-4 : TMR2-TMR1, Timer 2/Timer1 Interrupt Mask. The state of the mask bit of the Timer Interrupt Control register.

Set 1: Timer2 or Time1 has its interrupt requests masked

Bit 3-2 : D1-D0, DMA Channel Interrupt Mask. The state of the mask bits of the corresponding DMA control register.

Bit 1 : Reserved.

Bit 0 : TMR0, Timer 0 Interrupt Mask. The state of the mask bit of the Timer Interrupt Control Register

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Poll Status Register

Offset : 26h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S4 - S0				

(Master mode)

The Poll Status (POLLST) register mirrors the current state of the Poll register. the POLLST register can be read without affecting the current interrupt request.

Bit 15 : IREQ, Interrupt Request.

Set 1: if an interrupt is pending. The S4-S0 field contains valid data.

Bit 14-5 : Reserved.

Bit 4-0 : S4-S0, Poll Status. Indicates the interrupt type of the highest priority pending interrupt.

Poll Register

Offset : 24h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S4 - S0				

(Master mode)

When the Poll register is read, the current interrupt is acknowledged and the next interrupt takes its place in the Poll register.

Bit 15 : IREQ, Interrupt Request.

Set 1: if an interrupt is pending. The S4-S0 field contains valid data.

Bit 14-5 : Reserved.

Bit 4-0 : S4-S0, Poll Status. Indicates the interrupt type of the highest priority pending interrupt.

End - Of - Interrupt

Offset : 22h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NSPEC											S4 - S0				

(Master Mode)

Bit 15 : NSPEC, Non-Specific EOI.

Set 1: indicates non-specific EOI.

Set 0: indicates the specific EOI interrupt type in S4-S0.

Bit 14-5 : Reserved.

Bit 4-0: S4-S0, Source EOI Type. Specifies the EOI type of the interrupt that is currently being processed.

Specific EOI

Offset : 22h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	L2	L1	L0

(Slave Mode)

Bit 15-3 : Reserved.

Bit 2-0 : L2-L0, Interrupt Type. Encoded value indicating the priority of the IS(interrupt service) bit to reset. Writes to these bits cause an EOI to be issued for the interrupt type in slave mode.

Interrupt Vector Register

Offset : 20h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	T4 - T0					0	0	0

(Slave Mode)

Bit 15-8 : Reserved

Bit 7-3 : T4-T0, Interrupt Type.

The following interrupt type of slave mode can be programmed.

Timer 2 interrupt controller : (T4,T3,T2,T1,T0, 1, 0, 1)b

Timer 1 interrupt controller : (T4,T3,T2,T1,T0, 1, 0, 0)b

DMA 1 interrupt controller : (T4,T3,T2,T1,T0, 0, 1, 1)b

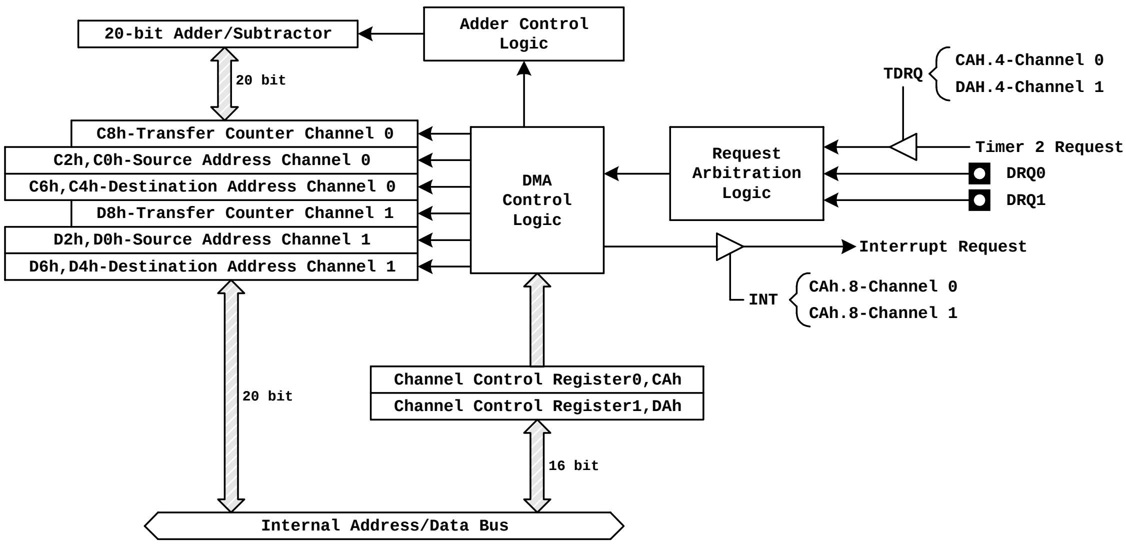
DMA 0 interrupt controller : (T4,T3,T2,T1,T0, 0, 1, 0)b

Timer 0 interrupt controller : (T4,T3,T2,T1,T0, 0, 0, 0)b

Bit 2-0 : Reserved

DMA Unit

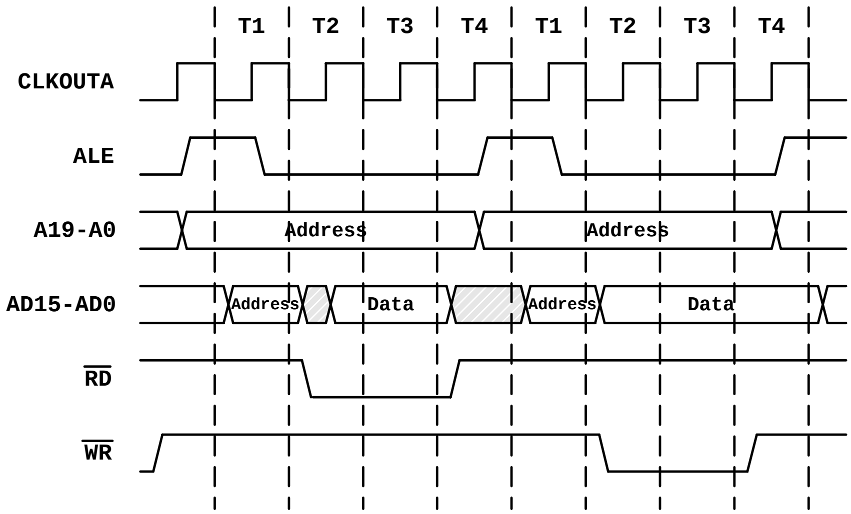
The DMA controller provides the data transfer between the memory and peripherals without the intervention of the CPU. There are two DMA channels in the DMA unit. Each channel can accept DMA request from one of two source : external pin (DRQ0 for channel 0 or DRQ1 for channel 1) or Timer 2 overflow. The data transfer from source to destination can be memory to memory or memory, to I/O, or I/O to I/O, or I/O to memory. Either bytes or words can be transferred to or from even or odd addresses and two bus cycles are necessary (read from source and write to destination) for each data transfer.



DMA Unit Block

DMA Operation

Every DMA transfer consists of two bus cycles (figure of Typical DMA Transfer) and the two bus cycles can not be separated by a bus hold request, a refresh request or another DMA request. The registers (CAh, C8h, C6h, C4h, C2h, C0h, DAh, D8h, D6h, D4h, D2h, D0h) are used to configure and operate the two DMA channels.



Typical DMA Trarsfer

DMA Control Registers

Offset : CAh (DMA0)
Reset Value : FFF9h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{DM}/\overline{IO}$	DDEC	DINC	SM/$\overline{IO}$	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	Res	CHG	ST	$\overline{B}$/W

The definition of Bits 15-0 for DMA0 are same as the Bits 15-0 of register DAh for DMA1.

DMA Transfer Count Register

Offset : C8h (DMA0)
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

Bit 15-0: TC15-TC0, DMA 0 transfer Count. The value of this register is decremented by 1 after each transfer.

DMA Destination Address High Register

Offset : C6h (DMA0)
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DDA19 - DDA16			

Bit 15-4: Reserved

Bit 3-0: DDA19-DDA16, High DMA 0 Destination Address. These bits are map to A19- A16 during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

DMA Destination Address Low Register

Offset : C4h (DMA0)
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDA15 - DDA0															

Bit 15-0: DDA15-DDA0, Low DMA 0 Destination Address. These bits are mapped to A15- A0 during a DMA transfer. The value of (DDA19-DDA0)b will increment or decrement by 2 after each DMA transfer.

DMA Source Address High Register

Offset : C2h (DMA0)
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												DSA19 - DSA16			

Bit 15-4: Reserved

Bit 3-0: DSA19-DSA16, High DMA 0 Source Address. These bits are mapped to A19- A16 during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

DMA Source Address Low Register

Offset : C0h (DMA0)
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSA15 - DSA0															

Bit 15-0: DSA15-DSA0, Low DMA 0 Source Address. These bits are mapped to A15- A0 during a DMA transfer. The value of (DSA19-DSA0)b will increment or decrement by 2 after each DMA transfer.

DMA Control Registers

Offset : DAh (DMA1)
Reset Value : FFF9h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{DM}/\overline{IO}$	DDEC	DINC	SM/$\overline{IO}$	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	Res	CHG	ST	$\overline{B}$/W

Bit 15: $\overline{\text{DM}}$ **/** $\overline{\text{IO}}$, Destination Address Space Select.

Set 1: The destination address is in memory space.

Set 0: The destination address is in I/O space.

Bit 14: DDEC, Destination Decrement.

Set 1: The destination address is automatically decrement after each transfer.

The $\overline{\text{B}}$/W (bit 0) bit determines the decrement value which is by 1 or 2 When both DDEC and DINC bits are set to 1, the address remains constant

Set 0 : Disable the decrement function.

Bit 13: DINC, Destination Increment.

Set 1: The destination address is automatically increment after each transfer.

The $\overline{\text{B}}$/W (bit 0) bit determines the increment value which is by 1 or 2

Set 0 : Disable the decrement function.

Bit 12: SM/ $\overline{\text{IO}}$, Source Address Space Select.

Set 1: The Source address is in memory space.

Set 0: The Source address is in I/O space

Bit 11: SDEC, Source Decrement.

Set 1: The Source address is automatically decrement after each transfer.

The $\overline{\text{B}}$/W (bit 0) bit determines the decrement value which is by 1 or 2 When both SDEC and SINC bits are set to 1, the address remains constant

Set 0 : Disable the decrement function.

Bit 10: SINC, Source Increment.

Set 1: The Source address is automatically increment after each transfer.

The $\overline{\text{B}}$/W (bit 0) bit determines the increment value which is by 1 or 2

Set 0 : Disable the decrement function

Bit 9 : TC, Terminal Count.

Set 1: The synchronized DMA transfer is terminated when the DMA transfer count register reaches 0.

Set 0: The synchronized DMA transfer is terminated when the DMA transfer count register reaches 0.

Unsynchronized DMA transfer is always terminated when the DMA transfer count register reaches 0, regardless the setting of this bit.

Bit 8 : INT, Interrupt.

Set 1: DMA unit generates an interrupt request when complete the transfer count .

The TC bit must set to 1 to generate an interrupt.

Bit 7-6: SYN1-SYN0, Synchronization Type Selection.

SYN1 , SYN0	--	Synchronization Type
0 , 0	--	Unsynchronized
0 , 1	--	Source synchronized

1 , 0 -- Destination synchronized

1 , 1 -- Reserved

Bit 5: P , Priority.

Set 1: It selects high priority for this channel when both DMA 0 and DMA 1 are transfer in same time.

Bit 4: TDRQ, Timer Enable/Disable Request

Set 1: Enable the DMA requests from timer 2.

Set 0: Disable the DMA requests from timer 2.

Bit 3: Reserved

Bit 2: CHG, Changed Start Bit. This bit must set to 1 when will modify the ST bit.

Bit 1: ST, Start/Stop DMA channel.

Set 1: Start the DMA channel

Set 0: Stop the DMA channel

Bit 0 : $\overline{B}$ /W, Byte/Word Select.

Set 1: The address is incremented or decremented by 2 after each transfer.

Set 0 :The address is incremented or decremented by 1 after each transfer.

DMA Transfer Count Register

Offset : D8h (DMA1)
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

Bit 15-0: TC15-TC0, DMA 1 transfer Count. The value of this register is decremented by 1 after each transfer.

DMA Destination Address High Register

Offset : D6h (DMA1)
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DDA19 - DDA16			

Bit 15-4: Reserved

Bit 3-0: DDA19-DDA16, High DMA 1 Destination Address. These bits are map to A19- A16 during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

DMA Destination Address Low Register

Offset : D4h (DMA1)
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDA15 - DDA0															

Bit 15-0: DDA15-DDA0, Low DMA 1 Destination Address. These bits are mapped to A15- A0 during a DMA transfer. The value of (DDA19-DDA0)b will increment or decrement by 2 after each DMA transfer.

DMA Source Address High Register

Offset : D2h (DMA1)
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DSA19 - DSA16			

Bit 15-4: Reserved

Bit 3-0: DSA19-DSA16, High DMA 1 Source Address. These bits are mapped to A19- A16 during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

DMA Source Address Low Register

Offset : D0h (DMA1)
Reset Value : —

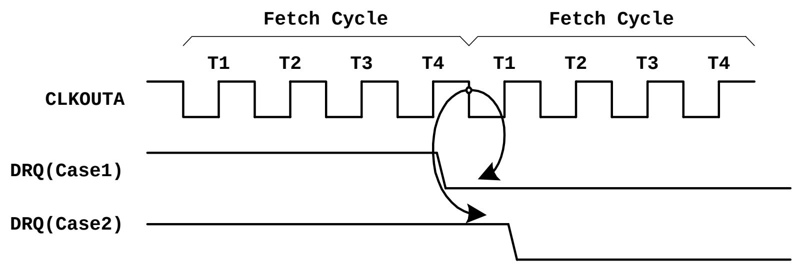
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSA15 - DSA0															

Bit 15-0: DSA15-DSA0, Low DMA 1 Source Address. These bits are map to A15- A0 during a DMA transfer. The value of (DSA19-DSA0)b will increment or decrement by 2 after each DMA transfer.

External Requests

External DMA requests are asserted on the DRQ pins. The DRQ pins are sampled on the falling edge of CLKOUTA. It takes a minimum of four clocks before the DMA cycle is initiated by the Bus Interface. The DMA request is cleared four clocks before the end of the DMA cycle. And no DMA acknowledge is provided, since the chip-selects (MCSx, PCSx) can be programmed to be active for a given block of memory or I/O space, and the DMA source and destination address registers can be programmed to point to the same given block.

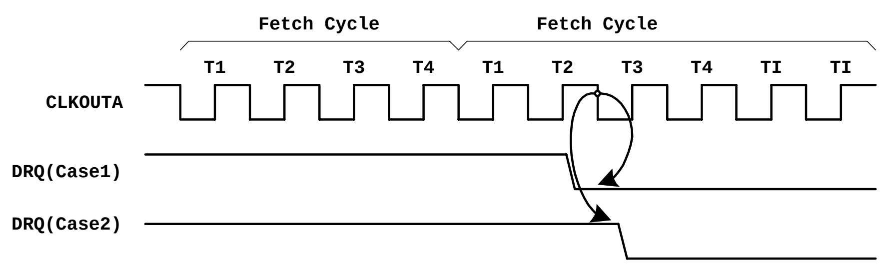
DMA transfer can be either source or destination synchronized, and it can also be unsynchronized. The Source-Synchronized Transfer figure shows the typical source-synchronized transfer which provides the source device at least three clock cycles from the time it is acknowledged to deassert its DRQ line.



NOTES:
Case1 : Current source synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current source synchronized transfer will be immediately followed by antoher DMA transfer.

Source-Synchronized Transfers

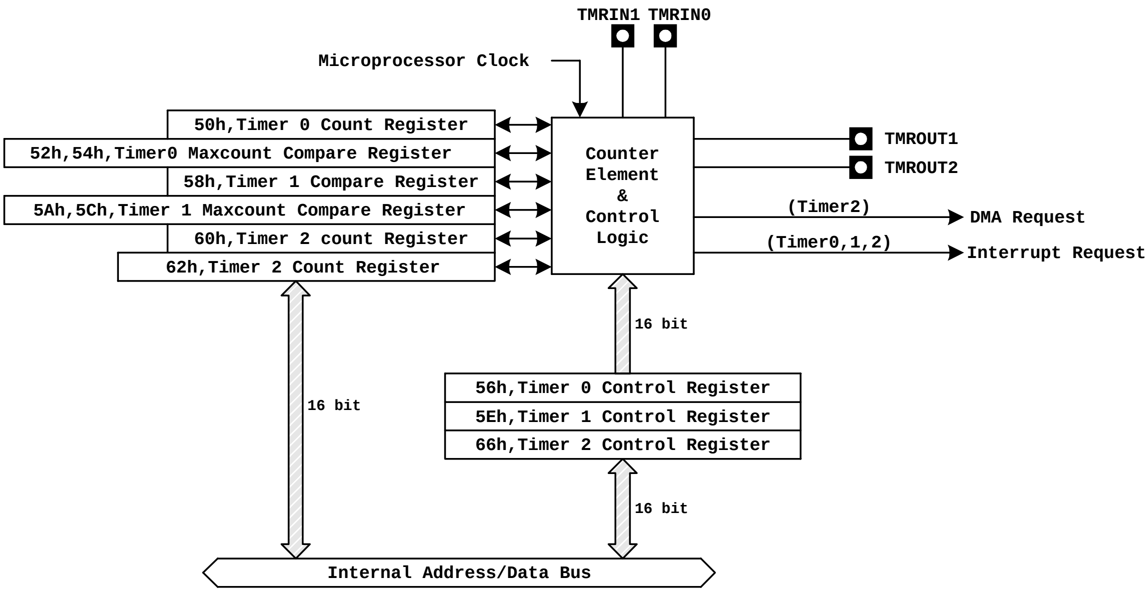
The Destination-Synchronized Transfer figure shows the typical destination-synchronized transfer which differs from a source-synchronized transfer in that two idle states are added to the end of the deposit cycle. The two idle states extend the DMA cycle to allow the destination device to deassert its DRQ pin four clocks before the end of the cycle. If the two idle states were not inserted, the destination device would not have time to deassert its DRQ signal.



NETES:
Case1 : Current destination synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current destination synchronized transfer will be immediately followed by another DMA transfer.

Destination-Synchronized Transfers

Timer Control Unit



Timer / Counter Unit Block

There are three 16-bit programmable timers in the R8800. The timer operation is independent of the CPU. The three timers can be programmed as a timer element or as a counter element. Timers 0 and 1 are each connect to two external pins (TMRIN0, TMROUT0, TMRIN1, TMROUT1) which can be used to count or time external events, or they can be used to generate a variable-duty-cycle waveforms. Timer 2 is not connected any external pins. It can be used as a prescale to timer 0 and timer 1 or as a DMA request source.

Timer 0 Mode / Control Register

Offset : 56h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	$\overline{INH}$	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

These bits definition for timer 0 are same as the bits of register 5Eh for timer 1.

Timer 0 Count Register

Offset : 50h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

Bit 15 – 0: TC15-TC0, Timer 0 Count Value. This register contains the current count of timer 0. The count is incremented by one every four internal processor clocks or by prescaled the timer 2, or by one every four external clock which is configured the external clock select bit to refer the TMRIN1 signal.

Timer 0 Maxcount Compare A Register

Offset : 52h

Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

Bit 15-0 : TC15 – TC0, Timer 0 Compare A Value.

Timer 0 Maxcount Compare B Register

Offset : 54h

Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

Bit 15-0 : TC15 – TC0, Timer 0 Compare B Value.

Timer 1 Mode / Control Register

Offset : 5Eh

Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	$\overline{\text{INH}}$	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

Bit 15: EN, Enable Bit.

Set 1: The timer 1 is enable.

Set 0: The timer 1 is inhibited from counting.

The $\overline{\text{INH}}$ bit must be set 1 during writing the EN bit, and the $\overline{\text{INH}}$ bit and EN bit must be in the same write.

Bit 14: $\overline{\text{INH}}$, Inhibit Bit. This bit is allows selective updating the EN bit. The $\overline{\text{INH}}$ bit must be set 1 during writing the EN bit, and both the $\overline{\text{INH}}$ bit and EN bit must be in the same write. This bit is not stored and is always read as 0.

Bit 13: INT, Interrupt Bit.

Set 1: A interrupt request is generated when the count register equals a maximum count. If the timer is configured in dual max-count mode, an interrupt is generated each time the count reaches max-count A or max-count B

Set 0: Timer 1 will not issue interrupt request.

Bit 12: RIU, Register in Use Bit.

Set 1: The Maxcount Compare B register of timer 1 is being used

Set 0: The Maxcount Compare A register of timer 1 is being used

Bit 11-6 : Reserved.

Bit 5: MC, Maximum Count Bit. When the timer reaches its maximum count, the MC bit will set to 1 by H/W. In dual maxcount mode, this bit is set each time either Maxcount Compare A or Maxcount Compare B register is reached. This bit is set regardless of the EN bit (66h.15).

Bit 4: RTG, Re-trigger Bit. This bit define the control function by the input signal of TMRIN1 pin. When EXT=1 (5Eh.2), this bit is ignored.

Set 1: Timer1 Count Register (58h) counts internal events; Reset the counting on every TMRIN1 input signal from low go high (rising edge trigger).

Set 0: Low input holds the timer 1 Count Register (58h) value; High input enables the counting which counts internal events.

The definition of setting the (EXT , RTG)

(0 , 0) – Timer1 counts the internal events. if the TMRIN1 pin remains high.

(0 , 1) -- Timer1 counts the internal events; count register reset on every rising transition on the TMRIN1 pin

(1 , x) -- TMRIN1 pin input acts as clock source and timer1 count register increase one every four external clock.

Bit 3: P, Prescaler Bit. This bit and EXT(5Eh.2) define the timer 1 clock source.

The definition of setting the (EXT , P)

(0 , 0) – Timer1 Count Register increase one every four internal processor clock.

(0 , 1) – Timer1 count register increase one which prescal by timer 2.

(1 , x) -- TMRIN1 pin input acts as clock source and Timer1 Count Register increase one every four external clock.

Bit 2: EXT, External Clock Bit.

Set 1: Timer 1 clock source from external

Set 0: Timer 1 clock source from internal

Bit 1 : ALT, Alternate Compare Bit. This bit controls whether the timer runs in single or dual maximum count mode.

Set 1: Specify dual maximum count mode. In this mode the timer counts to Maxcount Compare A, then resets the count register to 0. Then the timer counts to Maxcount Compare B, then resets the count register to 0 again, and starts over with Maxcount Compare A.

Set 0: Specify single maximum count mode. In this mode the timer will count to the valve contained in Maxcount Compare A and reset to 0, and then the timer counts to Maxcount Compare A again. Maxcount Compare B is not used in this mode.

Bit 0: CONT, Continuous Mode Bit.

Set 1: The timer to run continuously.

Set 0: The timer will halt after each counting to the maximum count and the EN bit will be cleared.

Timer 1 Count Register

Offset : 58h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

Bit 15 – 0: TC15-TC0, Timer 1 Count Value. This register contains the current count of timer 1. The count is incremented by one every four internal processor clocks or by prescaled the timer 2, or by one every four external clock which is configured the external clock select bit to refer the TMRIN1 signal.

Timer 1 Maxcount Compare A Register

Offset : 5Ah
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

Bit 15-0 : TC15 – TC0, Timer 1 Compare A Value.

Timer 1 Maxcount Compare B Register

Offset : 5Ch
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

Bit 15-0 : TC15 – TC0, Timer 1 Compare B Value.

Timer 2 Mode / Control Register

Offset : 66h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	$\overline{INH}$	INT	0	0	0	0	0	0	0	MC	0	0	0	0	CONT

Bit 15: EN, Enable Bit.

Set 1: The timer 2 is enable.

Set 0: The timer 2 is inhibited from counting.

The $\overline{INH}$ bit must be set 1 during writing the EN bit, and the $\overline{INH}$ bit and EN bit must be in the same write.

Bit 14: $\overline{INH}$, Inhibit Bit. This bit is allows selective updating the EN bit. The $\overline{INH}$ bit must be set 1 during writing the EN bit, and both the $\overline{INH}$ bit and EN bit must be in the same write. This bit is not stored and is always read as 0.

Bit 13: INT, Interrupt Bit.

Set 1: A interrupt request is generated when the count register equals a maximum count.

Set 0: Timer 2 will not issue interrupt request.

Bit 12-6 : Reserved.

Bit 5: MC, Maximum Count Bit. When the timer reaches its maximum count, the MC bit will set to 1 by H/W. This bit is set regardless of the EN bit (66h.15).

Bit 4-1: Reserved.

Bit 0: COUNT, Continuous Mode Bit.

Set 1: Timer is continuously running when timer reaches the maximum count.

Set 0: The EN bit (66h.15) is cleared and the timer is hold after each timer count reaches the maximum count.

Timer 2 Count Register

Offset : 60h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

Bit 15 – 0: TC15-TC0, Timer 2 Count Value. This register contains the current count of timer 2. The count is incremented by one every four internal processor clocks.

Timer 2 Maxcount Compare A Register

Offset : 62h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

Bit 15-0 : TC15 – TC0, Timer 2 Compare A Value.

Watchdog Timer

Timer 1 can also be configure as a watchdog timer. Software must fist programmed the Timer 1 Mode/Control (5Eh), Count (58h), and Max Count (5Ah, 5Ch) registers and then program the Watchdog Timer Interrupt Control Register (42h) to enable the watchdog timer interrupt , The Timer 1 Count Register must be reloaded at intervals less than the Timer 1 Maxcount value to assure the watchdog interrupt is not occurred.

Watchdog Timer Interrupt Control Register

Offset : 42h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4 : Reserved

Bit 3: MSK , Mask.

Set 1: Mask the interrupt source of the watchdog timer

Set 0: Enable the watchdog timer interrupt.

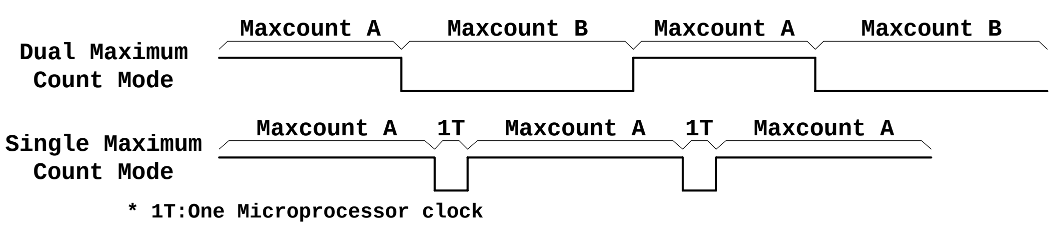
Bit 2- 0: PR, Priority.

The priority selection:

PR2	**PR1**	**PR0**	--	**Priority**	
0	0	0	--	0	(High)
0	0	1	--	1	
0	1	0	--	2	
0	1	1	--	3	
1	0	0	--	4	
1	0	1	--	5	
1	1	0	--	6	
1	1	1	--	7	(Low)

Timer/Counter Unit Output Mode

Timers 0 and 1 can use one maximum count value or two maximum count value. Timer 2 can use only one maximum count value. Timer 0 and timer1 can be configured to single or dual Maximum Compare count mode, the TMROUT0 or TMROUT1 signals can be used to generated waveform of various duty cycle.

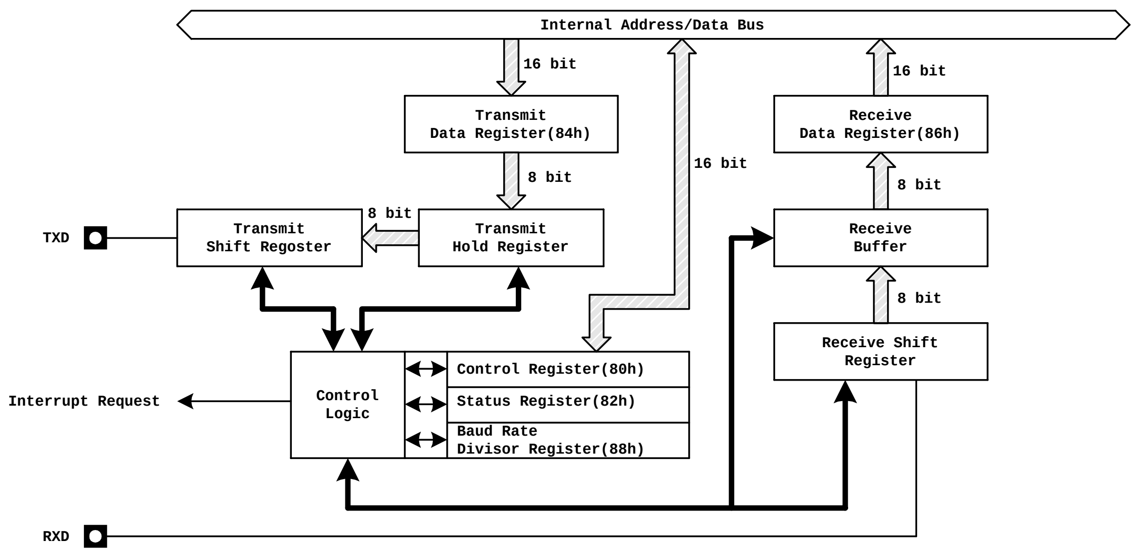


Timer/Counter Unit Output Modes

Asynchronous Serial Port

R8800 asynchronous serial port provides the TXD, RXD pins for the full duplex bi-directional data transfer and without handshaking signals. The UART port supports : 8-bit or 7-bit data transfer; odd parity, even parity, or no parity; 1 or 2 stop bits. DMA transfers through the serial port are not supported

The receive/transmit clock is based on the microprocessor clock. The serial port can be used in power-saved mode, but the transfer rate must be adjusted to correctly reflect the new internal operating frequency. Software is programmed through the 80h, 82h, 84h, 86h, 88h registers to configure the asynchronous serial port.



Serial Port Block Diagram

Serial Port Control Register

Offset : 80h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TXIE	RXIE	LOOP	BRK	BRKVAL	PMODE		WLGN	STP	TMOD	RSIE	RMODE

Bit 15-12: Reserved

Bit 11: TXIE, Transmit Holding Register Empty Interrupt Enable.

This bit is set 1 to enable serial port to generates an interrupt request when the transmit holding register is empty.

Bit 9: LOOP, Loopback.

Set 1: The serial port in the loopback mode. In this mode, the transmit shift register is connect to the transmit shift register internal and the TXD pin output high. It provides the serial port testing in this mode.

Bit 8: BRK, Send Break.

It should to check the TEMT bit (82h.6) is a 1 before setting the BRK bit.

Set 1: The serial port send a frame of continues level output on the TXD pin and the output level depends on the BRAVAL bit status, when any data is written to transmit data register.

Bit 7: BRKVAL, Break Value.

Set 1: TXD pin continuous drive high level signal during send break operation.

Set 0: TXD pin continuous drive low level signal during send break operation.

Bit 6-5: PMODE, Parity Mode. Parity generation and checking during transmission and reception.

Parity mode selection by (Bit 6 , Bit 5) : (0 , x) – No parity bit in frame , (1 , 0) – Odd number of 1s in frame. (1 , 1) – Even number of 1s in frame.

Bit 4: WLGN, Word Length.

Set 1: The serial port sends and receives 8 bits of data per frame.

Set 0: The serial port sends and receives 7 bits of data per frame.

Bit 3: STP, Stop Bits.

Set 1: Two stop bits are used to signify the end of a frame.

Set 0: One stop bit are used to signify the end of a frame.

Bit 2: TMODE, Transmit Mode.

Set 1: Enable the transmit section of the serial port.

Set 0: Disable the transmit section of the serial port.

Bit 1: RSIE, Receive Status interrupt Enable.

Set 1: Enable the receive section of serial port to generate an interrupt

Set 0: Disable the receive section of serial port to generate an interrupt

Bit 0: RMODE, Receive Mode.

Set 1: Enable the receive section of the serial port.

Set 0: Disable the receive section of the serial port.

Serial Port Status Register

Offset : 82h

Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									TEMT	THRE	RDR	BRK1	FER	PER	OER

Bit 15-7 : Reserved

Bit 6: TEMT, Transmitter Empty. Read only bit. This bit is set by H/W when the the transmit shift register is empty. It can not disable the transmit function when the bit is 0.

Bit 5: THRE, Transmit Holding Register Empty. Read only bit. When this bit is 1, the transmit holding buffer contains invalid data and the transmit data register (84h) can be written a new data. When this bit is 0, it indicate that transmit holding buffer contains valid data that not yet been copied to transmit shift register and the transmit data register (84h) can not be written a new data.

When the transmit interrupt is enabled, a serial port interrupt is generated when this bit is 1. The THRE bit is automatically cleared by H/W during copy data to transmit holding buffer.

Bit 4: RDR, Receive Data Ready. Read only bit. When the receive data register is ready to read, this bit is 1. When the bit is 0, the receive data register dose not contain valid data. This bit will be cleared by H/W when reading the receive data register.

Bit 3: BRKI, Break Interrupt. It indicates that a break has been receive when this bit is set 1 and it will generate a serial pot interrupt request if the RISE bit (80h.1) is enabled. This bit is set by H/W and should be cleared by software.

Bit 2: FER, Framing Error. This bit is set to indicate that a framing error occurred during reception of data and it will generate a serial pot interrupt request if the RISE bit (80h.1) is enabled. This bit is set by H/W and should be cleared by software.

Bit 1: PER, Parity Error. This bit is set to indicate that a party error occurred during reception of data and it will generate a serial pot interrupt request if the RISE bit (80h.1) is enabled. This bit is set by H/W and should be cleared by software.

Bit 0: OER, Overrun Error. This bit is set to indicate that a overrun error occurred during reception of data and it will generate a serial port interrupt request if the RISE bit (80h.1) is enabled. This bit is set by H/W and should be cleared by software.

Serial Port Transmit Data Register

Offset : 84h
Reset Value : —

15–8	7–0
Reserved	TDATA

Bit 15-8: Reserved

Bit 7-0 : TDATA, Transmit Data. Software writes this register with data to be transmitted on the serial port.
The THRE bit (82h.5) should be read as a 1 before writing this register to avoid overwriting data to this register.
When writing data to this register, the THRE bit will be cleared by H/W in the same time.

Serial Port Receive Data Register

Offset : 86h
Reset Value : —

15–8	7–0
Reserved	RDATA

Bit 15-8: Reserved

Bit 7-0: RDATA, Received DATA. The PDR bit (82h.4) should be read as 1 beforeread the RDATA register to avoid reading invalid data.

Serial Port Baud Rate Divisor Register

Offset : 88h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAUDDIV															

Bit 15-0: BAUDDIV, Baud Rate Divisor.

The general formula for baud rate divisor is **Baud Rate = Microprocessor Clock / [32 * (BAUDDIV+1)]**

For example, The Microprocessor clock is 22.1184MHz and the BAUDDIV=5 (Decimal), the baud rate of serial port is

115.2k.

Synchronous Serial Port

There are four pins for synchronous serial port interface, which is half duplex, bi-directional data transfer. The synchronous serial interface operates in a master/slave configuration, and the synchronous serial port of R8800 as a master mode. The SCLK frequency is affected by the reduced microprocessor clock frequency when in power-save mode. Software is programmed the 10h, 12h, 14h,16h, 18h to configured the synchronous serial port interface.

Synchronous Serial Status Register

Offset : 10h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													RE/TE	DR/DT	PB

Read only register that indicates the state of the SSI port.

Bit 15-3 : Reserved.

Bit 2 : **RE/TE,** Receive/Transmit Error Detect.

Set 1: Either a read of Synchronous Serial Receive register or a write to one transmit registers while the SSI is busy (PB=1).

Set 0: SDEN output is inactive.

Bit 1: DR/TR, Data Receive/Transmit Complete.

Set 1: End of the transfer of data bit 7 (SCLK rising edge) during a transmit or receive operation.

Set 0: When the SSR register is read, when one of the SSD0 or SSD1 registers is written, when the SSS register is read, or when both SDEN0 and SDEN1 become inactive.

Bit 0: PB, SSI port Busy.

Set 1: a transmit or receive operation is in progress.

Set 0: the port is ready to transmit or receive data.

Synchronous Serial Control Register

Offset : 12h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										SCLKDIV		Res		DE1	DE0

This read/write register controls the operation of the SDEN0-SDEN1 outputs the transfer rate of the SSI port.

Bit 15-3 : Reserved.

Bit 3-2 : SCLKDIV, SCLK Divide.

SCLKDIV	SCLK Frequency Divider
00b	Processor clock/2
01b	Processor clock/4

10b	Processor clock/8
11b	Processor clock/16

Bit 1 : DE1, SDEN1 Enable.

Set 1: SDEN1 pin is held High.

Set 0: SDEN1 pint is Low.

Bit 0 : DE0, SDEN0 Enable.

Set 1: SDEN0 pin is held High.

Set 0: SDEN0 pint is Low.

Synchronous Serial Transmit 1 Register

Offset : 14h
Reset Value : —

15–8	7–0
Reserved	SD

Synchronous Serial Transmit 1 Register. The register contains data to be transfer from the processor to the peripheral on a write operation.

Bit 15-8 : Reserved.

Bit 7-0: SD, Send Data. Data to transmit over the SDATA pin.

Synchronous Serial Transmit 0 Register

Offset : 16h
Reset Value : —

15–8	7–0
Reserved	SD

Synchronous Serial Transmit 0 Register. The register contains data to be transfer from the processor to the peripheral on a write operation.

Bit 15-8 : Reserved.

Bit 7-0: SD, Send Data. Data to transmit over the SDATA pin.

Synchronous Serial receive Register

Offset : 18h
Reset Value : —

15–8	7–0
Reserved	SR

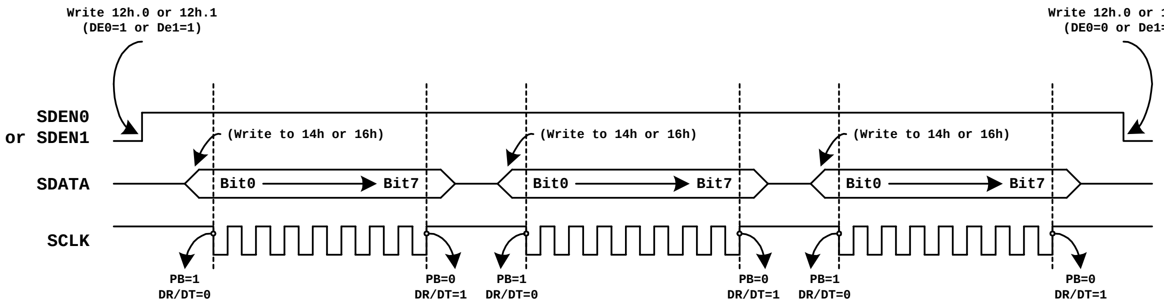
Th Synchronous Serial Receive Register contains the data transferred from the peripheral to the processor on a read operation.

Bit 15-8 : Reserved.

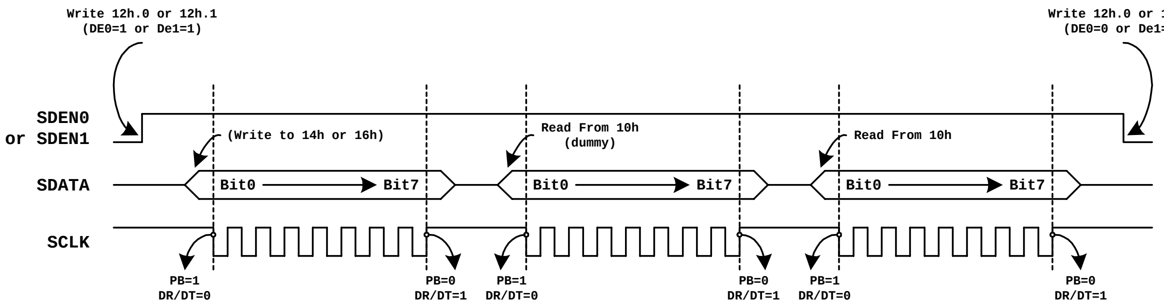
Bit 7-0: SR, Receive Data. Data received over the SDATA pin.

Synchronous serial port operation

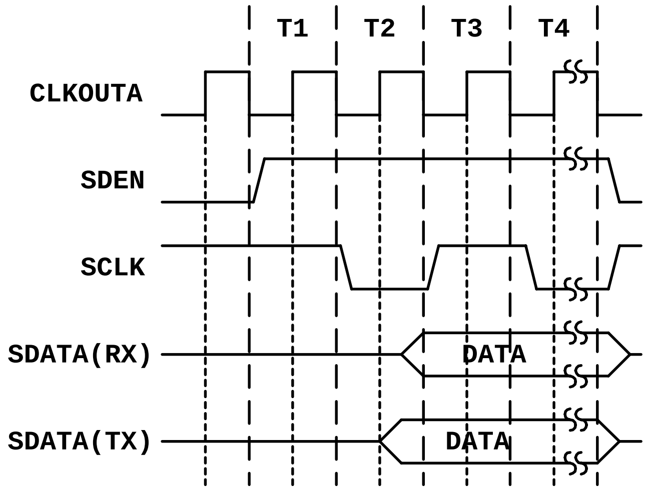
The following figures show the data transmit and data receive operation.



Synchronous Serial Port Multiple Write



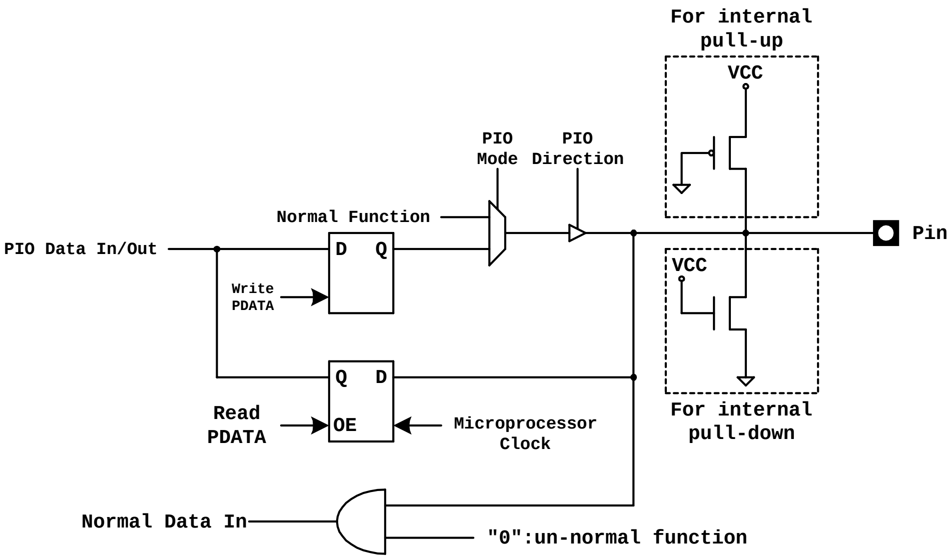
Synchronous Serial Port Multiple Read



Synchronous Serial Interface Waveforms

PIO Unit

R8800 provides 32 programmable I/O signals, which are multi-function pins with others normal function signals. Software is programmed through the registers (7Ah, 78h, 76h, 74h, 72h, 70h) to configure the multi-function pins for PIO or normal function.



PIO pin Operation Diagram

PIO multi-function Pin list table

PIO No.	Pin No.	Multi Function	Reset status/PIO internal resister
0	72	TMRIN1	Input with 10k pull-up
1	73	TMROUT1	Input with 10k pull-down
2	59	$\overline{\text{PCS6}}$ /A2	Input with 10k pull-up
3	60	$\overline{\text{PCS5}}$ /A1	Input with 10k pull-up
4	48	DT/ $\overline{\text{R}}$	Normal operation/ Input with 10k pull-up
5	49	DEN	Normal operation/ Input with 10k pull-up
6	46	SRDY	Normal operation/ Input with 10k pull-down
7	22	A17	Normal operation/ Input with 10k pull-up
8	20	A18	Normal operation/ Input with 10k pull-up
9	19	A19	Normal operation/ Input with 10k pull-up
10	74	TMROUT0	Input with 10k pull-down
11	75	TMRIN0	Input with 10k pull-up
12	77	DRQ0	Input with 10k pull-up
13	76	DRQ1	Input with 10k pull-up
14	50	$\overline{\text{MCS0}}$	Input with 10k pull-up
15	51	$\overline{\text{MCS1}}$	Input with 10k pull-up
16	66	$\overline{\text{PCS0}}$	Input with 10k pull-up
17	65	$\overline{\text{PCS1}}$	Input with 10k pull-up

18	63	$\overline{\text{PCS2}}$	Input with 10k pull-up
19	62	$\overline{\text{PCS3}}$	Input with 10k pull-up
20	3	SCLK	Input with 10k pull-up
21	100	SDATA	Input with 10k pull-up
22	2	SDEN0	Input with 10k pull-down
23	1	SDEN1	Input with 10k pull-down
24	68	$\overline{\text{MCS2}}$	Input with 10k pull-up
25	69	$\overline{\text{MCS3}}$ / $\overline{\text{RFSH}}$	Input with 10k pull-up
26	97	$\overline{\text{UZI}}$	Input with 10k pull-up
27	98	TXD	Input with 10k pull-up
28	99	RXD	Input with 10k pull-up
29	96	S6/ $\overline{\text{CLKDIV2}}$	Input with 10k pull-up
30	52	INT4	Input with 10k pull-up
31	54	INT2	Input with 10k pull-up

PIO Data 1 Register

Offset : 7Ah
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA (31 - 16)															

Bit 15- 0 : PDATA31-PDATA16, PIO Data Bits.

These bits PDATA31- PDATA16 map to the PIO31 –PIO16 which indicate the driven level when the PIO pin as an output or reflects the external level when the PIO pin as an input .

PIO Direction 1 Register

Offset : 78h
Reset Value : FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIR (31 - 16)															

Bit 15-0 : PDIR 31- PDIR16, PIO Direction Register.

Set 1: Configure the PIO pin as an input.

Set 0: Configure the PIO pin as an output or as normal pin function.

PIO Mode 1 Register

Offset : 76h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMODE (31 - 16)															

Bit 15-0: PMODE31-PMODE16, PIO Mode Bit.

The definition of PIO pins are configured by the combination of PIO Mode and PIO Direction. And the PIO pin is programmed individual.

The definition (PIO Mode, PIO Direction) for PIO pin function:

(0 , 0) – Normal operation , (0 , 1) – PIO input with pullup/pulldown

(1 , 0) – PIO output , (1 , 1) -- PIO input without pullup/pulldown

---

PIO Data 0 Register

Offset : 74h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA (15 - 0)															

Bit 15-0 : PDATA15- PDATA0 : PIO Data Bus.

These bits PDATA15- PDATA0 map to the PIO15 –PIO0 which indicate the driven level when the PIO pin as an output or reflects the external level when the PIO pin as an input.

PIO Direction 0 Register

Offset : 72h
Reset Value : FC0Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIR (15 - 0)															

Bit 15-0 : PDIR 15- PDIR0, PIO Direction Register.

Set 1: Configure the PIO pin as an input.

Set 0: Configure the PIO pin as an output or as normal pin function.

PIO Mode 0 Register

Offset : 70h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMODE (15 - 0)															

Bit 15-0: PMODE15-PMODE0, PIO Mode Bit.

PSRAM Control Unit

The PSRAM interface is provided by the R8800 and the refresh control unit automatically generates refresh bus cycles. The refresh control unit uses the internal microprocessor clock as a operating source clock. if the power-saved mode is enabled, the refresh control unit must be programmed to reflect the new clock rate. Software programs the registers (E0, E2, E4) to control the refresh control unit operation.

Memory Partition Register

Offset : E0h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M6 - M0							0	0	0	0	0	0	0	0	0

Bit 15-9: M6-M0, Refresh Base. M6-M0 map to A19-A13 of the 20-bit memory refresh address.

Bit 8-0 : Reserved.

Clock Prescaler Register

Offset : E2h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RC8 - RC0								

Bit 15-9 : Reserved

Bit 8-0: RC8-RC0, Refresh Counter Reload Value.

Enable RCU Register

Offset : E4h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E	0	0	0	0	0	0	T8 - T0								

Bit 15: E, Enable RCU.

Set 1: Enable the refresh counter unit

Set 0 : Disable the refresh counter unit.

Bit 14-9 : Reserved

Bit 8-0: T8-T0, Refresh Count. Read only bits and these bits present value of the down counter which triggers refresh requests.

INSTUCTION SET OPCODES AND CLOCK CYCLES

Function	Format				Clocks	Notes
DATA TRANSFER INSTRUCTIONS						
MOV = Move						
register to register/memory	1000100w	mod reg r/m			1/1	
register/memory to register	1000101w	mod reg r/m			1/6	
immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	1/1	
immediate to register	1011w reg	data	data if w=1		1	
memory to accumulator	1010000w	addr-low	addr-high		6	
accumulator to memory	1010001w	addr-low	addr-high		1	
register/memory to segment register	10001110	mod 0 reg r/m			3/8	
segment register to register/memory	10001100	mod 0 reg r/m			2/2	
PUSH = Push						
memory	11111111	mod 110 r/m			8	
register	01010 reg				3	
segment register	000reg110				2	
immediate	011010s0	data	data if s=0		1	
POP = Pop						
memory	10001111	mod 000 r/m			8	
register	01011 reg				6	
segment register	000 reg 111	(reg≠01)			8	
PUSHA = Push all	01100000				36	
POPA = Pop all	01100001				44	
XCHG = Exchange						
register/memory	1000011w	mod reg r/m			3/8	
register with accumulator	10010 reg				3	
XTAL = Translate byte to AL	11010111				10	
IN = Input from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
OUT = Output from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
LEA = Load EA to register	10001101	mod reg r/m			1	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		14	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		14	
ENTER = Build stack frame	11001000	data-low	data-high	L		
L = 0					7	
L = 1					11	
L > 1					11+10(L-1)	
LEAVE = Tear down stack frame	11001001				7	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				2	
PUSHF = Push flags	10011100				2	
POPF = Pop flags	10011101				11	
ARITHMETIC INSTRUCTIONS						
ADD = Add						
reg/memory with register to either	000000dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 000 r/m	data	data if sw=01	1/8	
immediate to accumulator	0000010w	data	data if w=1		1	

Function	Format				Clocks	Notes
ADC = Add with carry						
reg/memory with register to either	000100dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 010 r/m	data	data if sw=01	1/8	
immediate to accumulator	0001010w	data	data if w=1		1	
INC = Increment						
register/memory	1111111w	mod 000 r/m			1/8	
register	01000 reg				1	
SUB = Subtract						
reg/memory with register to either	001010dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 101 r/m	data	data if sw=01	1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
SBB = Subtract with borrow						
reg/memory with register to either	000110dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 011 r/m			1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
DEC = Decrement						
register/memory	1111111w	mod 001 r/m			1/8	
register	01001 reg				1	
NEG = Change sign						
register/memory	1111011w	mod reg r/m			1/8	
CMP = Compare						
register/memory with register	0011101w	mod reg r/m			1/7	
register with register/memory	0011100w	mod reg r/m			1/7	
immediate with register/memory	100000sw	mod 111 r/m	data	data if sw=01	1/7	
immediate with accumulator	0011110w	data	data if w=1		1	
MUL = multiply (unsigned)	1111011w	mod 100 r/m				
register-byte					13	
register-word					21	
memory-byte					18	
memory-word					26	
IMUL = Integer multiply (signed)	1111011w	mod 101 r/m				
register-byte					16	
register-word					24	
memory-byte					21	
memory-word					29	
register/memory multiply immediate (signed)	011010s1	mod reg r/m	data	data if s=0	23/28	
DIV = Divide (unsigned)	1111011W	mod 110 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
IDIV = Integer divide (signed)	1111011w	mod 111 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
AAS = ASCII adjust for subtraction	00111111				3	
DAS = Decimal adjust for subtraction	00101111				2	
AAA = ASCII adjust for addition	00110111				3	
DAA = Decimal adjust for addition	00100111				2	
AAD = ASCII adjust for divide	11010101	00001010			14	
AAM = ASCII adjust for multiply	11010100	00001010			15	
CBW = Corrvert byte to word	10011000				2	
CWD = Convert word to double-word	10011001				2	

Function	Format				Clocks	Notes
BIT MANIPULATION INSTRUCTUIONS						
NOT = Invert register/memory	1111011w	mod 010 r/m			1/7	
AND = And						
reg/memory and register to either	001000dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 100 r/m	data	data if w=1	1/8	
immediate to accumulator	0010010w	data	data if w=1		1	
OR = Or						
reg/memory and register to either	000010dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1	1/8	
immediate to accumulator	0000110w	data	data if w=1		1	
XOR = Exclusive or						
reg/memory and register to either	001100dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	1/8	
immediate to accumulator	0011010w	data	data if w=1		1	
TEST = And function to flags , no result						
register/memory and register	1000010w	mod reg r/m			1/7	
immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1	1/8	
immediate data and accumulator	1010100w	data	data if w=1		1	
Sifts/Rotates						
register/memory by 1	1101000w	mod TTT r/m			2/8	
register/memory by CL	1101001w	mod TTT r/m			1+n / 7+n	
register/memory by Count	1100000w	mod TTT r/m	count		1+n / 7+n	
STRING MANIPULATION INSTRUCTIONS						
MOVS = Move byte/word	1010010w				13	
INS = Input byte/word from DX port	0110110w				13	
OUTS = Output byte/word to DX port	0110111w				13	
CMPS = Compare byte/word	1010011w				18	
SCAS = Scan byte/word	101011w				13	
LODS = Load byte/word to AL/AX	1010110w				13	
STOS = Store byte/word from AL/AX	1010101w				7	
Repeated by count in CX:						
MOVS = Move byte/word	11110010	1010010w			4+9n	
INS = Input byte/word from DX port	11110010	0110110w			5+9n	
OUTS = Output byte/word to DX port	11110010	0110111w			5+9n	
CMPS = Compare byte/word	1111011z	1010011w			4+18n	
SCAS = Scan byte/word	1111001z	1010111w			4+13n	
LODS = Load byte/word to AL/AX	11110010	0101001w			3+9n	
STOS = Store byte/word from AL/AX	11110100	0101001w			4+3n	
PROGRAM TRANSFER INSTRUCTIONS						
Conditional Transfers — jump if:						
JE/JZ = equal/zero	01110100	disp			1/9	
JL/JNGE = less/not greater or equal	01111100	disp			1/9	
JLE/JNG = less or equal/not greater	01111110	disp			1/9	
JC/JB/JNAE = carry/below/not above or equal	01110010	disp			1/9	
JBE/JNA = below or equal/not above	01110110	disp			1/9	
JP/JPE = parity/parity even	01111010	disp			1/9	
JO = overflow	01110000	disp			1/9	
JS = sign	01111000	disp			1/9	
JNE/JNZ = not equal/not zero	01110101	disp			1/9	
JNL/JGE = not less/greater or equal	01111101	disp			1/9	
JNLE/JG = not less or equal/greater	01111111	disp			1/9	
JNC/JNB/JAE = not carry/not below /above or equal	01110011	disp			1/9	
JNBE/JA = not below or equal/above	01110111	disp			1/9	
JNP/JPO = not parity/parity odd	01111011	disp			1/9	
JNO = not overflow	01110001	disp			1/9	
JNS = not sign	01111001	disp			1/9	

Function	Format	Clocks	Notes
Unconditional Transfers			
CALL = Call procedure			
direct within segment	11101000 | disp-low | disp-high	11	
reg/memory indirect within segment	11111111 | mod 010 r/m	12/17	
indirect intersegment	11111111 | mod 011 r/m | (mod≠11)	25	
direct intersegment	10011010 | segment offset | selector	18	
RET = Retum from procedure			
within segment	11000011	16	
within segment adding immed to SP	11000010 | data-low | data-high	16	
intersegment	11001011	23	
instersegment adding immed to SP	1001010 | data-low | data-high	23	
JMP = Unconditional jump			
short/long	11101011 | disp-low	9/9	
direct within segment	11101001 | disp-low | disp-high	9	
reg/memory indirect within segment	11111111 | mod 100 r/m	11/16	
indirect intersegment	11111111 | mod 101 r/m | (mod ?11)	18	
direct intersegment	11101010 | segment offset | selector	11	
Iteration Control			
LOOP = Loop CX times	11100010 | disp	7/16	
LOOPZ/LOOPE = Loop while zero/equal	11100001 | disp	7/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000 | disp	7/16	
JCXZ = Jump if CX = zero	11100011 | disp	7/15	
Interrupt			
INT = Interrupt			
Type specified	11001101 | type	41	
Type 3	11001100	41	
INTO = Interrupt on overflow	11001110	43/4	
BOUND = Detect value out of range	01100010 | mod reg r/m	21-60	
IRET = Interrupt return	11001111	31	
PROCESSOR CONTROL INSTRUCTIONS			
CLC = clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	5	
STI = Set interrupt	11111011	5	
HLT = Halt	11110100	1	
WAIT = Wait	10011011	1	
LOCK = Bus lock prefix	11110000	1	
ESC = Math coprocessor escape	11011MMM | mod PPP r/m	1	
NOP = No operation	10010000	1	
SEGMENT OVERRIDE PREFIX			
CS	00101110	2	
SS	00110110	2	
DS	00111110	2	
ES	00100110	2	

R8800 Execution Timings

The above instruction timing represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

1. The opcode, along with and data or displacement required for execution, has been prefetched and resides in the instruction queue at the time is needed.
2. No wait states or bus HOLDs occur.
3. All word -data is located on even-address boundaries.
4. One RISC micro operation(*u*OP) maps one cycle(according the pipeline stages described below) , except the following case:

Pipeline Stages for single micro operation(one cycle):

Fetch → Decode → op_r → ALU → WB (For ALU function *u*OP)

Fetch → Decode → EA → Access → WB (For Memory function *u*OP)

4.1 *Memory read u*OP need 6 cycles for bus.

Pipeline stages for *Memory read u*OP(6 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB

Bus Cycle (Idle … T3)

4.2 *Memory push u*OP need 1 cycle if it has no previous *Memory push u*OP, and 5 cycles if it has previous *Memory push* or *Memory Write u*OP.

Pipeline stages for *Memory push u*OP after *Memory push u*OP (another 5 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB (1st *Memory push u*OP)

(2nd *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

pipeline stall (the four shaded Access stages)

4.3 *MUL u*OP and *DIV* of ALU function *u*OP for 8 bits operation need both 8 cycles, for 16 bits operation need both 16 cycles.

4.4 All jumps, calls, ret and loopXX instructions required to fetch the next instruction for the destination address(*Unconditional Fetch u*OP) will need 9 cycles.

Pipeline stages for unconditional fetch:

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → Fetch (*Fetch u*OP)

(next *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

will be flushed (the whole next *u*OP row)

These 9 cycles caused branch penalty (Fetch … T3)

→ Fetch → Decode → following stages...(New *u*OP)

Note: op_r: operand read stage, EA: Calculate Effective Address stage, Idle: Bus Idle stage, T0..T3: Bus T0..T3 stage, Access: Access data from cache memory stage.

DC Characteristics

Absolute Maximum Rating

Symbol	Rating	Commercial	Unit	Note
Vterm	Terminal Voltage with Respect To GND	-0.5 to Vcc+0.5 V	V	
Ta	Operating Temperature	0 to +70	Centigrade	
Pt	Power Dissipation	1.5	W	

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.75	5	5.25	V
GND	Ground	0	0	0	V
Vih	Input High Voltage(1)	2.0	---	Vcc+0.5	V
Vih1	Input High Voltage(RES)	3		Vcc+0.5	V
Vih2	Input High Voltage (X1)	3		Vcc+0.5	V
Vil	Input Low voltage	-0.5	0	0.8	V

Note 1:RES,X1 pins not included

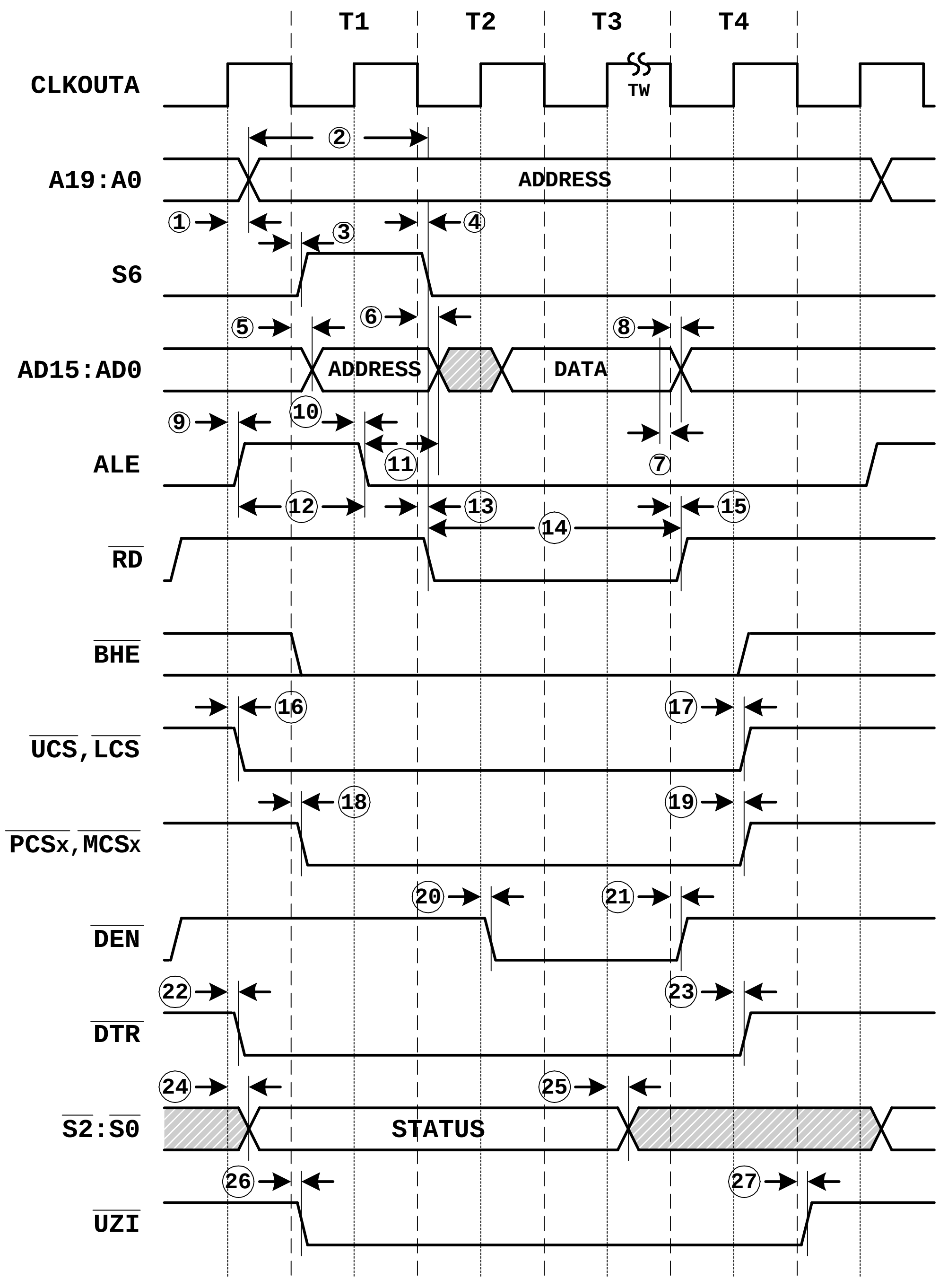
DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
Ili	Input Leakage Current	Vcc=Vmax Vin=GND to Vmax	-10	10	uA
Ili(with 10K pull R)	Input Leakage Current With Pull_R 10K enable	Vcc=Vmax Vin=GND to Vmax	-400	400	uA
Ili(with 50K pull R)	Input Leakage Current With Pull_R 50K	Vcc=Vmax Vin=GND to Vmax	-120	120	uA
Ilo	Output Leakage Current	Vcc=Vmax Vin=GND to Vmax	-10	10	uA
VOL	Output Low Voltage	Iol=6mA, Vcc=Vmin.	_____	0.4	V
VOH	Output High Voltagr	Ioh=-6mA, Vcc=Vmin.	2.4	____	V
Icc	Max Operating Current	Vcc=5.25V 40MHz	---	140	ma

Note1:Vmax=5.25V Vmin=4.75V

Symbol	Parameter	Min.	Max.	Unit	Note
Fmax	Max operation clock frequency	0	40	Mhz	Vcc+-5%

AC Characteristics



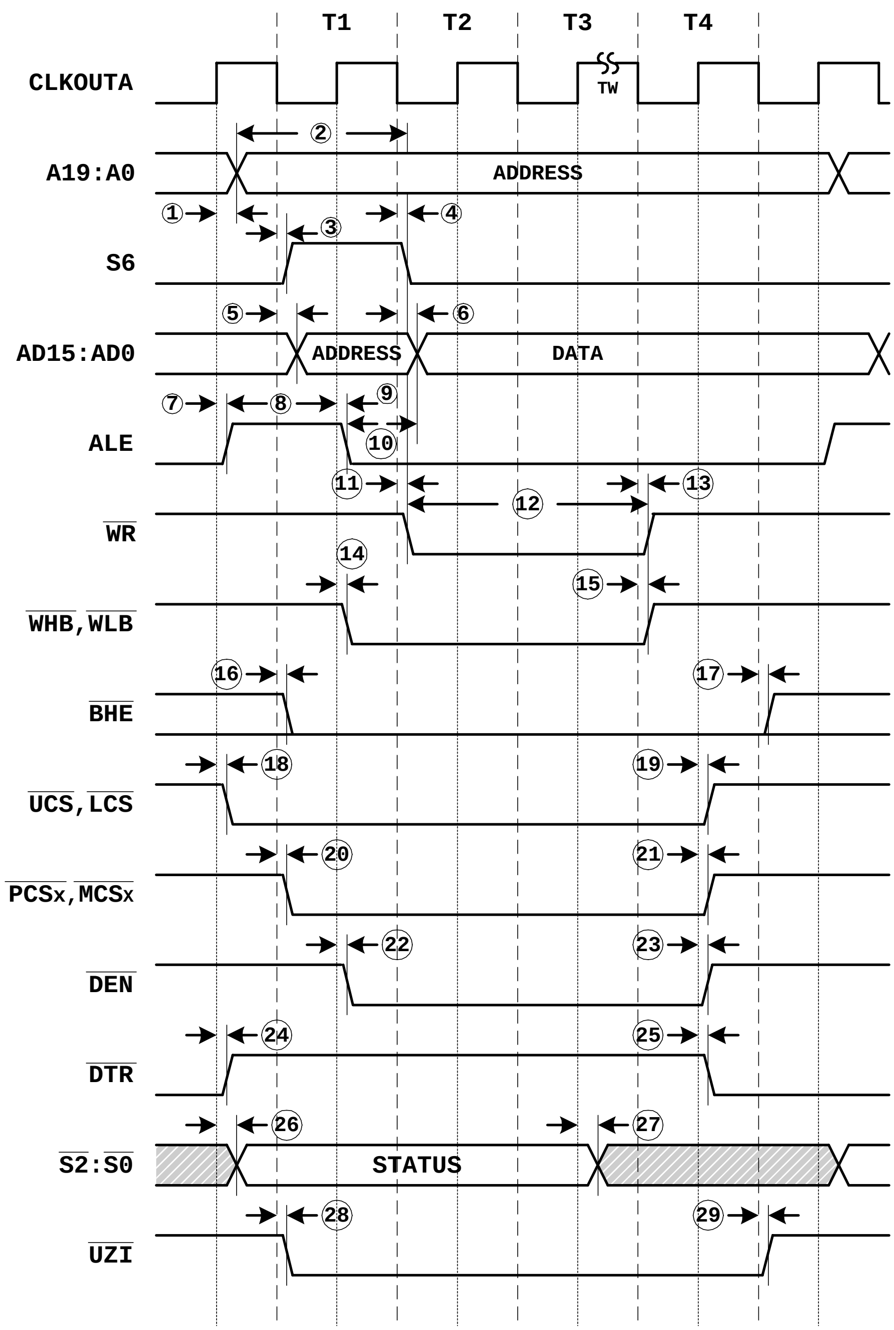
READ CYCLE

No.	Description	MIN	MAX	Unit
1	CLKOUTA high to A Address Valid	0	12	ns
2	A address valid to $\overline{RD}$ low	1.5T-9		ns
3	S6 active delay	0	15	ns
4	S6 inactive delay	0	15	ns
5	AD address Valid Delay	0	12	ns
6	Address Hold	0	12	ns
7	Data in setup	5		ns
8	Data in Hold	2		ns
9	ALE active delay	0	12	ns
10	ALE inactive delay	0	12	ns
11	Address Valid after ALE inactive	T/2-5		ns
12	ALE width	T-5		ns
13	$\overline{RD}$ active delay	0	12	ns
14	$\overline{RD}$ Pulse Width	2T-10		ns
15	$\overline{RD}$ inactive delay	0	12	ns
16	CLKOUTA HIGH to $\overline{LCS}$ $\overline{UCS}$ valid	0	15	ns
17	UCS,LCS inactive delay	0	15	ns
18	$\overline{PCS}$, $\overline{MCS}$ active delay	0	15	ns
19	$\overline{PCS}$, $\overline{MCS}$ inactive delay	0	15	ns
20	$\overline{DEN}$ active delay	0	15	ns
21	$\overline{DEN}$ inactive delay	0	15	ns
22	DTR active delay	0	15	ns
23	DTR inactive delay	0	15	ns
24	Status active delay	0	15	ns
25	Status inactive delay	0	15	ns
26	$\overline{UZI}$ active delay	0	15	ns
27	$\overline{UZI}$ inactive delay	0	15	ns

1. T means a clock period time

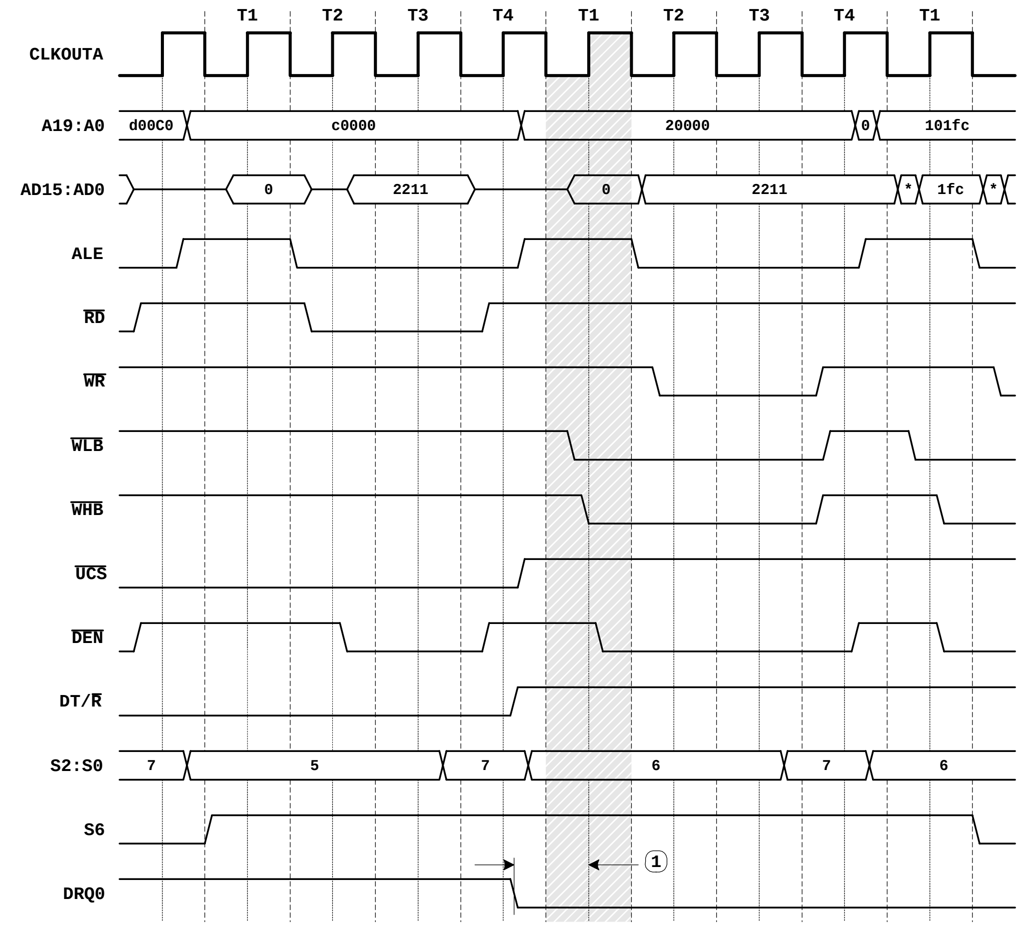
2. All timing parameters are measured at 1.5V with 50 PF loading on CLKOUTA

. All output test conditions are with CL=50 pF


T1
T2
T3
T4
CLKOUTA
TW
A19:A0
ADDRESS
S6
AD15:AD0
ADDRESS
DATA
ALE
WR
WHB,WLB
BHE
UCS,LCS
PCSx,MCSx
DEN
DTR
S2:S0
STATUS
UZI

WRITE CYCLE

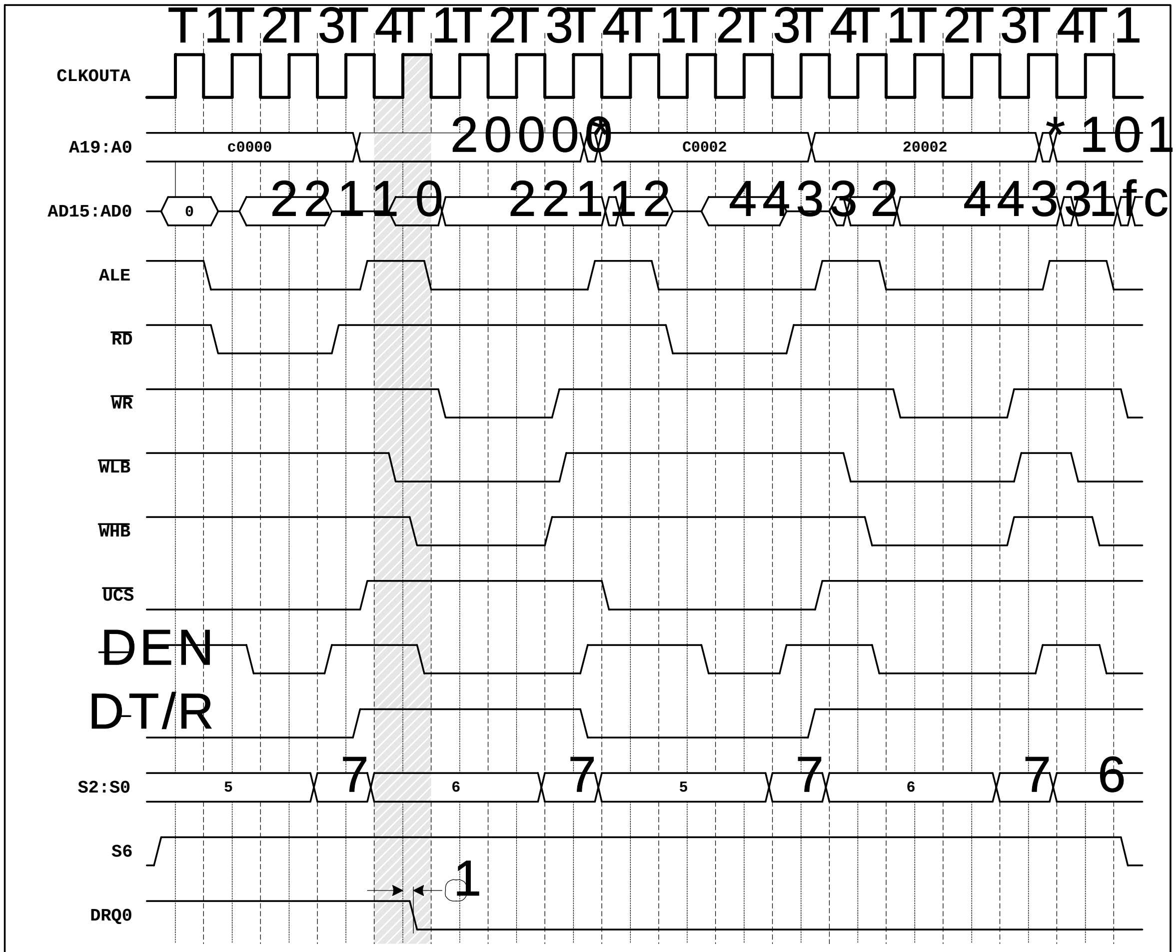
No.	Description	MIN	MAX	Unit
1	CLKOUTA high to A Address Valid	0	12	ns
2	A address valid to $\overline{WR}$ low	1.5T-9		ns
3	S6 active delay	0	15	ns
4	S6 inactive delay	0	15	ns
5	AD address Valid Delay	0	12	ns
6	Address Hold			ns
7	ALE active delay	0	12	ns
8	ALE width	T-10		ns
9	ALE inactive delay	0	12	ns
10	Address valid after ALE inactive	1/2T-5		ns
11	$\overline{WR}$ active delay	0	12	ns
12	$\overline{WR}$ pulse width	2T-10		ns
13	$\overline{WR}$ inactive delay	0	12	ns
14	$\overline{WHB}$, $\overline{WLB}$ active delay	0	15	ns
15	$\overline{WHB}$, $\overline{WLB}$ inactive delay	0	15	ns
16	BHE active delay	0	15	ns
17	BHE inactive delay	0	15	ns
18	CLKOUTA high to $\overline{UCS}$, $\overline{LCS}$ valid	0	15	ns
19	$\overline{UCS}$, $\overline{LCS}$ inactive delay	0	15	ns
20	$\overline{PCS}$, $\overline{MCS}$ active delay	0	15	ns
21	$\overline{PCS}$, $\overline{MCS}$ inactive delay	0	15	ns
22	$\overline{DEN}$ active delay	0	15	ns
23	$\overline{DEN}$ inactive delay	0	15	ns
24	$\overline{DTR}$ active delay	0	15	ns
25	$\overline{DTR}$ inactive delay	0	15	ns
26	Status active delay	0	15	ns
27	Status inactive delay	0	15	ns
28	$\overline{UZI}$ active delay	0	15	ns
29	$\overline{UZI}$ inactive delay	0	15	ns



DMA (1)

*** The source-synchronized transfer is not followed immediately by another DMA transfer**

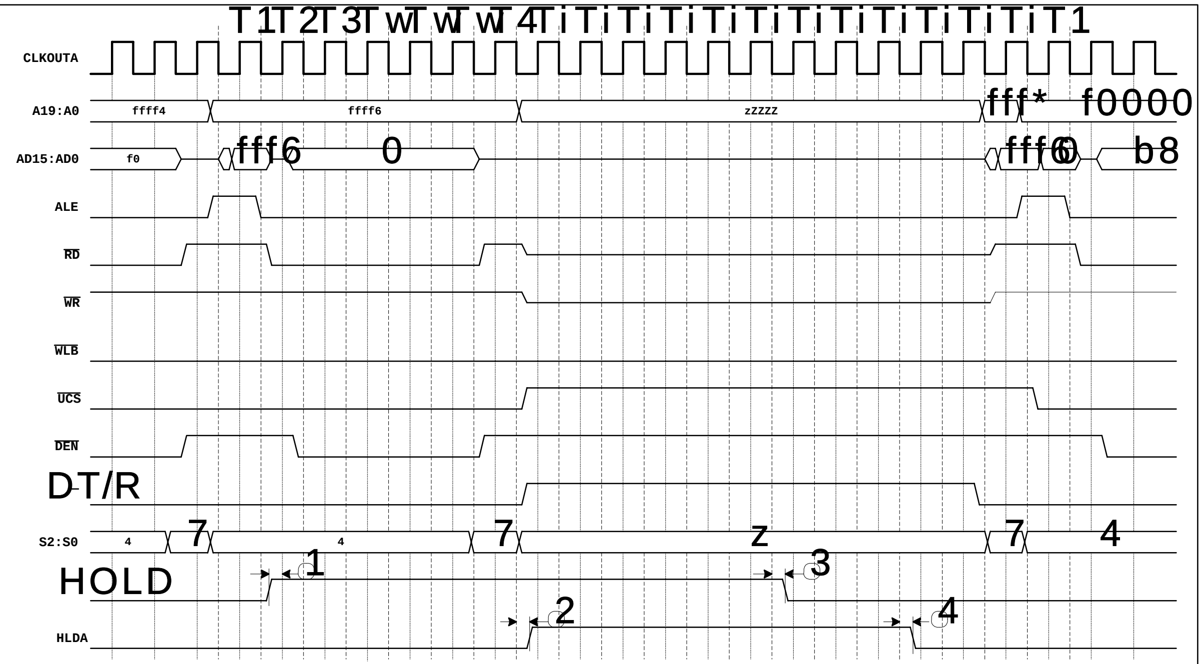
No.	Description	MIN	MAX	Unit
1	DRQ is confirmed time	5		ns



DMA (2)

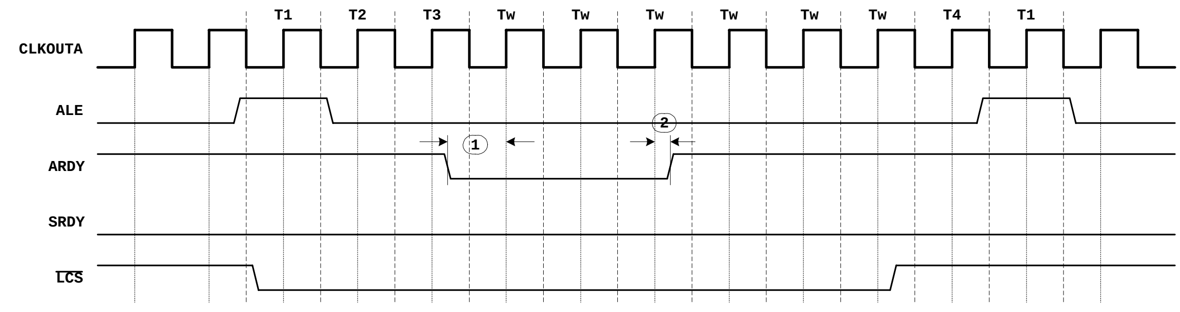
*** The source-synchronized transfer is followed immediately by another DMA transfer**

No.	Description	MIN	MAX	Unit
1	DRQ is confirmed time	2	0	ns



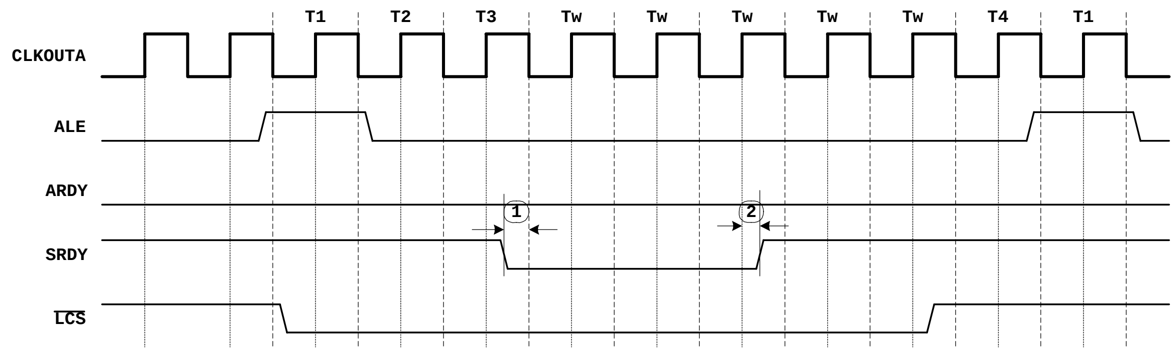
HOLD/HLDA Timing

No.	Description	MIN	MAX	Unit
1	HOLD setup time	5	0	ns
2	HLDA Valid Delay	0	15	ns
3	HOLD hold time	2	0	ns
4	HLDA Valid Delay	0	15	ns



ARDY Timing

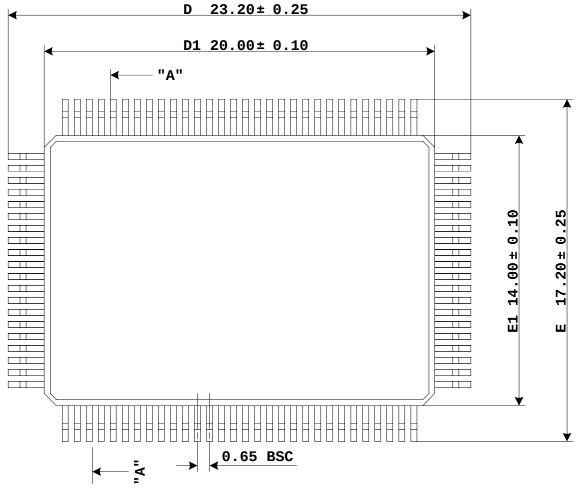
No.	Description	MIN	MAX	Unit
1	ARDY Resolution Transition setup time	5	0	ns
2	ARDY active hold time	5	0	ns

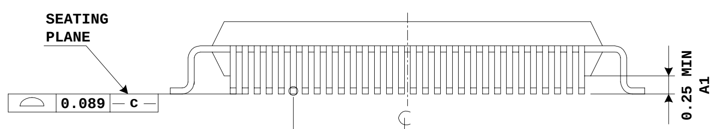


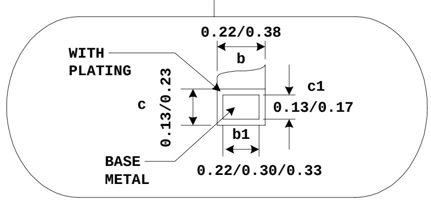
SRDY Timing

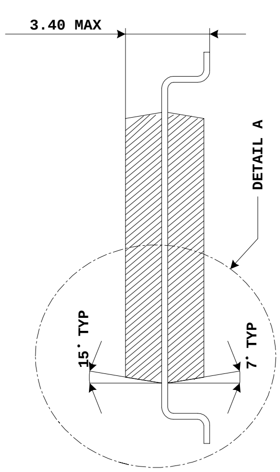
No.	Description	MIN	MAX	Unit
1	SRDY transition setup time	5	0	ns
2	SRDY transition hold time	5	0	ns

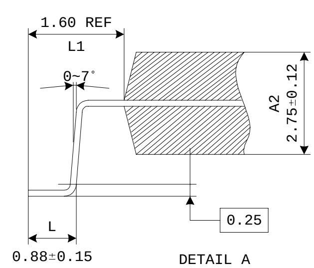
PACKAGE INFORMATION
(PQFP)



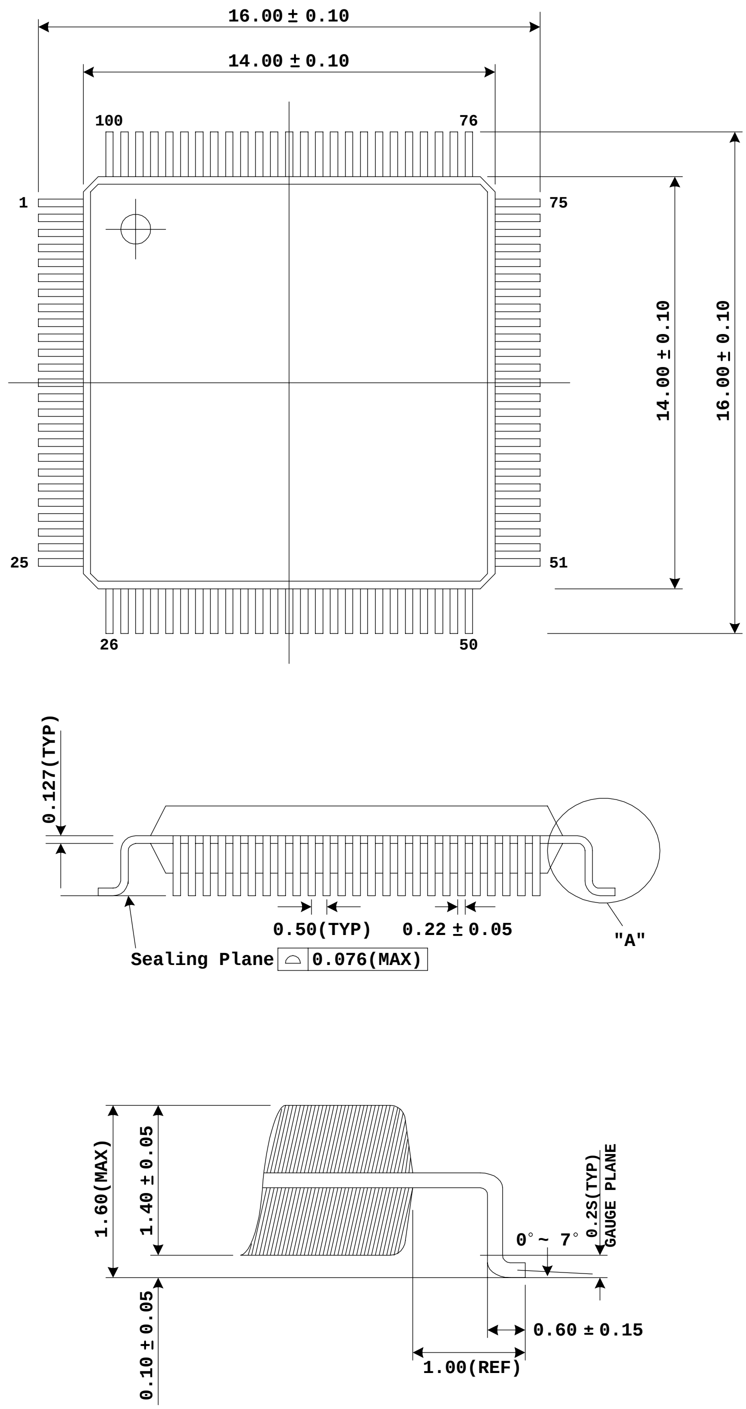








(LQFP)


16.00 ± 0.10
14.00 ± 0.10
100
76
1
75
25
51
26
50
14.00 ± 0.10
16.00 ± 0.10
0.127(TYP)
0.50(TYP)
0.22 ± 0.05
"A"
Sealing Plane
0.076(MAX)
1.60(MAX)
1.40 ± 0.05
0.10 ± 0.05
0° ~ 7°
0.25(TYP)
GAUGE PLANE
0.60 ± 0.15
1.00(REF)

UNIT:mm

Revision History

Rev.	Date	History
0.1	2000/3/8	Preliminary release
1.0	2000/7/31	Formal release
1.1	2000/9/1	Adding the pin configuration & package information for LQFP package.
1.2	2001/2/20	Add AC/DC.
1.3	2001/3/13	Add PQFP and LQFP Pin-Out Table
1.4	2001/8/7	Modify Wait state description(p26).
1.5	2001/12/12	DC Characteristics
1.6	2001/12/24	Modify Oscillator Characteristics
1.7	2002/05/06	Modify Wait State Description