

CLD SERIES: CLOCK OSCILLATOR, LVDS, +3.3 VDC

DESCRIPTION: A crystal controlled, high frequency, highly stable oscillator, adhering to Low Voltage Differential Signaling (LVDS) Standards. The output can be Tri-stated to facilitate testing or combined multiple clocks. The device is contained in a sub-miniature, very low profile, leadless ceramic SMD package with 6 gold contact pads. This miniature oscillator is ideal for today's automated assembly environments.

APPLICATIONS AND FEATURES:

- Infiniband; 10GbE; Network Processors; SOHO Routing; Switches; WAN Interfaces
- Common Frequencies: 106.25 MHz; 125 MHz; 150 MHz; 155.52 MHz; 156.25 MHz; 161.1328 MHz
- +3.3 VDC LVDS
- Frequency Range from 80 to 250 MHz
- Miniature Ceramic SMD Package Available on Tape and Reel
- Lead Free

■ ELECTRICAL PARAMETERS:

PARAMETER	SYMBOL	TEST CONDITIONS ^{*1}	VALUE	UNIT
Nominal Frequency	fo		80.000 ~ 250.000	MHz
Supply Voltage	V _{cc}		+3.3 ±5%	VDC
Supply Current	I _s		60.0 MAX	mA
Output Logic Type			LVDS	
Load		Connected between Out and Complementary Out	100	Ω
Output Voltage Levels	V _{oh} V _{ol}		1.43 TYP; 1.60 MAX 0.90 MIN; 1.10 TYP	VDC VDC
Duty Cycle	DC	Measured at 50% of V _{cc}	40/60 to 60/40 or 45/55 to 55/45	%
Rise / Fall Time	t _r / t _f	Measured at 20/80% and 80/20% V _{cc} Levels	1.0 TYP ^{*2}	ns
Jitter	J	RMS, F _j = 12 kHz...20 MHz	1 TYP	ps
Overall Frequency Stability	Δf/fc	Op. Temp., Aging, Load, Supply and Cal. Variations	±25, ±50, or ±100 MAX ^{*3}	ppm
Pin 1 Output Enabled	En	High Voltage or No Connect	0.7•V _{cc} MIN	VDC
Pin 1 Output Disabled	Dis	Ground	0.3•V _{cc} MAX	VDC
Absolute voltage range	V _{cc} (abs)	Non-Destructive	-0.5...+7.0	VDC

*1 Test Conditions Unless Stated Otherwise: Nominal V_{cc}, Nominal Load, +25 ±3°C

*2 Frequency Dependent

*3 Not All Stabilities Available With All Temperature Ranges—Please Consult Factory For Availability

■ ENVIRONMENTAL PARAMETERS:

PARAMETER	SYMBOL	TEST CONDITIONS ^{*1}	VALUE	UNIT
Operating temperature range	T _a		SEE PART NUMBER TABLE	°C
Storage temperature range	T(stg)		-55...+90	°C

■ PART NUMBERING SYSTEM:

SERIES	SYMMETRY	TEMPERATURE RANGE (°C)	FREQUENCY STABILITY (Overall)	FREQUENCY (MHz)
CLD: Clock with LVDS Comp. Output	A: 40/60 to 60/40% T: 45/55 to 55/45%	R: 0...+50 S: 0...+70 U: -20...+70 V: -40...+85	I: ±25 ppm H: ±50 ppm J: ±100 ppm	80.000...250.000

EXAMPLE: CLDPASH-155.520

Clock Oscillator, 7x5mm Package, +3.3 VDC Supply Voltage, LVDS Output, Standard Symmetry, 0...+70°C Operating Temperature Range, ±50 ppm Total Frequency Stability, 155.520 MHz

Please consult the factory for any custom requirements.

■ **MECHANICAL PARAMETERS:**

The image contains three main mechanical drawings of a clock component:

- Top View:** Shows a rectangular component with a small circle in the top-left corner labeled "INDICATES PIN 1". Dimensions include a width of 7.0 ± 0.2 and a height of 5.0 ± 0.2 . A specific feature is dimensioned as $1.97 \pm .008$ and another as $.276 \pm .008$.
- Side View:** Shows the profile of the component with a maximum height of $.079 \text{ MAX.}$ and a maximum thickness of 2.00 MAX.
- Pinout View:** Shows a top-down view of the six pins, numbered 1 through 6. Dimensions include a total width of 5.08 , a pin pitch of 1.00 (with a 2.54 spacing between pins 2 and 3), and a pin width of $.055 \text{ TYP.}$ with a 1.40 spacing between pins 1 and 2. Other dimensions include $.150$, 3.81 , and 1.27 .

SOLDER PATTERN: A separate drawing shows the layout for soldering the component. It features a central pad with a width of $.071$ and a length of 1.80 . The spacing between pads is 2.54 . The overall height of the solder pattern is $.087$ (with a 2.20 spacing between pads) and $.079 \text{ TYP.}$ (with a 2.00 TYP. spacing between pads).

OUTLINE TOLERANCE:
 $\pm 0.006'' / 0.15\text{mm}$
 (Unless otherwise specified)

PIN FUNCTIONS:
 [1] ENABLE/ DISABLE
 [2] NO CONNECT
 [3] CASE GROUND
 [4] OUTPUT
 [5] COMP. OUTPUT
 [6] SUPPLY VOLTAGE

MARKING:
 CLDASH
 155.52
 RAL D/C

***0.01mF external by-pass filter is recommended as seen on solder pattern.**