QLogic Corporation

FAS466 Fast Architecture SCSI Processor

Data Sheet

Features Summary

- Compliance with ANSI X3T10/855D SCSI configured automatically (SCAM) protocol levels 1 and 2
- Compliance with ANSI X3.131-1996 SCSI-3 parallel interface (SPI-2) standard
- Compliance with ANSI X3T10/1142D Fast-40 standard
- SCSI synchronous data transfer rates up to:
  - ❒ 80 Mbytes/sec (wide, 16-bit Fast-40)
  - ❒ 40 Mbytes/sec (narrow, eight-bit Fast-40)
- On-chip LVD (low voltage differential) drivers
- Versatile 40 million instructions per second (MIP) microcontroller
- Programmable microcontroller to automate SCSI protocol handling
- Programmable filtering on select SCSI signals
- Programmable slew-rate control
- Supports initiator and target modes
- DMA interface with late transfer tolerant design that provides 160 Mbytes/sec sustained transfers
- Expanded 128-word DMA FIFO
- On-chip phase lock loop (PLL) for high frequency clock synthesis

Product Description

The FAS466 incorporates an enhanced, high-performance SCSI engine derived from the QLogic TEC450/452 triple embedded controller family.

The FAS466 provides Fast-40 SCSI synchronous transfer rates. The highly integrated SCSI core provides advanced SCAM level 1 and level 2 support. The FAS466 includes a microcontroller that provides a flexible, programmable means to coordinate SCSI sequences.

The FAS466 supports single-ended and low-voltage differential SCSI mode operations in initiator and target modes. The FAS466 block diagram is shown in figure 1.

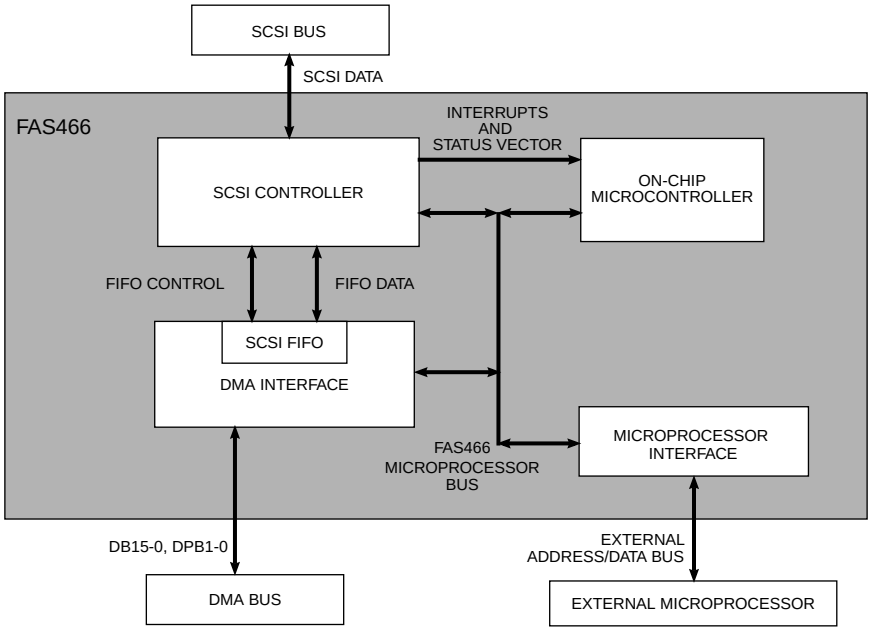

Figure 1. FAS466 Block Diagram

SCSI Controller

The following list highlights the FAS466 SCSI controller features.

- Asynchronous data transfers greater than 5 Mtransfers/sec
- Synchronous data transfers (5 Mtransfers/sec)
- Fast synchronous data transfers (10 Mtransfers/sec)
- Fast-20 synchronous data transfers (20 Mtransfers/sec)
- Fast-40 synchronous data transfers (40 Mtransfers/sec)
- 8-bit (narrow) and 16-bit (wide) SCSI bus widths
- SCAM levels 1 and 2

The SCSI controller provides powerful and flexible low-level hardware assistance for SCSI protocol handling. The FAS466 microcontroller, SCSI FIFO, and SCSI controller perform frequently used SCSI operations with low firmware overhead at performance levels ranging from asynchronous SCSI to Fast-40.

The core of the FAS466 SCSI processor, with enhanced initiator support, is derived from the proven TEC452 SCSI disk controller.

Microcontroller

The following list highlights the FAS466 SCSI microcontroller features.

- Maximum 40 MIPS with a 25-ns instruction cycle (except for branch)
- 64 single-word instructions
- 16-bit wide instructions
- Eight-bit wide data path
- 1024x16 static random access memory (SRAM) program memory
- 16x8 dual-port, general purpose registers; 32 mailbox registers
- Five-level deep hardware stack
- Direct, indirect, and absolute addressing modes
- Two firmware interrupt sources
- Two hardware interrupts; one with four-bit, automatic interrupt vector and status
- Full chip access through the microprocessor bus

The FAS466 provides a microcontroller with separate program and data memory. The result is improved bandwidth over traditional Von Neuman architecture where program and data share the same memory. Separating program and data memory allows independent widths for instruction and data. All instructions are 16 bit wide, single-word.

The four operations for each instruction cycle are fetch, decode, execute, and write back. A three-stage pipeline allows overlaps between fetch and write-back cycles with decode and execute cycles. Consequently, all instructions execute in one instruction cycle or two clock periods (25 ns at 80 MHz) except for program branches, which require two instruction cycles.

The microcontroller is composed of a 1024x16 program memory, a 32x8 register file, a 5x8 stack, an integer ALU, 32 mailbox registers, and other special purpose registers. The microcontroller has direct access to addresses in the register files or in data memory. The first 16 bytes of the external SCSI FIFO is mapped directly into data memory locations 90h-9Fh. The microcontroller can monitor the FIFO contents (one byte at a time) without removing it. The microcontroller accesses external registers through the external access read (EARD) instruction or the external access write (EAWR) instruction.

DMA Interface

The FAS466 has an improved DMA interface with an expanded 128-word FIFO that provides transfer rates up to 160 Mbytes/sec. The FAS466 supports 16-bit wide data strobe transfers of up to 80 MHz with 160 Mbytes/sec data throughput. The internal FIFO provides programmable threshold logic for determining FIFO full and empty conditions.

Microprocessor Interface

The FAS466 microprocessor interface provides the interface between the internal modules (SCSI controller, FIFO, microcontroller, and DMA engine) and an external microprocessor.

Interfaces

The FAS466 interfaces consist of SCSI, microprocessor, DMA, and differential mode support. Pins that support these interfaces and other chip operations are shown in figure 2.

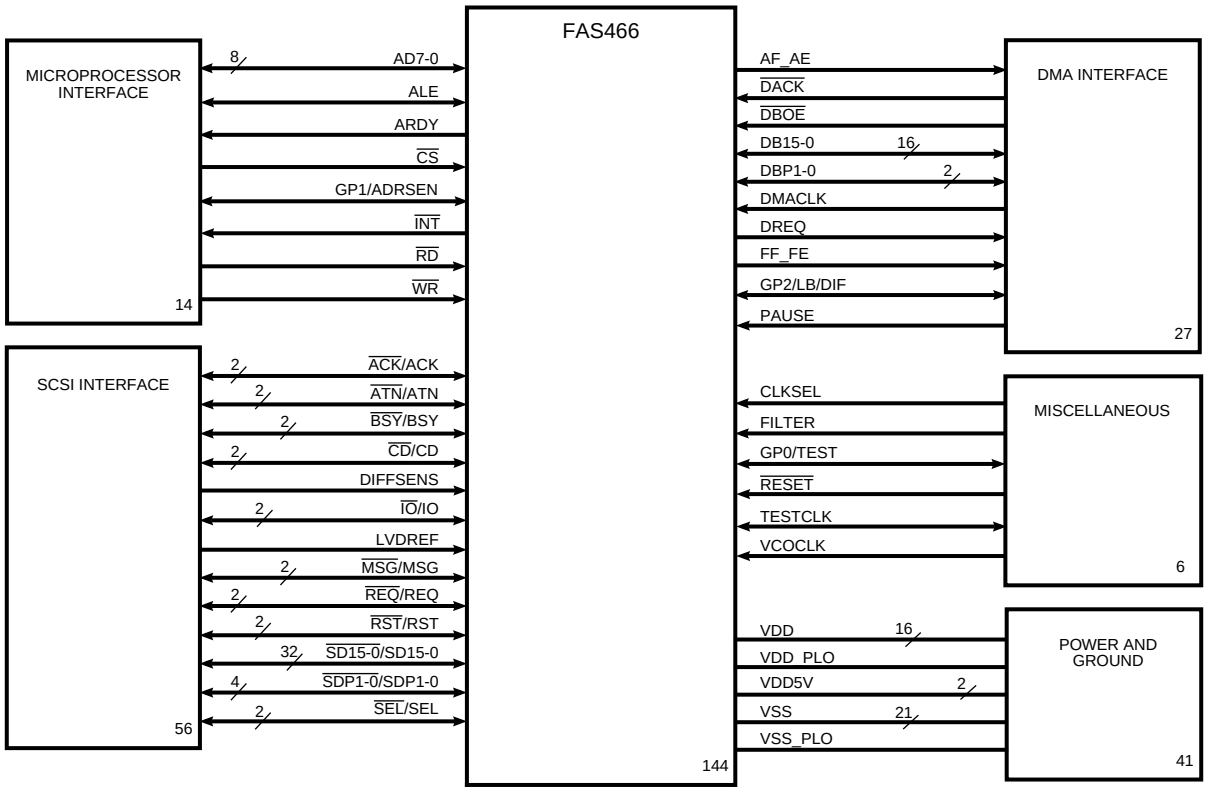

Figure 2. FAS466 Functional Signal Grouping

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