# DUAL-GATE UNIDIRECTIONAL OVERVOLTAGE PROTECTOR

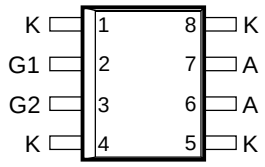
 FEBRUARY 1999

## OVERVOLTAGE PROTECTION FOR DUAL-VOLTAGE RINGING SLICS

- **Programmable Protection Configurations up to ±100 V**
- **Typically 5 Lines Protected by Two TISP83121D + Diode Steering Networks**
- **High Surge Current**
  - **150 A 10/1000 µs**
  - **150 A 10/700 µs**
  - **500 A 8/20 µs**
- **Pin compatible with the LCP3121**
  - **Functional Replacement in Diode Steering Network Applications**
  - **50% more surge current**
- **Small Outline Surface Mount Package**
  - **Available Ordering Options**

| CARRIER | PART # |
|---|---|
| Tube | TISP83121D |
| Taped and reeled | TISP83121DR |

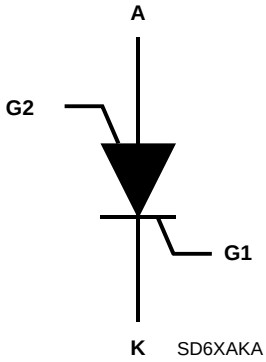
**D PACKAGE**
**(TOP VIEW)**




MD6XAYA

For operation at the rated current values connect pins 1, 4, 5 and 8 together.

## device symbol




SD6XAKA

## description

The TISP83121D is a dual-gate reverse-blocking unidirectional thyristor designed for the protection of dual-voltage ringing SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction.

The device chip is a four-layer NPNP silicon thyristor structure which has an electrode connection to every layer. For negative overvoltage protection the TISP83121D is used in a common anode configuration with the voltage to be limited applied to the cathode (K) terminal and the negative reference potential applied to the gate 1 (G1) terminal. For positive overvoltage protection the TISP83121D is used in a common cathode configuration with the voltage to be limited applied to the anode (A) terminal and the positive reference potential applied to the gate 2 (G2) terminal.

The TISP83121D is a unidirectional protector and to prevent reverse bias, requires the use of a series diode between the protected line conductor and the protector. Further, the gate reference supply voltage requires an appropriately poled series diode to prevent the supply from being shorted when the TISP83121D crowbars.

Under low level power cross conditions the TISP83121D gate current will charge the gate reference supply. If the reference supply cannot absorb the charging current its potential will increase, possibly to damaging levels. To avoid excessive voltage levels a clamp (zener or avalanche breakdown diode) may be added in shunt with the supply. Alternatively, a grounded collector emitter-follower may be used to reduce the charging current by the transistors $H_{FE}$ value.

This monolithic protection device is made with a ion-implanted epitaxial-planar technology to give a consistent protection performance and be virtually transparent to the system in normal operation.

## absolute maximum ratings

| RATING | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Repetitive peak off-state voltage, 0 °C to 70 °C | $V_{DRM}$ | 100 | V |
| Non-repetitive peak on-state pulse current (see Notes 1 and 2) | | | |
| 10/1000 µs (GR-1089-CORE, open-circuit voltage wave shape 10/1000 µs) | $I_{TSP}$ | 150 | A |
| 5/310 µs (CCITT K20/21, open-circuit voltage wave shape 7 kV10/700 µs) | | 150 | |
| 8/20 µs (ANSI C62.41, open-circuit voltage wave shape 1.2/50 µs) | | 500 | |
| Non-repetitive peak on-state current, 50 Hz, halfwave rectified sinewave, (see Notes 1 and 2) | | | |
| 100 ms | $I_{TSM}$ | 22 | A |
| 1 s | | 8 | |
| 900 s | | 3 | |
| Junction temperature | $T_J$ | -40 to +150 | °C |
| Storage temperature range | $T_{stg}$ | -65 to +150 | °C |

NOTES: 1. Initially the protector must be in thermal equilibrium with 0 °C < $T_J$ < 70 °C. The surge may be repeated after the device returns to its initial conditions. For operation at the rated current value, pins 1, 4, 5 and 8 must be connected together.
2. Above 70 °C, derate linearly to zero at 150 °C lead temperature.

## electrical characteristics, $T_J$ = 25 °C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_D$ | Off-state current | $V_d$ = 70 V, $I_G$ = 0 | | | | 1 | µA |
| $I_{DRM}$ | Repetitive peak off-state current | $V_d = V_{DRM}$ = 100 V, $I_G$ = 0, 0 °C to 70 °C | | | | 10 | µA |
| $I_H$ | Holding current | $I_T$ = 1 A, di/dt = -1A/ms | $T_J$ = 0 to 70 °C | | | 300 | mA |
| | | | $T_J$ = 25 °C | 90 | | | |
| | | | $T_J$ = 70 °C | 60 | | | |
| $I_R$ | Reverse current | $V_R$ = 0.3 V | | | | 1 | mA |
| $I_{G1T}$ | Gate G1 trigger current | $I_T$ = +1 A, $t_{p(g)}$ = 20 µs | | | | +200 | mA |
| $I_{G2T}$ | Gate G2 trigger current | $I_T$ = +1 A, $t_{p(g)}$ = 20 µs | | | | -180 | mA |
| $V_{G1T}$ | G1-K trigger voltage | $I_T$ = +1 A, $t_{p(g)}$ = 20 µs | | | | +1.8 | V |
| $V_{G2T}$ | G2-A trigger voltage | $I_T$ = +1 A, $t_{p(g)}$ = 20 µs | | | | -1.8 | V |
| $C_{AK}$ | Anode to cathode off-state capacitance | f = 1 MHz, $V_d$ = 1 $V_{RMS}$, $V_D$ = 5 V, $I_G$ = 0 (see Note 3) | | | | 100 | pF |

NOTE 3: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are decoupled to the guard terminal of the bridge.

## thermal characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction to free air thermal resistance | $T_A$ = 25 °C, EIA/JESD51-3 PCB, EIA/JESD51-2 environment, $I_T = I_{TSM(900)}$ | | | 105 | °C/W |

## PARAMETER MEASUREMENT INFORMATION

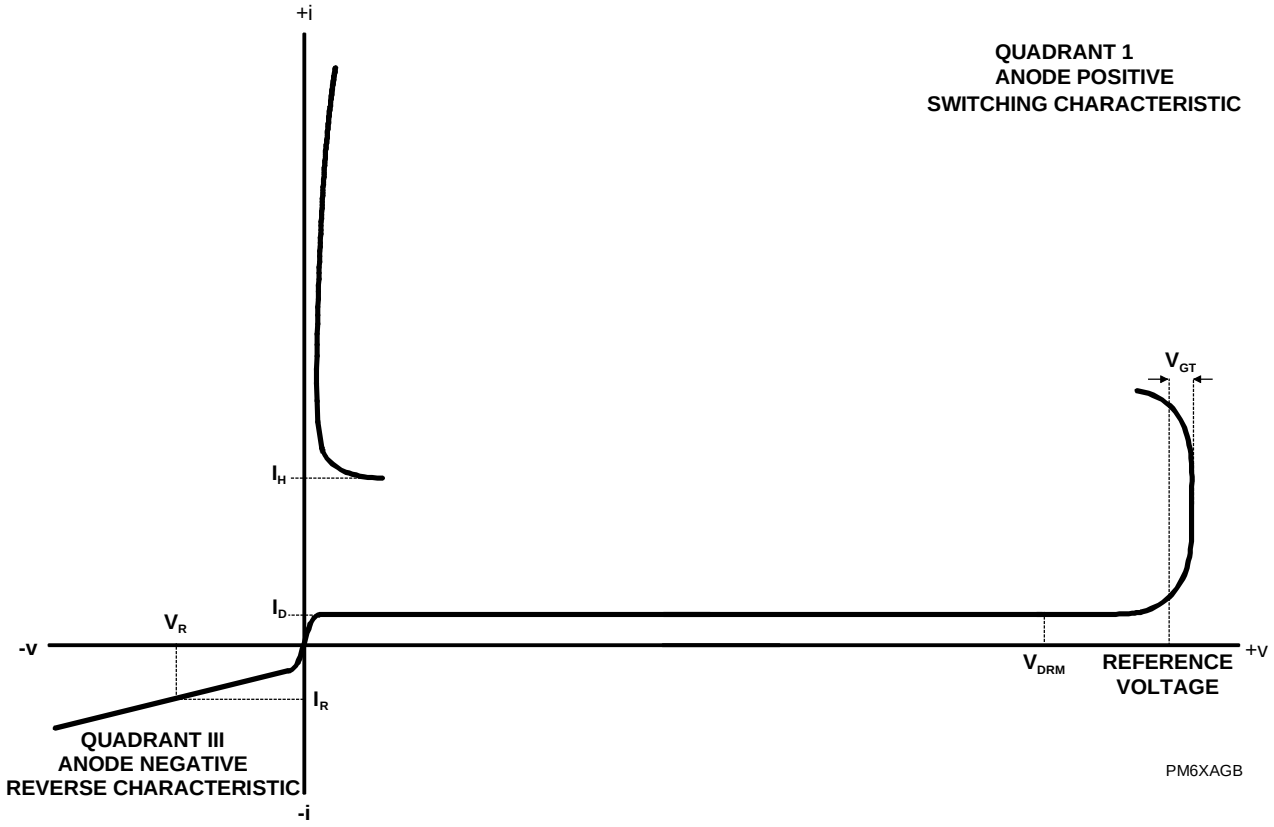



**Figure 1. VOLTAGE-CURRENT CHARACTERISTIC**

### multiple line overvoltage protection

Figure 2 shows two TISP83121D devices protecting many lines. Line conductor positive overvoltage protection is given by the steering diode array connected to the anode of the upper TISP83121D and the TISP83121D itself. The TISP83121D gate reference voltage is the positive battery supply, $+V_{BAT}$. The initial limiting voltage will be the sum of the voltages of the battery, the forward biased conductor diode, the gate trigger of the TISP83121D and the forward biased reference voltage blocking diode. Typically the conductor voltage will be initially limited at 2.5 V above the $+V_{BAT}$ value.

Line conductor negative overvoltage protection is given by the diode steering array connected to the cathode of the lower TISP83121D and the TISP83121D itself. The TISP83121D gate reference voltage is the negative battery supply, $-V_{BAT}$. The initial limiting voltage will be the sum of the voltages of the battery, the forward biased conductor diode, the gate trigger of the TISP83121D and the forward biased reference voltage blocking diode. Typically the conductor voltage will be initially limited at 2.5 V below the $-V_{BAT}$ value.

When an TISP83121D crowbars and grounds all conductors of the appropriate polarity, the device current will be the sum of all the SLIC output currents. This will usually exceed the TISP83121D holding current. To switch off the TISP83121D and restore normal operation, the grounded condition of the SLIC output must be detected and the SLIC outputs turned off.

The 150 A rating of the TISP83121D allows a large number of lines to be protected against currents caused by lightning. For example, if a recommendation K.20 10/700 generator was connected to all lines, together

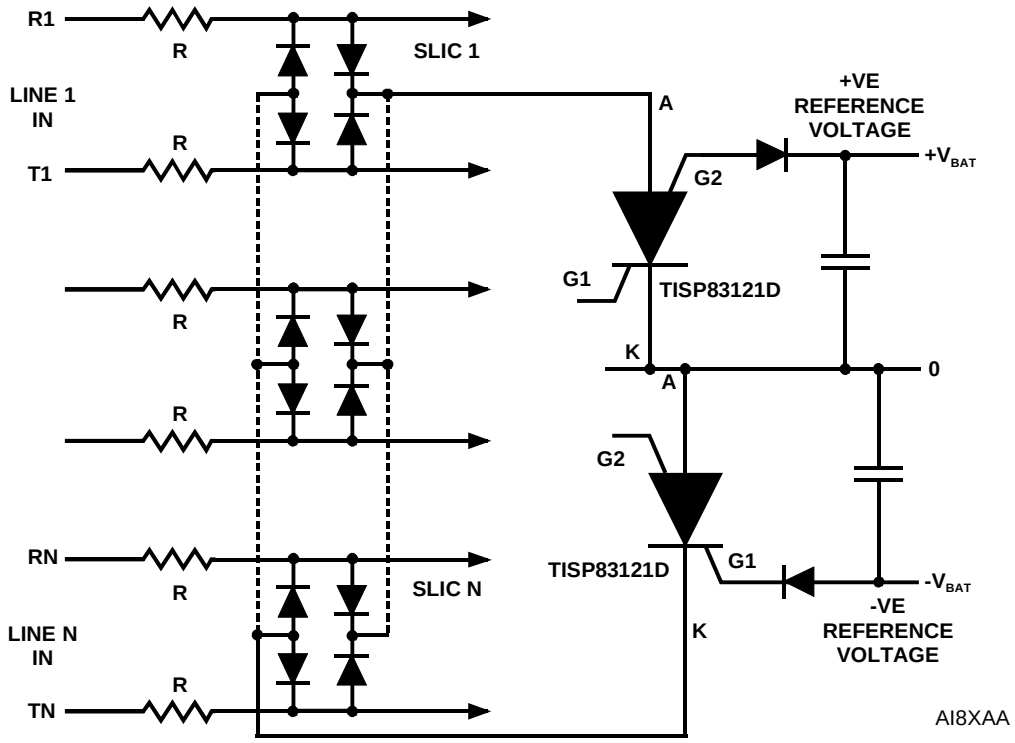



**Figure 2. N LINE POSITIVE AND NEGATIVE OVERVOLTAGE PROTECTION**

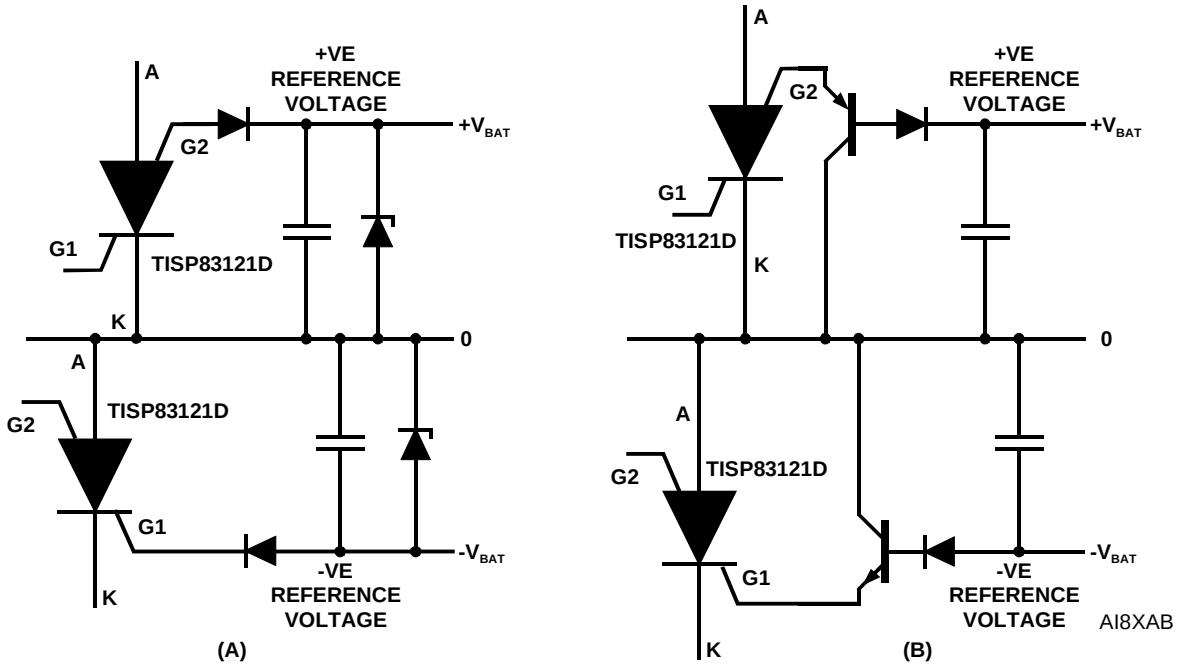



**Figure 3. REFERENCE VOLTAGE CONTROL BY (A) BREAKDOWN DIODES OR (B) BY TRANSISTOR BUFFERS**

with 350 V primary protection and a series conductor resistance (R) of 25 Ω, the maximum conductor current before the primary protection operated would be 350/25 = 14 A or 28 A per line. For a total return current of about 150 A the number of lines would be 150/28 = 5. At this current level, 5x28 = 140 A, the generator

voltage would be 140((25+25)/10+15) = 2800 V. Another limitation is long term power cross. The long term power cross capability of the TISP83121D is 3 A peak or 2.1 A rms. If the line conductor overcurrent protection was given by a PTC resistor which switched at 0.2 A, the maximum number of conductors becomes 2.1/0.2 = 10 or 5 lines.

### battery supply impedance

In many designs, the battery supply voltages are generated by switching mode power supplies. This type of power supply cannot be charged like a battery. Feeding a charging current to a switching mode power supply will usually cause the supply to stop switching and the voltage to rise. The gate current of the TISP83121D is a charging current for the supply. To avoid the supply voltage from rising and damaging the connected SLICs, an avalanche diode voltage clamp can be connected across the supply (Figure 3. (A)).

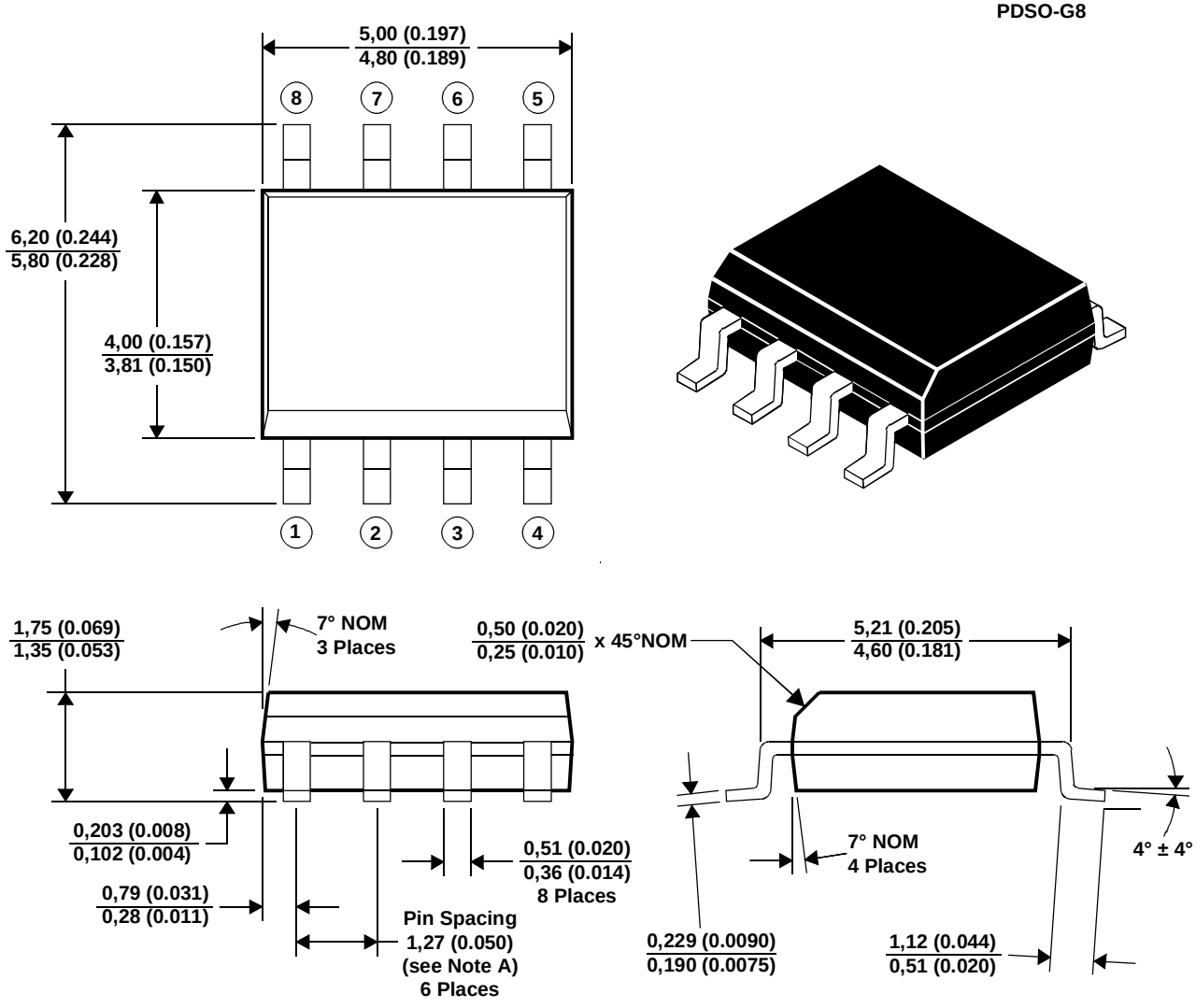
Another approach is to reduce the gate charging current for the supply by a transistor buffer (Figure 3. (B)). If the transistor gain was 50, a 200 mA gate current would be reduced to a supply charging current of 200/50 = 4 mA  In both cases, the dissipation in the control devices can be substantial and power capability needs to be taken into account in device selection.

## MECHANICAL DATA

### D008

### plastic small-outline package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.




MDXXAA

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002).

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