Advanced Computing

# VAS96031 Pier39

## PCI to Mac I/O Bridge Controller for PowerPC Common Platform

### OVERVIEW

Pier39 is a highly integrated, cost-effective bridge controller specifically designed for your high performance PowerPC Platform-based computers. It is a simple direct drop-in solution to the existing PowerPC Platform systems. Pier39 is pin-to-pin Compatible to the Apple Hydra I/O controller which is used in Apple RISC machines with a PCI bus. Pier39 implements a full set of the Apple Hydra function including the ADB interface, the MPIC multi-processor interrupt controller and much more.

Pier39 Connects to the host via the PCI bus. PCI provides an inexpensive and moderately high performance interconnect for I/O devices.

It is a 32-bit, multiplexed address/data bus, running at 33 MHz. PCI implementation of Pier39 is compliant with v2.0 of the PCI specification.

The Pier39 Controller functions are very flexible to the users design needs. Most of its functions such as timing, resource selections, .etc are programmable via a set of internal device specific configuration registers.

### FEATURES

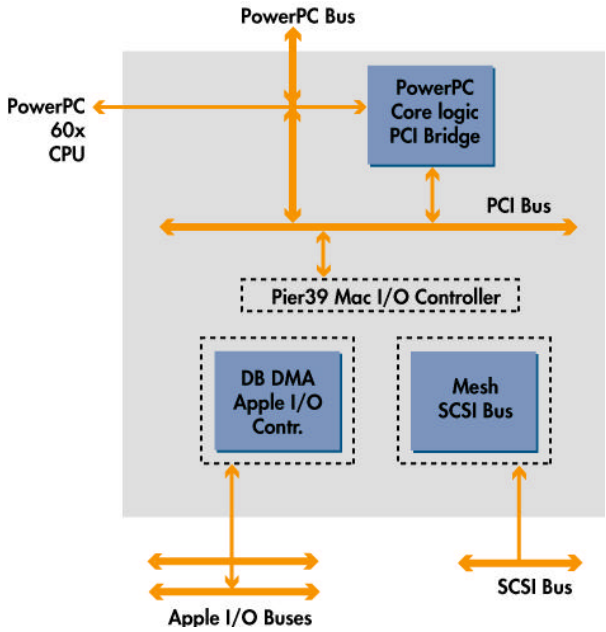
- Allows up to 33 MHz PCI Bus interface
- Supports PCI master and slave transactions
- Compliant with v2.0 of the PCI specification
- Integrated SCSI controller implemented using Mesh
- Integrated 85C30 SCC cell which supports GeoPort™ and has additional support for LocalTalk
- Integrated VIA cell
- Built in 5 channel DB-DMA controller performs scatter/gather transfers, based on a buffer list in main memory
- ADB hardware interface
- Sleep mode for reduced power
- MPIC interrupt controller which supports 2 processors
- 0.6-micron CMOS technology
- 160 pins MQFP (Metric Quad Flat Pack)
- Easy integration into PowerPC Common Platform Roadmap

### SPECIFICATIONS

#### PCI Interface

This block acts both as a master, and a slave on the PCI bus. As a slave, it decodes and responds to accesses to registers within the I/O controllers as well as registers within the DB-DMA controller. As a master, it acts on behalf of the DB-DMA controller to generate transactions on the PCI bus. These transactions are used to move streams of data between system memory and the devices, as well as to read and write the DB-DMA command lists.

## Block Diagram



## DB-DMA Controller

This module is responsible for supplying the addresses associated with all of the data transfers initiated by Pier39. The DB-DMA controller is capable of sequencing through buffer descriptor lists stored in main memory in order to find the next buffer address after a channel exhausts the previous buffer. This frees the system from stringent interrupt response requirements after buffer transfer completes. The DB-DMA controller contains a register file which stores the current channel program pointers for each of the 5 DB-DMA channels. Another register file stores the current context (address, count and flags) for each of the channels. A single 32-bit incrementer updates both the Channel Program Pointers, and the current buffer pointers. A common 16-bit decrementer is used to adjust the count values for all of the channels. The DB-DMA controller arbitrates data transfer requests from each of the IO modules, and generates PCI transactions which read and write the data buffers, as well as the channel program entries.

SCSI Controller Pier39 integrates the Mesh SCSI controller. A single DB-DMA channel is used to support the data transfers. The SCSI controller's register set is mapped into the host processor's address space.

## SCC

Pier39 integrates an SCC cell (Z85C30 compatible). The SCC is also used to drive the GeoPort™ Telecom interface. External GeoPort™ compatible parts are used to drive and receive the serial lines for both SCC ports. Four DB-DMA channels are used to support simultaneous transmission and reception on both of the SCC's serial ports. The SCC's register set is mapped into the host processor's address space. When performing register accesses, the Pier39 hardware ensures that the "recovery" time of the SCC is satisfied.

## VIA

To improve system compatibility, the VIA functionality is implemented. This interface is quite primitive, and no DB-DMA support is provided.

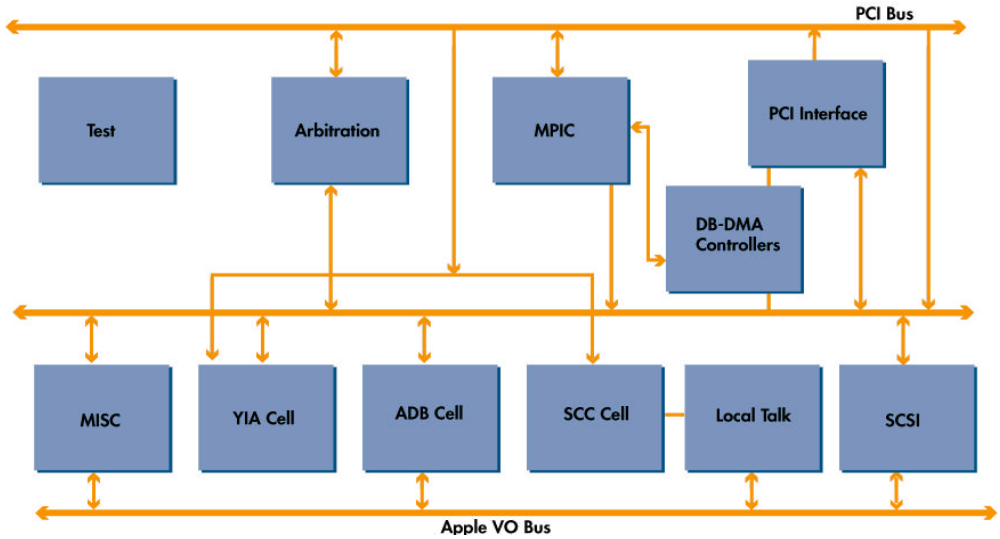
## ADB

The ADB cell in Pier39 is a full feature hardware implementation of the master controller for the Apple Desktop Bus. The ADB cell is designed to relieve the CPU from the tedious time consuming tasks associated with performing ADB functions. The ADB cell performs all ADB Master functions, including Auto-polling and SRQ Auto-polling with error recovery. The ADB cell also implements keyboard invoked RESET and NMI.

## MPIC

Pier39 integrates the MPIC interrupt controller which is compliant with OpenPIC standard v1.2. The MPIC register set is mapped into the host processor's address space. The MPIC inside Pier39 can be disabled if an external interrupt controller is used.

# Typical Application






VLSI Technology

VLSI Technology, Inc.
1109 McKay Drive
San Jose, CA 95131