dvanced Computing

VAS96011/VAS96012 PowerPC System Controller



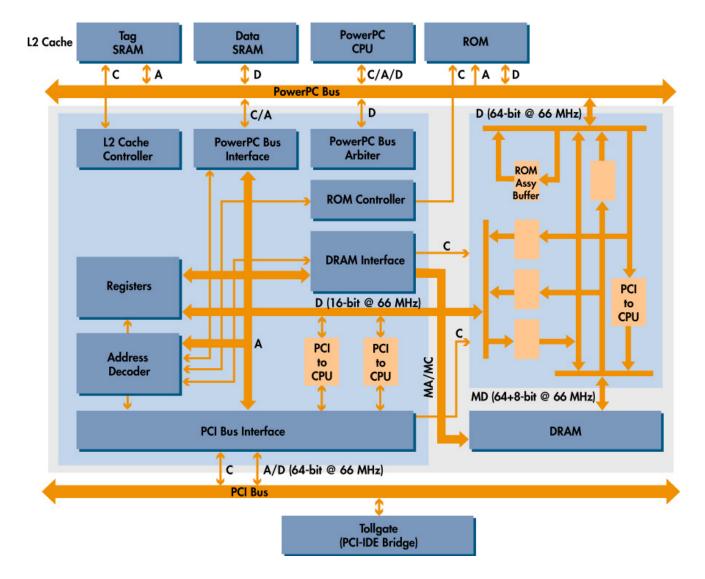
O V E R V I E W

VLSI's VAS96011/2 is a cost-effective core logic solution for CHRP PowerPC platforms. The dual-chip solution integrates system control logic and provides a logical connection between the PowerPC microprocessor and the PCI bus. VAS96011/2 enable glueless connection to the PowerPC processor, secondary cache, system memory, ROM and the PCI bus. This significantly

reduces overall system cost and footprint. The VAS96011's system memory controller supports a variety of memory types and configurations. The integrated secondary (L2) cache controller supports programmable copy back and write through modes. Caching and shadowing of the ROM contents are also supported to significantly enhance ROM access performance under MacOS.

The 32-bit PCI bus interface is operational up to 33 MHz, with programmable option to run synchronously with or independent of the CPU bus clock. All PCI bus master accesses to main memory are snooped. VAS96011 contains system control logic, CPU address path and PCI interface. VAS96012 is a 3-way, 64-bit wide data path to the CPU, system memory and VAS96011.

<u>Block Diagram</u>



FEATURES

- CHRP-compliant PowerPC system controller
- Highly integrated dual-chip solution
 - · VAS96011: Address path and system controller (240 MQFP)
 - · VAS96012: Data path controller (208 MQFP)
- High performance 64-bit, 66 MHz PowerPC CPU interface
 - · Supports PowerPC 603 and 604 processor families
- Integrated Phase-Locked Loop
- Secondary look-aside cache controller
 - Configurable for copy-back or write-through operation with direct-mapped organization
 - · Cache sizes of 256 KB, 512 KB, 1 MB
 - · Supports synchronous pipelined burst SRAM
 - · Supports COASt 3.0 cache module

- · Integrated tag comparator
- Caches ROM for improved ROM access performance
- Integrated DRAM controller
 - Supports Synchronous DRAM (SDRAM), FPM-, EDO-, and BEDO-DRAM
 - · 64-bit memory organization
 - · Addressable up to six 64-bit banks
 - · Glue-less connection of up to three 64-bit banks
 - Supports 1 MB x 4, 16 MB x 1,
 4 MB x 4, 2 MB x 8, 16 MB x 4,
 and 8 MB x 8 DRAMs
- Supports symmetrical and asymmetrical DRAM addressing
- · Programmable access timing
- Integrated ROM interface controller
 - · Supports 2 independent ROM banks
 - Supports burst cache line-fill transactions from ROM and flash ROM writes

- Option to boot from PCI-based ROM
- · ROM shadowing in system memory
- Integrated PCI interface controller
 - · Compliant with PCI 2.1 specification
 - · Concurrent operation of PowerPC and PCI buses
 - Up to 33 MHz PCI bus operation with optional synchronization to the PowerPC bus
- Prefetching (32 bytes) of PCI reads from system memory and of PowerPC reads from PCI slaves
 - · Write FIFOs for writes from a PCI master to system memory (64 bytes)
 - Supports big- and little-endian PCI modes
 - · Configuration support (IDSEL) for up to 15 external PCI devices
 - · 3.3 V with 5 V-tolerant PCI pads
- 3.3V, 0.5µm technology

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VLSI Technology, Inc. 1109 McKay Drive San Jose, CA 95131