

FEATURES

- **CHRP-compliant PowerPC system controller**
- **Highly integrated dual-chip solution**
 - VAS96011: Address path and system controller (240 MQFP)
 - VAS96012: Data path controller (208 MQFP)
- **High performance 64-bit, 66 MHz PowerPC CPU interface**
 - Supports PowerPC 603 and 604 processor families
- **Integrated Phase-Locked Loop**
- **Secondary look-aside cache controller**
 - Configurable for copy-back or write-through operation with direct-mapped organization
 - Cache sizes of 256 KB, 512 KB, 1 MB
 - Supports synchronous pipelined burst SRAM
 - Supports COAST 3.0 cache module
- **Integrated tag comparator**
- **Caches ROM for improved ROM access performance**
- **Integrated DRAM controller**
 - Supports Synchronous DRAM (SDRAM), FPM-, EDO-, and BEDO-DRAM
 - 64-bit memory organization
 - Addressable up to six 64-bit banks
 - Glue-less connection of up to three 64-bit banks
 - Supports 1 MB x 4, 16 MB x 1, 4 MB x 4, 2 MB x 8, 16 MB x 4, and 8 MB x 8 DRAMs
 - Supports symmetrical and asymmetrical DRAM addressing
 - Programmable access timing
- **Integrated ROM interface controller**
 - Supports 2 independent ROM banks
 - Supports burst cache line-fill transactions from ROM and flash ROM writes
- **Option to boot from PCI-based ROM**
- **ROM shadowing in system memory**
- **Integrated PCI interface controller**
 - Compliant with PCI 2.1 specification
 - Concurrent operation of PowerPC and PCI buses
 - Up to 33 MHz PCI bus operation with optional synchronization to the PowerPC bus
- **Prefetching (32 bytes) of PCI reads from system memory and of PowerPC reads from PCI slaves**
 - Write FIFOs for writes from a PCI master to system memory (64 bytes)
 - Supports big- and little-endian PCI modes
 - Configuration support (IDSEL) for up to 15 external PCI devices
 - 3.3 V with 5 V-tolerant PCI pads
- **3.3V, 0.5µm technology**

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