DATA SHEET

UAA3580
Wideband code division multiple access frequency division duplex zero IF receiver

Objective specification
Supersedes data of 2002 Oct 16

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Philips
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Wideband code division multiple access frequency division duplex zero IF receiver

UAA3580

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Wideband code division multiple access frequency division duplex zero IF receiver

UAA3580

1 FEATURES

- Low noise wide dynamic range for zero IF receivers
- 79 dB gain control range; in steps of 1 dB
- Channel filters
- 96 dB voltage gain
- Fully integrated fractional-N synthesizer with AFC control capability
- Fully integrated RF VCO with integrated supply voltage regulator
- Fully differential design to minimize crosstalk
- Supply voltage from 2.4 to 3.3 V
- 3-wire serial interface bus
- HVQFN24 package.

2 APPLICATIONS

- WCDM-FDD receiver for GSM hand-portable equipment
- Dual mode GSM/GPRS/EDGE/UMTS handset.

3 GENERAL DESCRIPTION

The UAA3580 is a BiCMOS integrated circuit receiver intended for the Third Generation Partnership Project (3GPP) specification for the Universal Mobile Telecommunication System (UMTS).

The circuit is specially designed for the Frequency Division Duplex (FDD) mode of the Wide Code Division Multiple Access (WCDMA) that operates in the 2110 to 2170 MHz band.

The UAA3580 contains the whole analog receive chain from Radio Frequency (RF) Low Noise Amplifier (LNA) to baseband IQ outputs including a channel filter, a complete RF Phase-Locked Loop (PLL) with a fully integrated Voltage Controlled Oscillator (VCO), and a clock PLL that generates a programmable UMTS system clock from an external 26 MHz reference signal.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	2.6	–	3.3	V
V_{DDD}	digital supply voltage	1.6	–	2.8	V
T_{amb}	ambient temperature	–30	–	+70	°C

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		VERSION
	NAME	DESCRIPTION	
UAA3580HN	HVQFN24	plastic, heatsink very thin quad flat package; no leads 24 terminals; body $4 \times 4 \times 0.90$ mm	SOT616-1

6 BLOCK DIAGRAM

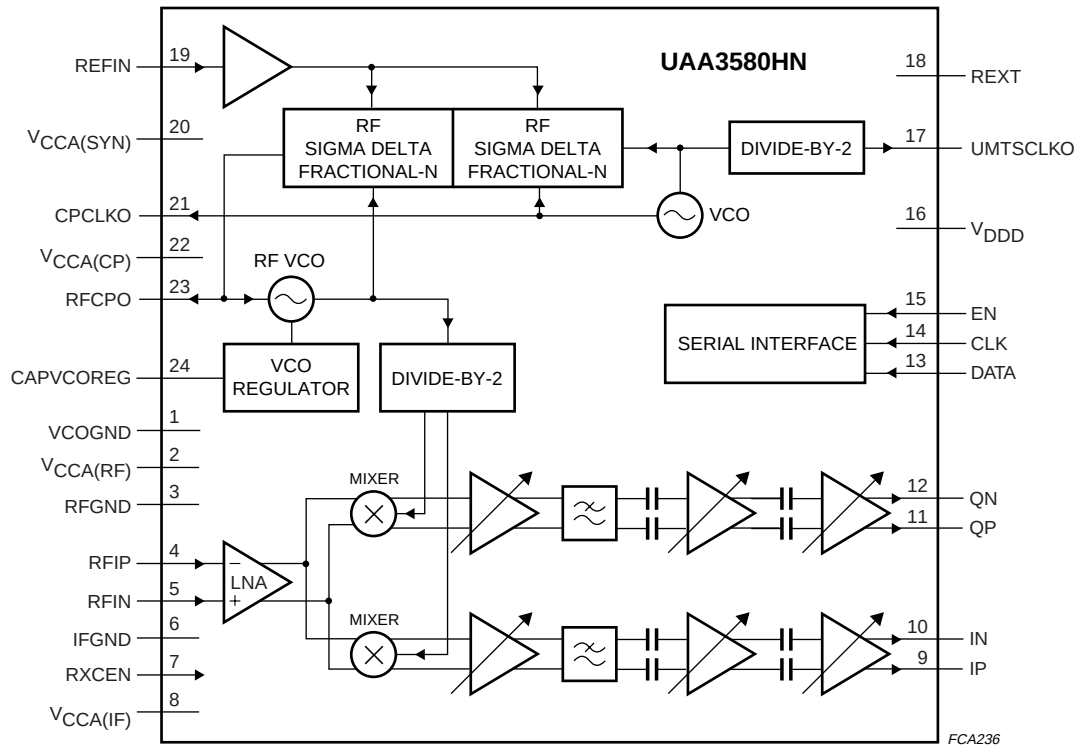


Fig.1 Block diagram.

7 PINNING INFORMATION

7.1 Pinning

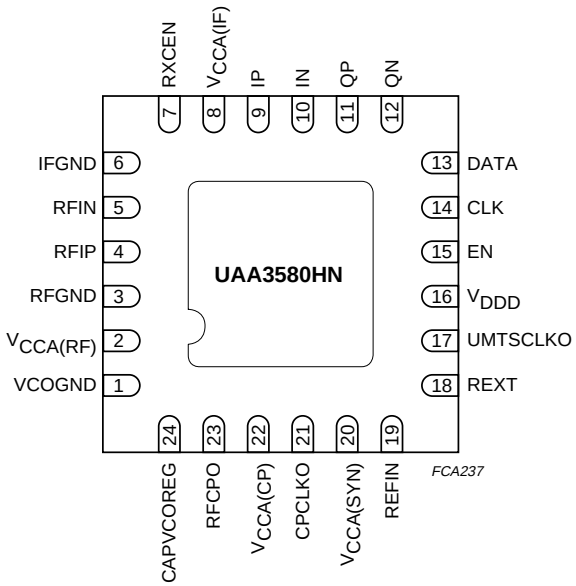


Fig.2 Pin configuration.

7.2 Pin description

Table 1 HVQFN24 package

SYMBOL	PIN	DESCRIPTION
VCOGND	1	RF VCO ground
$V_{CCA(RF)}$	2	analog supply voltage for the RF receiver
RFGND	3	RF receiver ground
RFIP	4	RF positive input
RFIN	5	RF negative input
IFGND	6	IF section ground
RXCEN	7	receiver chip enable input
$V_{CCA(IF)}$	8	analog supply voltage for the IF section
IP	9	differential receive baseband positive in-phase output
IN	10	differential receive baseband negative in-phase output
QP	11	differential receive baseband positive in-quadrature output
QN	12	differential receive baseband negative in-quadrature output
DATA	13	serial bus data input
CLK	14	serial bus clock input
EN	15	serial bus enable input
V_{DDD}	16	digital supply voltage
UMTSCLKO	17	UMTS system clock output
REXT	18	external charge pump biasing resistor connection
REFIN	19	reference clock input
$V_{CCA(SYN)}$	20	analog supply voltage for the synthesizer
CPCLKO	21	charge pump clock output
$V_{CCA(CP)}$	22	analog supply voltage for the charge pump section
RFCPO	23	RF charge pump output
CAPVCOREG	24	decoupling capacitor for the VCO regulator
	die pad	ground

8 FUNCTIONAL DESCRIPTION

The receiver consists of an RF receiver front-end, an RF VCO, a channel filter, Automatic Gain Control (AGC), a RF fractional-N synthesizer PLL, a clock PLL, a Power-up reset circuit and a 3-wire serial programming bus.

8.1 RF receiver front-end and RF VCO

The front-end receiver converts the aerial RF signal from WCMDA (2.11 to 2.17 GHz) band down to a Zero Intermediate Frequency (ZIF). The first stage is a differential low noise amplifier matched to 50 Ω using an external balun. The LNA is followed by an IQ down-mixer which consists of two mixers in parallel but driven by quadrature out-of-phase LO signals. The In phase (I) and Quadrature phase (Q) ZIF signals are then low-pass filtered, to provide protection from high frequency offset interference, and fed into the channel filter.

8.2 Channel filter and AGC

The front-end zero IF I and Q outputs are applied to the integrated low-pass channel filter with a provision for 4×8 dB gain steps in front of the filter. The filter is a self-calibrated fifth-order low-pass filter with a cut-off frequency around 2.4 MHz. Once filtered the zero IF I and Q outputs are further amplified with provision for 47×1 dB steps and DC offset compensation. The zero IF output buffer provides close rail-to-rail output signal.

8.3 RF VCO

The RF VCO is fully integrated and self-calibrated on manufacturing tolerances. It consists of 16 different frequency ranges that are selected internally, depending on the frequency programmation. It covers the necessary bandwidth of 4.22 to 4.34 GHz and is tuned via the RF charge pump and external loop filter. An internal supply voltage regulator using the pin CAPVCOREG as external decoupling capacitor supplies the RF VCO and minimizes parasitic coupling and pushing. The regulator and the RF VCO are turned on by the RXCEN signal.

8.4 RF LO section

The RF LO section covering the 4.22 to 4.34 GHz band is driven by the internal RF VCO module. It includes the LO buffering for the RF PLL and a divide-by-two circuit to generate the quadrature LO signals to drive the RX IQ down-mixer.

8.5 RF fractional-N synthesizer PLL

A high performance RF fractional-N synthesizer PLL is included on-chip which enables the frequency of the RF VCO to be synthesized. The frequency is set via the 3-wire serial programming bus.

The PLL is based on Sigma-Delta ($\Sigma\Delta$) fractional-N synthesis that enables the required channel frequency, including Automatic Frequency Control (AFC) from a free running external 26 MHz GSM reference frequency, to be obtained. Very low close in-phase noise is achieved which allows a wider PLL loop bandwidth and a shorter settling time. The programmable main dividers are controlled by a second-order ($\Sigma\Delta$) modulus controller. They divide the RF VCO signals down to frequencies of 26 MHz (in programmable 12 Hz steps). Their phase is then compared in a digital Phase/Frequency Detector (PFD) to the 26 MHz reference clock signal. The phase error information is fed back to the RF VCO via the charge pump circuit that ‘sources’ into or ‘sinks’ current from the loop filter capacitor, thus changing the VCO frequency so that the loop is finally brought into phase-lock.

The RF synthesizer division range enables an external reference frequency of 13 to 26 MHz to be used.

8.6 Clock PLL

The clock PLL is based on SD fractional-N synthesis that allows the UMTS system clock, including AFC from a non-corrected external 26 MHz GSM reference frequency, to be obtained. The PLL comprises a fully integrated RC VCO. The PLL output is a low harmonic content waveform, the frequency of which can be programmed to 15.36, 30.72 or 61.44 MHz. The default value is 30.72 MHz.

8.7 Control

The control of the chip is done via the 3-wire serial bus and pin RXCEN. At power-up the clock PLL section is automatically enabled, the other sections are enabled when the RXCEN signal is set HIGH (also via the 3-wire bus). The power-up signal is detected on pin V_{DDD} when the voltage rises. The V_{DDD} pin, if the supply voltage is maintained, enables the programming parameters to be retained in memory.

9 OPERATING MODES

9.1 Basic operating modes

The circuit can be powered up into different operating modes, depending on the control bits RXON and SYNON, via the 3-wire bus. This defines three main modes called IDLE, SYN and RX mode.

The voltage level applied to pin RXCEN must be set HIGH to enable the device. The VCO and the PLL sections are enabled in SYN mode. In the RX mode every section is enabled (receive part, VCO and PLL sections).

Table 2 Selection of operating mode

MODE	SYNON	RXON
IDLE	0	0
SYN	1	0
RX	1	1

9.2 AGC gain look-up table

The AGC gain is set via the AGC[8:0] bits; see Table 3.

Table 3 AGC gain look-up table

AGC8	AGC7	AGC6	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0	ATTENUATION FROM MAXIMUM GAIN (dB)
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	0	1	2
1	1	1	1	1	1	1	0	0	3
1	1	1	1	1	1	0	1	1	4
1	1	1	1	1	1	0	1	0	5
1	1	1	1	1	1	0	0	1	6
1	1	1	1	1	1	0	0	0	7
1	1	1	1	1	0	1	1	1	8
1	1	1	1	1	0	1	1	0	9
1	1	1	1	1	0	1	0	1	10
1	1	1	1	1	0	1	0	0	11
1	0	1	1	1	1	0	1	1	12
1	0	1	1	1	1	0	1	0	13
1	0	1	1	1	1	0	0	1	14
1	0	1	1	1	1	0	0	0	15
1	0	1	1	1	0	1	1	1	16
1	0	1	1	1	0	1	1	0	17
1	0	1	1	1	0	1	0	1	18
1	0	1	1	1	0	1	0	0	19
0	1	1	1	1	1	0	1	1	20
0	1	1	1	1	1	0	1	0	21
0	1	1	1	1	1	0	0	1	22
0	1	1	1	1	1	0	0	0	23
0	1	1	1	1	0	1	1	1	24
0	1	1	1	1	0	1	1	0	25
0	1	1	1	1	0	1	0	1	26
0	1	1	1	1	0	1	0	0	27
0	0	1	1	1	1	0	1	1	28
0	0	1	1	1	1	0	1	0	29

AGC8	AGC7	AGC6	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0	ATTENUATION FROM MAXIMUM GAIN (dB)
0	0	1	1	1	1	0	0	1	30
0	0	1	1	1	1	0	0	0	31
0	0	1	1	1	0	1	1	1	32
0	0	1	1	1	0	1	1	0	33
0	0	1	1	1	0	1	0	1	34
0	0	1	1	1	0	1	0	0	35
0	0	0	1	1	1	0	1	1	36
0	0	0	1	1	1	0	1	0	37
0	0	0	1	1	1	0	0	1	38
0	0	0	1	1	1	0	0	0	39
0	0	0	1	1	0	1	1	1	40
0	0	0	1	1	0	1	1	0	41
0	0	0	1	1	0	1	0	1	42
0	0	0	1	1	0	1	0	0	43
0	0	1	1	0	1	0	1	1	44
0	0	1	1	0	1	0	1	0	45
0	0	1	1	0	1	0	0	1	46
0	0	1	1	0	1	0	0	0	47
0	0	1	1	0	0	1	1	1	48
0	0	1	1	0	0	1	1	0	49
0	0	1	1	0	0	1	0	1	50
0	0	1	1	0	0	1	0	0	51
0	0	0	1	0	1	0	1	1	52
0	0	0	1	0	1	0	1	0	53
0	0	0	1	0	1	0	0	1	54
0	0	0	1	0	1	0	0	0	55
0	0	0	1	0	0	1	1	1	56
0	0	0	1	0	0	1	1	0	57
0	0	0	1	0	0	1	0	1	58
0	0	0	1	0	0	1	0	0	59
0	0	1	0	0	1	0	1	1	60
0	0	1	0	0	1	0	1	0	61
0	0	1	0	0	1	0	0	1	62
0	0	1	0	0	1	0	0	0	63
0	0	1	0	0	0	1	1	1	64
0	0	1	0	0	0	1	1	0	65
0	0	1	0	0	0	1	0	1	66
0	0	1	0	0	0	1	0	0	67
0	0	0	0	0	1	0	1	1	68
0	0	0	0	0	1	0	1	0	69
0	0	0	0	0	1	0	0	1	70

AGC8	AGC7	AGC6	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0	ATTENUATION FROM MAXIMUM GAIN (dB)
0	0	0	0	0	1	0	0	0	71
0	0	0	0	0	0	1	1	1	72
0	0	0	0	0	0	1	1	0	73
0	0	0	0	0	0	1	0	1	74
0	0	0	0	0	0	1	0	0	75
0	0	0	0	0	0	0	1	1	76
0	0	0	0	0	0	0	1	0	77
0	0	0	0	0	0	0	0	1	78
0	0	0	0	0	0	0	0	0	79

The AGC[8:0] code required to program the AGC attenuation (AGC_{att}) can be calculated from the following formulas:

$AGC[8:0] = (511 - AGC_{att})_B$ if $0 < AGC_{att} < 11$

$AGC[8:0] = (391 - AGC_{att})_B$ if $12 < AGC_{att} < 19$

$AGC[8:0] = (271 - AGC_{att})_B$ if $20 < AGC_{att} < 27$

$AGC[8:0] = (151 - AGC_{att})_B$ if $28 < AGC_{att} < 35$

$AGC[8:0] = (95 - AGC_{att})_B$ if $36 < AGC_{att} < 43$

$AGC[8:0] = (151 - AGC_{att})_B$ if $44 < AGC_{att} < 51$

$AGC[8:0] = (95 - AGC_{att})_B$ if $52 < AGC_{att} < 59$

$AGC[8:0] = (135 - AGC_{att})_B$ if $60 < AGC_{att} < 67$

$AGC[8:0] = (79 - AGC_{att})_B$ if $68 < AGC_{att} < 79$

Where $(X)_B$ is the binary code of the integer X.

9.3 RF PLL synthesizer

The RF fractional-N synthesizer is set via the 3-wire bus with the FRAC and CH chains. CH sets the integer divider ratio and FRAC the fractional divider ratio. They both provide the LO frequency in accordance with the following equation:

$$f_{RFLO} = f_{ref} \times \left(\frac{N_{RX}}{2} + K_{frac(RX)} \right)$$

Where $K_{frac(RX)} = \frac{1}{2^{22}} \times \left(K_{RX} + \frac{1}{2} \right)$

Where K_{RX} is the integer value of FRAC[21:0], N_{RX} is the integer value of CH[8:0] and f_{ref} is the external frequency reference applied to pin REFIN.

Example: to obtain a f_{RFLO} frequency of 2.14 GHz with an error less than Δf_{PLL} N_{RX} must be set to 164 and $K_{frac(RX)}$ to 1290555 if the reference frequency is 26 MHz. It should be noted that some particular frequencies can be obtained in two ways; N_{RX} = x and $K_{frac(RX)}$ = 0.25 provides the same frequency as N_{RX} = x – 1 and $K_{frac(RX)}$ = 0.75

9.4 Clock PLL synthesizer

9.4.1 AFC MODE

The clock PLL is based on the SD fractional-N synthesizer that allows to derive the UMTS system clock including AFC from a non-corrected external 26 MHz only GMS reference. The clock PLL frequency with the AFC correction word is given by the following equation:

$$f_{CLKPLL} = f_{ref} \times \left(\frac{9 + K_{AFC}}{2} \right)$$

Where $K_{AFC} = \frac{231}{512} + \frac{AFC}{2^{21}}$

AFC represents the integer value of AFC[11:0] and f_{ref} is the external reference frequency applied to pin REFIN.

9.4.2 CLOCK PLL MODES

The clock PLL synthesizer is controlled by bits CLKon and CLKoff. At power-up the clock PLL synthesizer is automatically on when pin RXCEN is set HIGH. The control, done with CLKon, will be reset at the rising edge of RXCEN. For application which do not require the UMTS clock system, the clock PLL can be powered-down with bit CLKoff set to logic 1.

Table 4 Clock mode

RXCEN	CLKon	CLKoff	DESCRIPTION
1	1	0	CLKPLL synthesizer enabled (default)
0	1	0	CLKPLL synthesizer disabled; note 1
1	0	0	CLKPLL synthesizer disabled; note 2
X[4]	X[4]	1	CLKPLL synthesizer disabled; note 3

Notes

1. Hard power-down of the clock PLL done with RXCEN.
2. Power-down achieved via the 3-wire bus, reset by RXCEN.
3. Power-down achieved via the 3-wire bus, no effect by RXCEN in this mode. This mode will be reset if V_{DDD} is not maintained.
4. X = don't care.

9.4.3 CLOCK PLL OUTPUT DIVIDER

The clock PLL output divider ratio is set in accordance with Table 5.

Table 5 Clock mode; note 1

CLKoff	CLK1	CLK0	DESCRIPTION
1	X	X	UMTSCLKO output disabled
0	0	0	clock divider ratio set to default
0	0	1	clock divider ratio set to 2
0	1	0	clock divider ratio set to 4
0	1	1	clock divider ratio set to 8

Note

1. X = don't care.

10 PROGRAMMING

10.1 Serial programming bus

A simple 3-wire unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and EN.

The data sent to the device is loaded in bursts framed by EN. Programming clock edges are ignored until EN goes active LOW. The programmed information is loaded into the addressed latch when EN goes HIGH (inactive). This is allowed when CLK is in either state without causing any consequences to the data register. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses.

The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during Power-down of the synthesizer.

10.2 Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The address bits are decoded on the rising edge of EN. This produces an internal load pulse to store the data in the address latch.

To ensure that data is correctly loaded on first power-up, EN should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is inhibited during the period when data is read by the frequency dividers. This condition is guaranteed by respecting a minimum EN pulse width after data transfer.

10.3 Register contents

Table 6 Register bit allocation

<table>
<tr><th colspan="21">CONTROL BITS</th><th colspan="4">ADDRESS</th></tr>
<tr><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="21">for test purposes only; all bits must be set to zero for normal operation; this is a forbidden address</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="21">for test purposes only; all bits must be set to zero for normal operation; this is a forbidden address</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td colspan="20">FRAC[15:0]</td><td>SYNON</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td colspan="15">CH[8:0]</td><td colspan="5">FR[21:16]</td><td>1</td><td>SYNON</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="14">AGC[8:0]</td><td>1</td><td>1</td><td>RXON</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td colspan="13">AFC[11:0]</td><td colspan="2">CKO[1:0]</td><td>CLKoff</td><td>CLKon</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
</table>

Table 7 Description of symbols used in Table 6

SYMBOL	BITS	DESCRIPTION
SYNON	1	3-wire bus
RXON	1	3-wire bus
AGC	9	automatic gain control
CH	6	integer division ratio for the RF PLL
FRAC	22	fractional division ratio for the RF PLL
AFC	12	automatic frequency control for the clock PLL
CLKoff	1	clock PLL disabled
CKO	2	integer division ratio for the clock PLL

Table 8 Register preset condition

CONTROL																ADDRESS			
20	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	0
0	1	0	0	1	0	1	0	0	1	1	1	0	0	0	0	0	0	1	1	1

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		–0.3	–	+2.8	V
V_{CCA}	analog supply voltage		–0.3	–	+3.3	V
P_{tot}	total power dissipation		–	–	300	mW
T_{amb}	ambient temperature		–30	–	+80	°C
T_{stg}	storage temperature		–40	–	+150	°C

12 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; on a 4 layer PCB and with soldered exposed die pad	36	K/W

13 DC CHARACTERISTICS

V_{CCA} = 2.6 V; $V_{CCA(CP)}$ = 2.6 V;T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage	on pins $V_{CCA(RF)}$, $V_{CCA(IF)}$, $V_{CCA(CP)}$ and $V_{CCA(SYN)}$	2.6	2.8	3.3	V
V_{DDD}	digital supply voltage		1.6	1.8	2.8	V
$I_{CCA(tot)}$	total analog supply current	receive mode; note 1	–	52	63	mA
		receive mode; note 2	–	45	54	mA
		synthesizer mode; note 3	–	25	30	mA
		standby mode; note 4	–	12	15	mA
		sleep mode; note 5	–	10	50	µA
$I_{CCA(RF)}$	analog supply current for the RF VCO section		–	19	–	mA
$I_{CCA(IF)}$	analog supply current for the RX section		–	16	–	mA
$I_{CCA(SYN)}$	analog supply current for the synthesizer		–	15	–	mA
$I_{CCA(CP)}$	analog supply current for the charge pump		–	0.9	–	mA
I_{DDD}	digital supply current		–	1.1	–	mA
Baseband IQ section; pins IN, IP, QP and QN						
$V_{O(IQ)(CM)}$	IQ common mode output voltage	$0.5(V_{IN} + V_{IP})$ or $0.5(V_{QP} + V_{QN})$; note 6	1.15	1.25	1.35	V
RF VCO section; pin CAPVCOREG						
$V_{O(CAPVCOREG)}$	output voltage		–	2	–	V
CLKPLL section; pin UMTSCLKO						
$V_{O(UMTSCLKO)}$	output voltage		–	0.8	–	V
Reference voltage; pin REXT						
V_{REXT}	reference voltage for the charge pump	R_{ext} = 1.8 kΩ	–	360	–	mV
Control section; pins DATA, CLK, EN and RXON						
V_{IH}	HIGH-level input voltage		0.9	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.3	V

Notes

1. Receive mode: All circuits are active.
2. Receive mode: All circuits are active with the clock PLL off (CLKoff = 1).
3. Synthesizer mode: RF PLL and clock PLL are active.
4. Standby mode: Clock PLL is active.
5. Sleep mode: RXCEN set LOW, DATA, CLK and EN are in high-impedance.
6. Receive mode: DC voltage supplied from the IC.

14 AC CHARACTERISTICS

V_{CCA} = 2.6 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF receiver inputs; pins RFIN and RFIP						
$f_{i(RF)}$	RF input frequency		2.11	–	2.17	GHz
R_i	input resistance		–	170	–	Ω
C_i	input capacitance		–	1	–	pF
s_{11}	input power matching	with external balun	–	–10	–	dB
F	noise figure	in receive mode with maximum gain	–	3.2	4	dB
CP_1	1 dB compression point	in receive mode with maximum gain	–23	–20	–	dBm
IP_3	input referred 3rd-order intercept point	in receive mode with maximum gain; interference 20 MHz away from channel bandwidth	–18	–15	–	dBm
IP_2	input referred 2nd-order intercept point	in receive mode with maximum gain; interferers 190 MHz away from channel bandwidth	37	42	–	dBm
φ_n	phase noise	at 15 MHz offset	–	–	–135	dBc/Hz
Baseband IQ section; pins IP, IN, QP and QN						
$G_{v(max)}$	maximum voltage gain		92	96	100	dB
$G_{v(min)}$	minimum voltage gain		12	17	22	dB
AGC_{tot}	total AGC range		–	79	–	dB
$G_{step(AGC)}$	AGC gain step		–	1	–	dB
$AGC_{tot(lin)}$	total AGC linearity		–0.5	–	+0.5	dB
$\Delta G_{v(IQ)}$	voltage gain mismatch between the I and Q paths		–	–	0.5	dB
$\Delta\Phi$	quadrature phase error between the I and Q paths	peak error	–	–	5	deg
$V_{o(max)}$	maximum output voltage per pin	$R_{L(diff)}$ = 10 kΩ; THD < 3%	0.75	–	–	V
$I_{o(max)}$	maximum output current per pin	$V_{o(p-p)}$ = 1.75 V at 1 MHz; $R_{L(diff)}$ = 10 kΩ; $C_{L(diff)}$ = 20 pF	650	–	–	μA
$V_{offset(diff)}$	differential output offset voltage		–20	–	+20	mV
HP_{-3dB}	–3 dB high-pass corner frequency	2nd-order high-pass frequency	10	15	20	kHz
LP_{-3dB}	–3 dB low-pass corner frequency	5th-order low-pass frequency	2.25	2.4	2.55	MHz
$\Delta d_{(g)}$	group delay variation	100 kHz < f_o < 2 MHz	–	260	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{LPF}	LPF attenuation	f_i = 5 MHz	39	42	–	dB
		f_i = 10 MHz	72	75	–	dB
		f_i = 15 to 60 MHz	91	94	–	dB
RF synthesizer; pin RFCPO						
f_{RFLO}	synthesizer frequency		2.11	–	2.17	GHz
$f_{comp(RF)}$	RF comparison frequency		–	26	–	MHz
Δf_{PLL}	frequency resolution	f_{comp} = 13 to 26 MHz	0.05	–	–	ppm
		f_{comp} = 26 MHz	–	–	6.2	Hz
Φ_n	close-in-phase noise	at 2 kHz offset	–	–85	–80	dBc/Hz
I_{sink}	sink current	R_{ext} = 1.8 kΩ; THD = 1%	170	200	230	µA
I_{source}	source current	R_{ext} = 1.8 kΩ; THD = 1%	170	200	230	µA
$V_{o(CP)}$	charge pump output voltage	charge pump current within specified range	0.4	–	V_{CCA} – 0.4	V
KΦ	PFD gain	R_{ext} = 1.8 kΩ; THD = 1%	27	32	37	µA/rad
$I_{leak(CP)}$	charge pump leakage current in off state	over full charge pump voltage range	–1	–	+1	µA
Fractional-N synthesizer; $f_{RFLO} = f_{ref} \times \left(\frac{N_{RX}}{2} + K_{frac(RX)}\right)$ **where** $K_{frac(RX)} = \frac{1}{2^{22}} \times \left(K_{RX} + \frac{1}{2}\right)$						
N	integer divider ratio		130	–	507	
K_{frac}	fractional divider ratio		0.25	–	0.75	
Integrated RF VCO; pin RFCPO						
f_{RF}	RF frequency	V_{RFCPO} = 0 to 3.3 V	4.22	–	4.34	GHz
G_{VCO}	VCO gain	V_{RFCPO} = 1.3 V	50	70	90	MHz/V
V_{tune}	tuning voltage		0.4	–	V_{CCA} – 0.4	V
Δf_{VCC}	pushing		–	–	tbf	MHz/V
$t_{cal(VCO)}$	VCO calibration time	after RXON = LO ≥ HI	–	–	35	µs
CLKPLL synthesizer; pin CPCLKO						
f_{CLKPLL}	synthesizer frequency	V_{CPCLKO} = 0 to 3.3 V	-	122.88	-	MHz
f_{comp}	comparison frequency		–	13	–	MHz
Δf_{PLL}	frequency resolution	f_{ref} = 26 MHz	0.477	–	–	ppm
AFC_{cor}	AFC correction range		–	±30	–	ppm
I_{sink}	sink current	R_{ext} = 1.8 kΩ; THD = 1%	170	200	230	µA
I_{source}	source current	R_{ext} = 1.8 kΩ; THD = 1%	170	200	230	µA
$V_{o(CP)}$	charge pump output voltage	charge pump current within specified range	0.4	–	V_{CCA} – 0.4	V
KΦ	PFD gain	R_{ext} = 1.8 kΩ; THD = 1%	27	32	37	µA/rad
$I_{leak(CP)}$	charge pump leakage current in off state	over full charge pump voltage range	–1	–	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fractional-N synthesizer; $f_{CLKPLL} = f_{ref} \times \left(\frac{N + K_{AFC}}{2}\right)$ **where** $K_{AFC} = \frac{231}{512} + \frac{AFC}{2^{21}}$						
N	integer divider ratio		–	9	–	
K_{AFC}	fractional divider ratio		0.4512	–	0.4532	
Integrated CLKPLL VCO; pin CPCLKO						
f_{VCO}	CLKPLL frequency	V_{CPCLKO} = 0 to 3.3 V	100	–	140	MHz
G_{VCO}	VCO gain	V_{CPCLKO} = 1.3 V	12	15	23	MHz/V
V_{tune}	tuning voltage		0.4	–	V_{CCA} – 0.4	V
Output CLKPLL buffer; pin UMTSCLKO						
$f_{UMTSCLKO}$	frequency range		15.36	30.72	61.44	MHz
N	divider ratio		2	4	8	
Φ_n	close-in-phase noise	at 2 kHz offset for 30.72 MHz	–	–	–90	dBc/Hz
	phase noise	at 3.84 MHz offset for 30.72 MHz	–	–	–110	dBc/Hz
$V_{o(p-p)}$	output voltage (peak-to-peak value)	R_L = 10 kΩ	1	–	–	V
Low noise crystal amplifier; pin REFIN						
f_{REF}	reference frequency		13	–	26	MHz
$V_{i(REF)(rms)}$	input voltage (RMS value)		50	–	400	mV
$R_{i(REF)}$	input resistance	f_{REF} = 26 MHz	–	tbf	–	kΩ
$C_{i(REF)}$	input capacitance	f_{REF} = 26 MHz	–	tbf	–	pF

15 SERIAL BUS TIMING CHARACTERISTICS

V_{CCA} = 2.6 V; $V_{CCA(CP)}$ = 2.6 V; V_{DDD} = 1.6 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial clock; pin CLK					
$t_{i(r)}$	input rise time	–	–	20	ns
$t_{i(f)}$	input fall time	–	–	20	ns
T_{cyc}	clock period	67	–	–	ns
Enable; pin EN					
$t_{d(START)}$	delay to rising clock edge	200	–	–	ns
$t_{d(END)}$	delay from last falling clock edge	100	–	–	ns
t_W	minimum inactive pulse width	400	–	–	ns
$t_{su;EN}$	enable set-up time to next clock	200	–	–	ns
Register serial input data; pin DATA					
$t_{su;DATA}$	input data to clock set-up time	25	–	–	ns
$t_{h;DATA}$	input data to clock hold time	25	–	–	ns

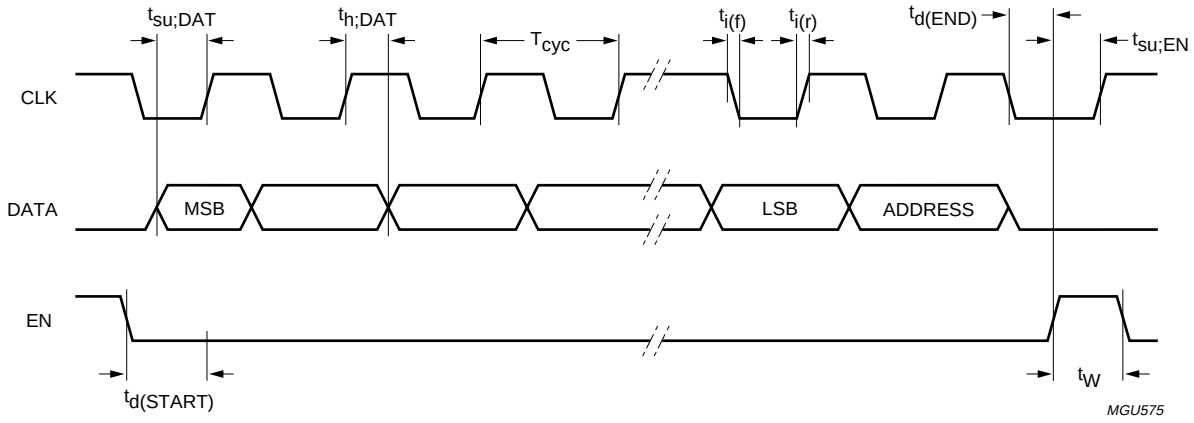


Fig.3 Serial bus timing diagram.

16 APPLICATION INFORMATION

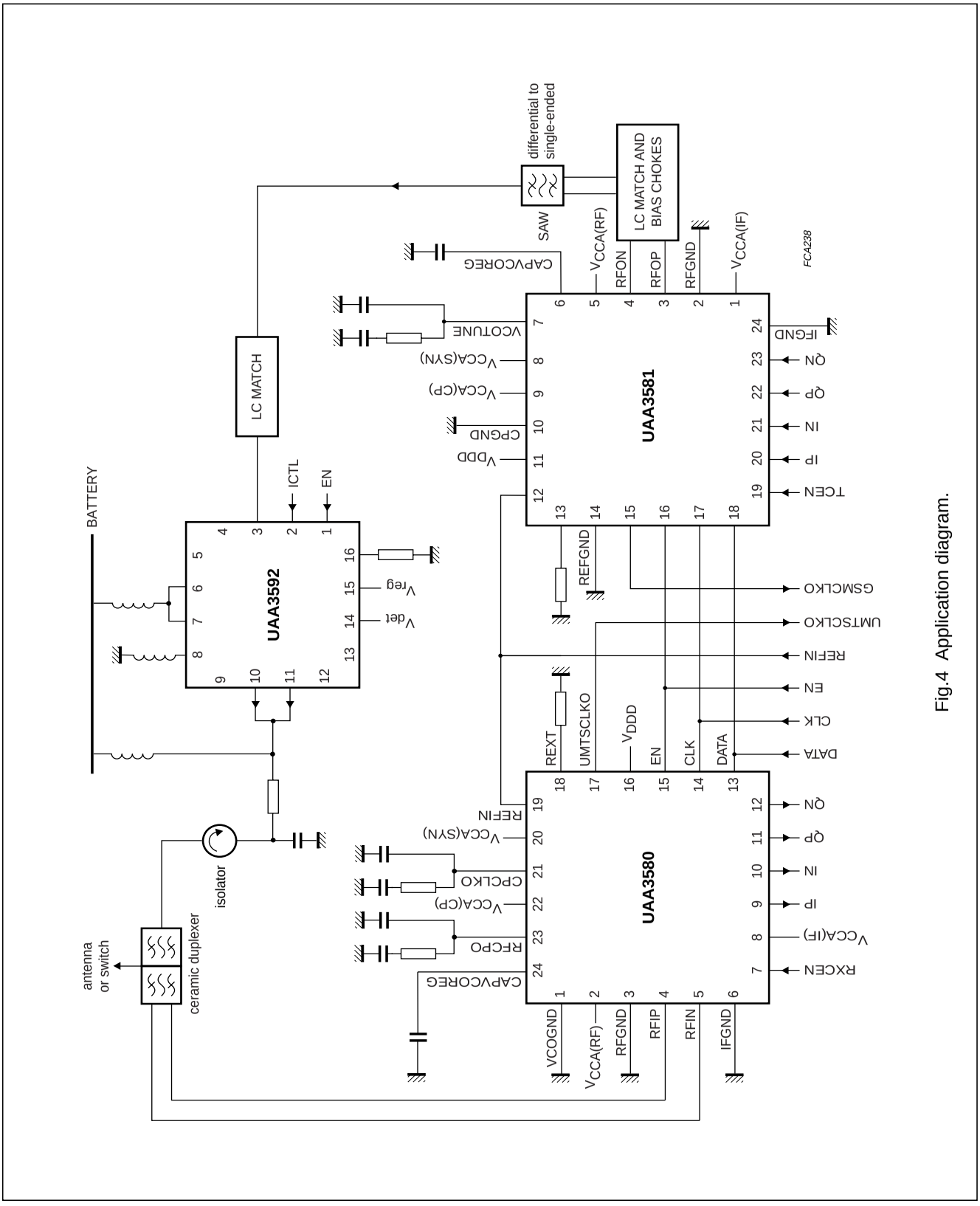
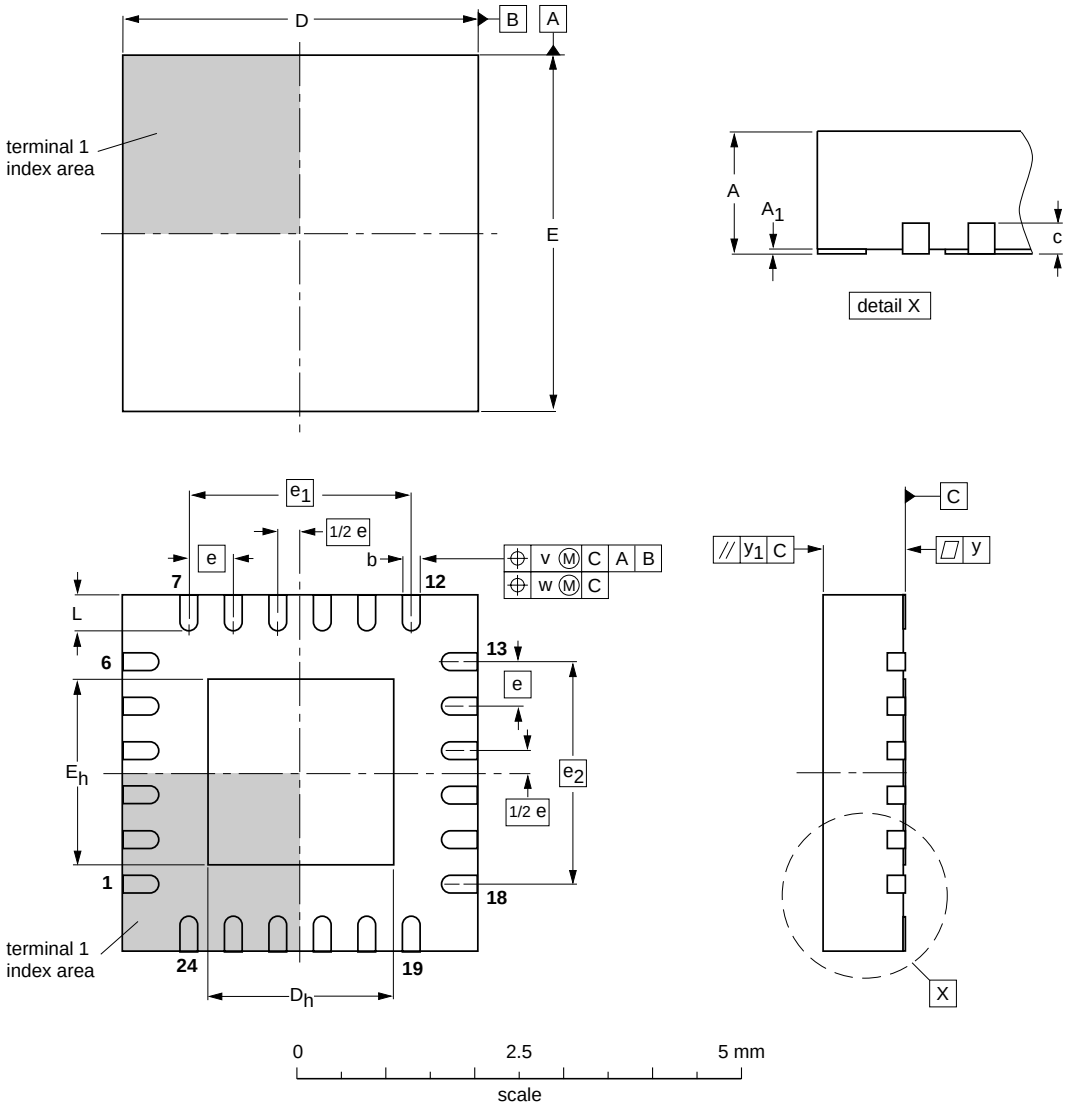


Fig.4 Application diagram.

17 PACKAGE OUTLINE

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

18 SOLDERING

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

18.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

19 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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