DATA SHEET

SAA5252
Line twenty-one acquisition and display (LITOD)

Product specification
Supersedes data of March 1995
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

Line twenty-one acquisition and display (LITOD) SAA5252

FEATURES

- Complete ‘stand-alone’ Line 21 decoder in one package
- On-chip display RAM allowing full page Text mode
- Enhanced character display modes
- Full colour captions
- RGB interface for standard colour decoder ICs
- Automatic handling of Field 2 data
- Automatic selection of (1H, 1V), (2H, 1V) or (2H, 2V) scan modes
- Onboard OSD facility using Character generator
- RGB inputs to support existing OSD ICs
- I^2C-bus or ‘stand-alone’ pin control
- Automatic data-ready signal generation on data acquisition
- Can decode signals recorded on standard VHS and S-VHS tape.

GENERAL DESCRIPTION

The SAA5252 (LITOD) is a single-chip CMOS device, which will acquire, decode and display Line 21 Closed Captioning data from a 525-line composite video signal. Operation as an On-Screen Display (OSD) device is also possible. Normal and line progressive scan modes are supported.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	30	–	mA
V_{syn}	CVBS sync amplitude	0.1	0.3	0.6	V
V_{vid}	CVBS video amplitude	0.7	1.0	1.4	V
T_{amb}	operating ambient temperature	–20	–	+70	°C
T_{stg}	storage temperature	–55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5252P	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
SAA5252T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

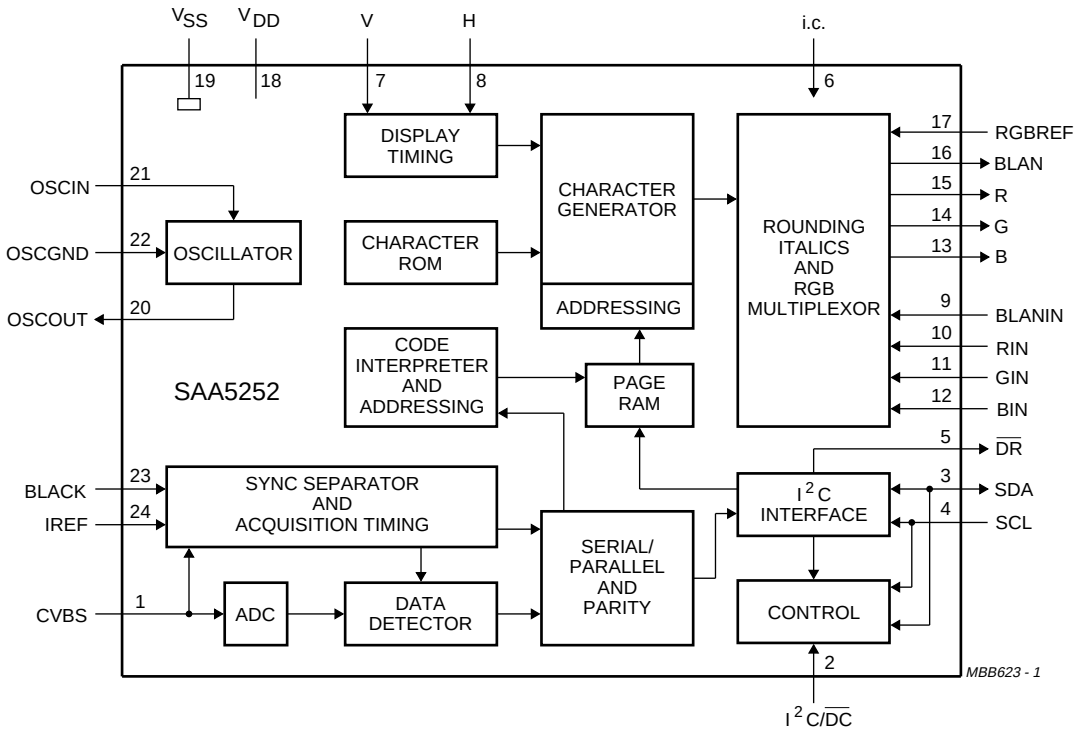


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	composite video input; signal should be connected via a 100 nF capacitor
$I^2C/\overline{DC}$	2	input selects I^2C or Direct Control
SDA	3	serial data port for I^2C-bus or mode select input for direct control
SCL	4	serial clock input for I^2C-bus or mode select input for direct control
$\overline{DR}$	5	data-ready signal to microcontroller (active-LOW) or mode select input for direct control
i.c.	6	internally connected; connect to V_{SS} for normal operation
V	7	vertical reference input for display timing
H	8	horizontal reference input for display timing
BLANIN	9	video blanking input from external OSD device
RIN	10	RED video input from external OSD device
GIN	11	GREEN video input from external OSD device
BIN	12	BLUE video input from external OSD device
B	13	BLUE video output
G	14	GREEN video output
R	15	RED video output
BLAN	16	video blanking output
RGBREF	17	input voltage defining output HIGH level for RGB pins for closed captioning output
V_{DD}	18	+5 V supply
V_{SS}	19	0 V ground
OSCOUT	20	oscillator output
OSCIN	21	oscillator input
OSCGND	22	oscillator ground
BLACK	23	video black level storage input; connected to V_{SS} via 100 nF capacitor
IREF	24	reference current input; connected to V_{SS} via 27 kΩ resistor

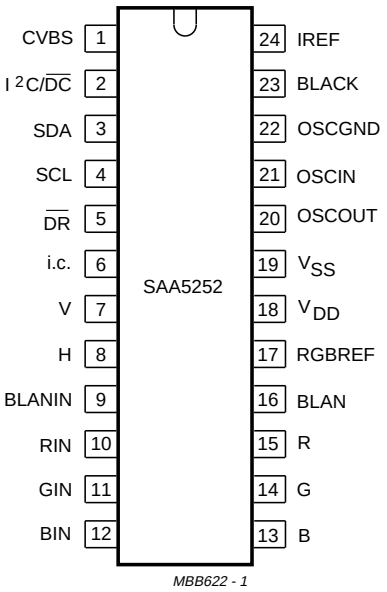


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)		–0.3	+6.5	V
V_{Imax}	maximum input voltage (any input)	note 1	–0.3	V_{DD} + 0.5	V
V_{Omax}	maximum output voltage (any output)	note 1	–	V_{DD} + 0.5	V
V_{dif}	difference between V_{SS} and OSCGND		–	±0.25	V
I_{IOK}	DC input or output diode current		–	±20	mA
I_{Omax}	maximum output current (each output)		–	±10	mA
T_{amb}	operating ambient temperature		–20	+70	°C
T_{stg}	storage temperature		–55	+125	°C
V_{es}	electrostatic handling				
	human body model	note 2	–2000	+2000	V
	machine model	note 3	–200	+200	V

Notes

1. This maximum value has an absolute maximum of 6.5 V independent of V_{DD}.
2. The human body model ESD simulation is equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor, which produces a single discharge transient. Reference *“Philips Semiconductors Test Method UZW-BO/FQ-A302 (similar to MIL-STD 883C method 3015.7)”*.
3. The machine model ESD simulation is equivalent to discharging a 200 pF capacitor via a resistor and series inductor with effective dynamic values of 25 Ω and 2.5 μH, which produces a damped oscillating discharge. Reference *“Philips Semiconductors Test Method UZW-BO/FQ-B302 (similar to EIAJ IC-121 Test Method 20 condition C)”*.

Quality

This device will meet the requirements of the *“Philips Semiconductors General Quality Specification UZW-BO/FQ-0601”* in accordance with *“Quality Reference Handbook (order number 9397 750 00192)”*. This details the acceptance criteria for all Q & R tests applied to the product.

CHARACTERISTICS

V_{DD} = 5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DDtot}	total supply current		–	30	–	mA
Inputs						
CVBS (PIN 1)						
V_{syn}	sync voltage amplitude		0.1	0.3	0.6	V
$V_{vid(p-p)}$	video voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
V_{dat}	caption data voltage amplitude		0.25	0.35	0.49	V
Z_{source}	source impedance		–	–	250	Ω
V_I	input switching voltage level of sync separator		1.7	2.0	2.3	V
Z_I	input impedance		2.5	5	–	kΩ
C_I	input capacitance		–	–	10	pF
IREF (PIN 24)						
R_{24}	resistor to ground		–	27	–	kΩ
V_{24}	voltage on pin 24		–	$\frac{1}{2}V_{DD}$	–	V
H (PIN 8)						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_{Imax}	maximum input current		–1	–	+1	mA
C_I	input capacitance		–	–	10	pF
t_r	pulse rise time		–	–	5	µs
t_f	pulse fall time		–	–	5	µs
t_W	pulse width					
	scan mode 1H		1	12	63	µs
	scan mode 2H		1	6	31	µs
V (PIN 7)						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_{Imax}	maximum input current		–1	–	+1	mA
C_I	input capacitance		–	–	10	pF
t_r	pulse rise time		–	–	5	ns
t_f	pulse fall time		–	–	5	ns
t_W	pulse width		1	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGBREF (PIN, 17)						
V_I	input voltage		–0.3	–	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
R, G AND B (PINS 15, 14 AND 13); note 1						
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
Z_I	input impedance		2.5	5.0	–	kΩ
BLANIN (PIN 9)						
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
t_r	input rise time	between 10% and 90%	–	–	80	ns
t_f	input fall time	between 90% and 10%	–	–	80	ns
$I^2C/\overline{DC}$ (PIN 2)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
SCL (PIN 4)						
V_{IL}	LOW level input voltage		–0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
f_{clk}	clock frequency		0	–	100	kHz
t_r	input rise time	between 10% and 90%	–	–	2	µs
t_f	input fall time	between 90% and 10%	–	–	2	µs
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CERAMIC RESONATOR (PINS 20, 21 AND 22); see Fig.5						
f_{osc}	oscillator frequency		11.82	12	12.18	MHz
C0	parallel capacitance		–	5.35	–	pF
C1	series capacitance		–	37.4	–	pF
L1	series inductance		–	35.5	–	µH
R1	series resistance		–	6	25	Ω
BLACK (PIN 23)						
C_{black}	storage capacitor to ground		–	100	–	nF
V_{black}	black level voltage for nominal sync amplitude		1.8	2.15	2.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDA (PIN 3; OPEN DRAIN)						
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	between 10% and 90%	–	–	2	µs
t_f	input fall time	between 90% and 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	between 3 V and 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF
$\overline{DR}$ (PIN 5; OPEN DRAIN)						
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
t_f	output fall time	between 4 V and 1 V with 3.3 kΩ to 5 V	–	–	50	ns
C_L	load capacitance		–	–	100	pF
Outputs						
R, G AND B (PINS 15, 14 AND 13; CAPTION MODE)						
V_{OL}	LOW level output voltage	I_{OL} = +2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA	V_{17} – 0.3	V_{17}	V_{17} + 0.4	V
Z_O	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%	–	–	10	ns
t_f	output fall time	between 90% and 10%	–	–	10	ns
BLAN (PIN 16)						
V_{OL}	LOW level output voltage	I_{OL} = +2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA	1.1	–	2.8	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%	–	–	10	ns
t_f	output fall time	between 90% and 10%	–	–	10	ns
t_{skew}	skew delay time between display and R, G, B, BLAN		–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C timing (see Fig.3)						
t_{LOW}	clock LOW time		4	–	–	µs
t_{HIGH}	clock HIGH time		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH-to-STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs
t_r	output rise time	between 10% and 90%	–	–	10	ns
t_f	output fall time	between 90% and 10%	–	–	10	ns

Note

1. These inputs are analog, V_{IL} and V_{IH} values are quoted as a guide for digital RGB users.

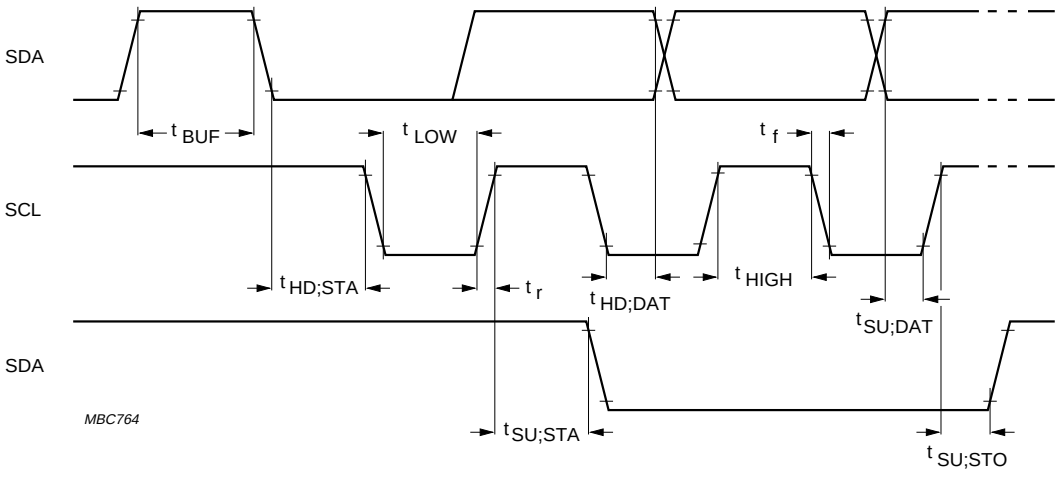
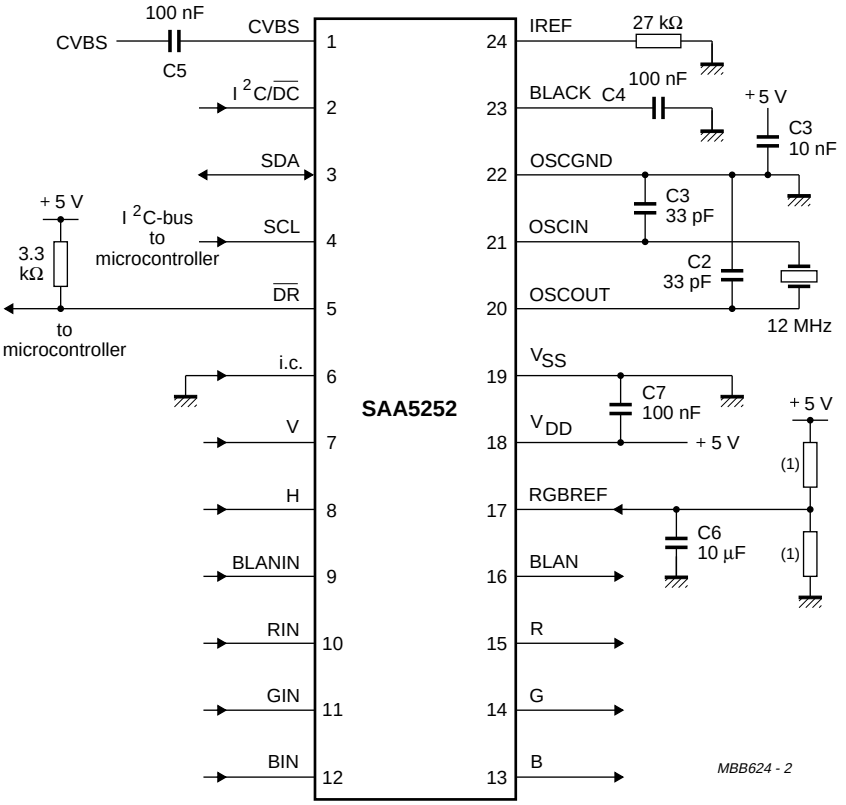


Fig.3 I^2C-bus timing diagram.

APPLICATION INFORMATION



(1) Value dependent on application.

Fig.4 Application diagram.

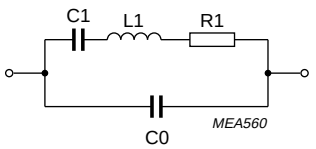


Fig.5 Ceramic resonator equivalent circuit.

DISPLAY GENERATOR

General description

The displayed characters are defined on a 5-by-12 matrix within a 7-by-13 window, allowing one blank pixel either side of the character and a blank pixel row above. There are a number of display options available controlled by Register 1, or external pins in ‘stand-alone’ mode.

The three display modes are video, text and caption, the device is powered up in the video mode.

The display generator reads the Pre-amble Address Code (PAC) then the data associated with that row. Each character is then rounded after which it can be italicized and/or underlined, depending on the PAC or mid-row codes, before being passed on to the output circuitry. Figure 6 shows the character set.

Display of external On-Screen Display (OSD) facilities

The R, G, B and BLAN outputs of the display have the capability to be put in a 3-state mode allowing other OSD devices to take control of the television R, G, B and BLAN signals.

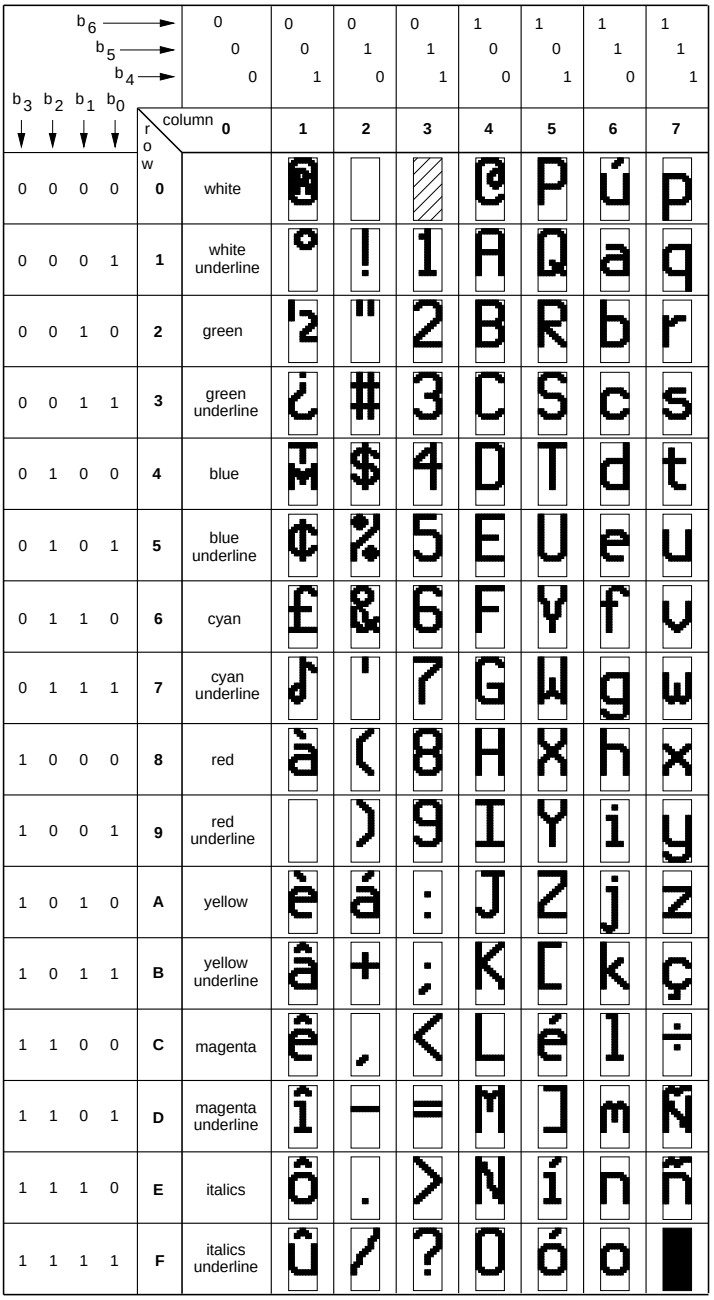
When the BLANIN is held HIGH then the R, G, B and BLAN outputs from display are disabled and the R, G, B and BLAN signals come directly from the RGBIN and BLANIN inputs. This will allow On-Screen Display to be placed on top of the captioning without any corruption, leaving the captions intact when the On-Screen Display is switched off (BLANIN goes LOW). In this form of operation the RGBIN and RGBOUT pins can be considered transparent; BLANIN goes through the normal output buffer to BLAN.

Table 1 Register map (WRITE)

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00	DF$\overline{1}$/2	RGB, BLAN +$\overline{\text{ve}}$/–ve	H +ve/–$\overline{\text{ve}}$	V +ve/–$\overline{\text{ve}}$	H3	H2	H1	H0
01	CLEAR	CH 2/$\overline{1}$	$\overline{\text{NARROW}}$/ WIDE	ACQ OFF	EN1	EN0	M1	M0
02	–	–	–	–	ROW3	ROW2	ROW1	ROW0
03	–	–	–	COL4	COL3	COL2	COL1	COL0
04	–	OSD6	OSD5	OSD4	OSD3	OSD2	OSD1	OSD0

Table 2 Register map (READ)

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
80	POR	0	0	0	$\overline{\text{F1}}$/F2	EDS	PARITY SHUTDOWN	DATA READY
81	PARITY ERROR	DATA BIT 7	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1
82	PARITY ERROR	DATA BIT 7	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1



b_3 b_2 b_1 b_0	row	b_6 / b_5 / b_4	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
		column	0	1	2	3	4	5	6	7
0 0 0 0	0	white	®				@	P	ú	p
0 0 0 1	1	white underline	°	!	1	A	Q	a	q
0 0 1 0	2	green	½	"	2	B	R	b	r
0 0 1 1	3	green underline	¿	#	3	C	S	c	s
0 1 0 0	4	blue	™	$	4	D	T	d	t
0 1 0 1	5	blue underline	¢	%	5	E	U	e	u
0 1 1 0	6	cyan	£	&	6	F	V	f	v
0 1 1 1	7	cyan underline	♪	'	7	G	W	g	w
1 0 0 0	8	red	à	(	8	H	X	h	x
1 0 0 1	9	red underline		)	9	I	Y	i	y
1 0 1 0	A	yellow	è	á	:	J	Z	j	z
1 0 1 1	B	yellow underline	â	+	;	K	[	k	ç
1 1 0 0	C	magenta	ê	,	<	L	é	l	÷
1 1 0 1	D	magenta underline	î	–	=	M	]	m	Ñ
1 1 1 0	E	italics	ô	.	>	N	í	n	ñ
1 1 1 1	F	italics underline	û	/	?	O	ó	o	■

signifies "flash on" command

signifies a transparent space

MBB625 - 2

The ‘0’ and ‘zero’ use the same character, 4FH.

Fig.6 Character set.

I²C INTERFACE

Description of WRITE registers

The write subaddresses auto increment from 0 through to 4 at which point they stay until a new write subaddress is sent. Registers are set to all logic 0 at power-up.

Table 3 Register 0 WRITE (Control Byte 1)

BIT	DESCRIPTION
D0 to D3	H0 to H3 set the offset position from the start of the horizontal sync pulse, set to a nominal value on reset.
D4	Vertical sync pulse expected to be negative going logic 0 or positive-going logic 1.
D5	Horizontal sync pulse expected to be negative going logic 0 or positive-going logic 1.
D6	Video outputs will be positive going logic 0 or negative-going logic 1.
D7	Data field select. When set to logic 0 Field 1 is decoded, when set to logic 1 Field 2 is decoded.

Table 4 Register 1 WRITE (Control Byte 2)

BIT	DESCRIPTION
D0, D1	Display mode selection bits. Table 8 shows the possible display modes.
D2, D3	Enhanced caption mode selection bits. Table 9 shows the possible enhanced caption modes.
D4	When set to logic 1 acquisition of caption data is inhibited to allow the display to be used for On-Screen Display purposes.
D5	Acquisition window selection. When set to logic 0 only Line 21 is checked for caption data. When set to logic 1, lines 19 to 23 of both fields are checked, allowing encrypted video signals to be handled.
D6	User channel selection.
D7	Clears the page memory when set HIGH. The page memory will be within two fields (30 ms).

Table 5 Register 2 WRITE (On-Screen Display data row address)

BIT	DESCRIPTION
D0 to D3	Row 0 to 3 sets the row address for On-Screen Display. This stored value will be incremented by overflow increments of Register 3.

Table 6 Register 3 WRITE (On-Screen Display data column address)

BIT	DESCRIPTION
D0 to D4	Columns 0 to 4 sets the column address for On-Screen Display. This stored value will be incremented by writes to Register 4.

Table 7 Register 4 WRITE (On-Screen Display data)

BIT	DESCRIPTION
D0 to D6	OSD0 to OSD6, On-Screen Display data bits writing to this register causes Register 3 to increment its stored value.

Table 8 Display modes

DISPLAY MODE OPTIONS	M1	M0
Video only	0	0
Text mode	0	1
Normal caption mode	1	0
Enhanced caption mode	1	1

Table 9 Enhanced caption modes

ENHANCED CAPTION MODES	EN1	EN0
Enhanced caption modes	EN1	EN0
Shadowed character/Video background	0	0
Shadowed character/Mesh background	0	1
Normal character/Video background	1	0
Normal character/Mesh background	1	1

Description of READ registers

The read subaddresses auto increment from 80H through to 82H at which point they stay until a new read subaddress is sent.

All the bits in Table 10 are reset to logic 0 after the register is read.

Table 10 Register 80H READ (status)

BIT	DESCRIPTION
D0	Data ready (new data has been acquired).
D1	Parity error shut-down, goes HIGH when SAA5252 has a parity shut-down condition.
D2	Indicates the following bytes are extended data service bytes.
D3	Indicates Field 1 or Field 2 data bytes.
D7	Indicates Power-On Reset (POR) has occurred, all I^2C-bus write registers have been reset to logic 0.

Table 11 Register 81H READ (first data byte)

BIT	DESCRIPTION
D0 to D6	Data Bit 1 to Data Bit 7 (see note 1).
D7	Parity error flag bit. Bit goes HIGH when a parity error has occurred.

Note

1. In the Line 21, specification data bits are numbered D1 to D8.

Table 12 Register 82H READ (second data byte)

BIT	DESCRIPTION
D0 to D6	Data Bit 1 to Data Bit 7 (see note 1).
D7	Parity error flag bit. Bit goes HIGH when a parity error has occurred.

Note

1. In the Line 21, specification data bits are numbered D1 to D8.

Interface to microcontroller using I²C-bus

The interface to the microcontroller is via the two-wire serial I²C-bus, and optionally by a Data-Ready signal ($\overline{DR}$). On power up the microcontroller initializes the device by an I²C-bus WRITE to Registers 0 (Control Byte 1). The I²C-bus subaddress is then auto incremented to point to Register 1 (Control Byte 2). These two registers configure the device to the users requirements.

If the device is to be used for data acquisition only, then there are three methods by which the microcontroller can be informed of the arrival of valid Line 21 data:

- It can poll the $\overline{DR}$ pin, if the function has been enabled, and wait for it to go LOW.
- It can use the negative edge of the $\overline{DR}$ signal to cause an interrupt.
- It can poll the Data Ready bit (bit D0 of the status byte, I²C-bus READ Register 0).

When valid data is detected, the microcontroller must initiate an I²C-bus READ of Registers 80H, 81H and 82H. The first and second data bytes from the most recently received Line 21 are in Register 81H and Register 82H respectively.

The $\overline{DR}$ pin, and the Data Ready bit (Status bit D0) will be cleared after any register has been read. POR is reset after Register 80H has been read.

‘STAND-ALONE’ (NON I²C-BUS) OPERATION

To set the SAA5252 for ‘stand-alone’ operation pin 2 (I²C/$\overline{DC}$) is tied LOW. This will change the operation of the SCL, SDA and $\overline{DR}$ pins to mode select inputs which will select as shown in Table 13.

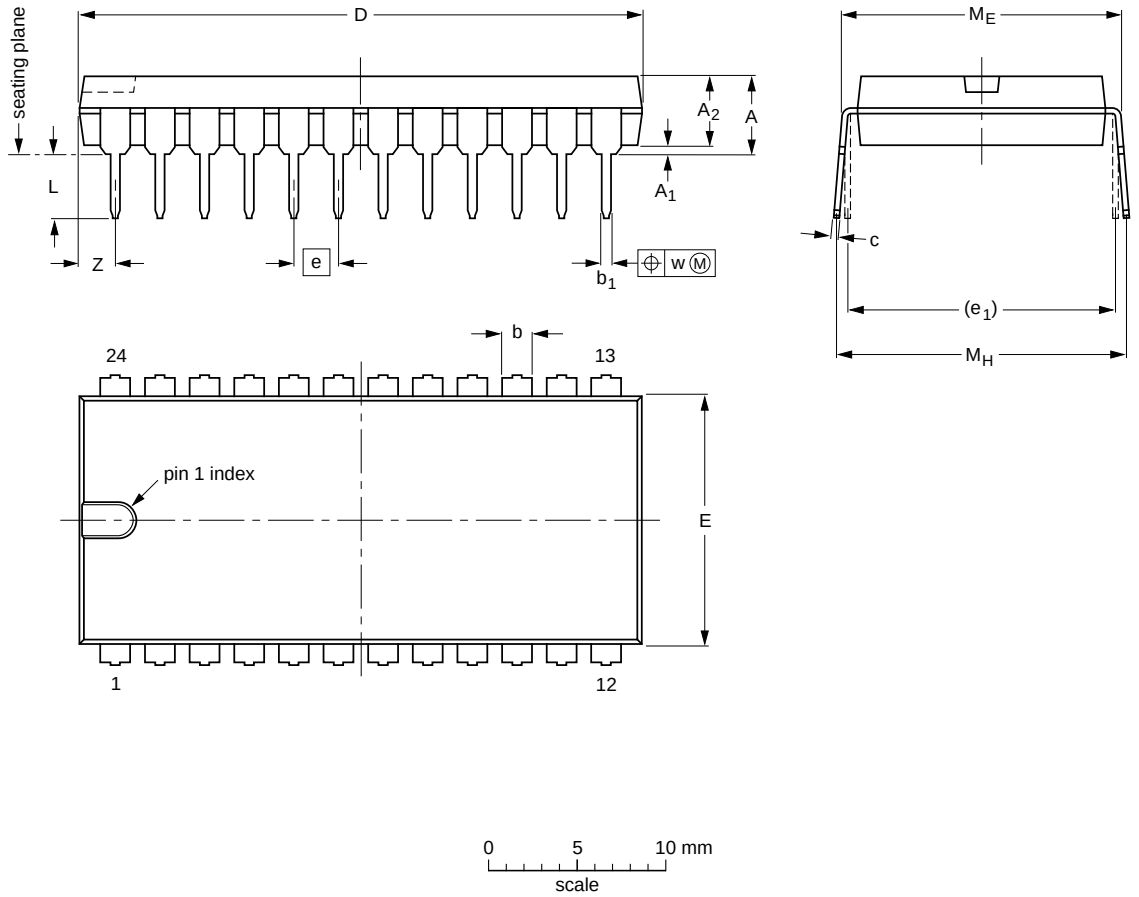
In the caption mode the SAA5252 operates in the basic Normal character/Black background mode. This complies with the FCC ruling. In the Enhanced caption mode the set-up will be Shadowed character/Video background. SDA and SCL in the ‘stand-alone’ operation act as bits M0 and M1 in Table 8.

Table 13 Stand-alone modes

$\overline{DR}$	SCL	SDA	MODE OF OPERATION	CHANNEL RECEPTION
0	0	0	video mode	Channel 1
0	0	1	text mode	Channel 1
0	1	0	normal captions	Channel 1
0	1	1	enhanced captions	Channel 1
1	0	0	video mode	Channel 2
1	0	1	text mode	Channel 2
1	1	0	normal captions	Channel 2
1	1	1	enhanced captions	Channel 2

PACKAGE OUTLINES

DIP24: plastic dual in-line package; 24 leads (600 mil) SOT101-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

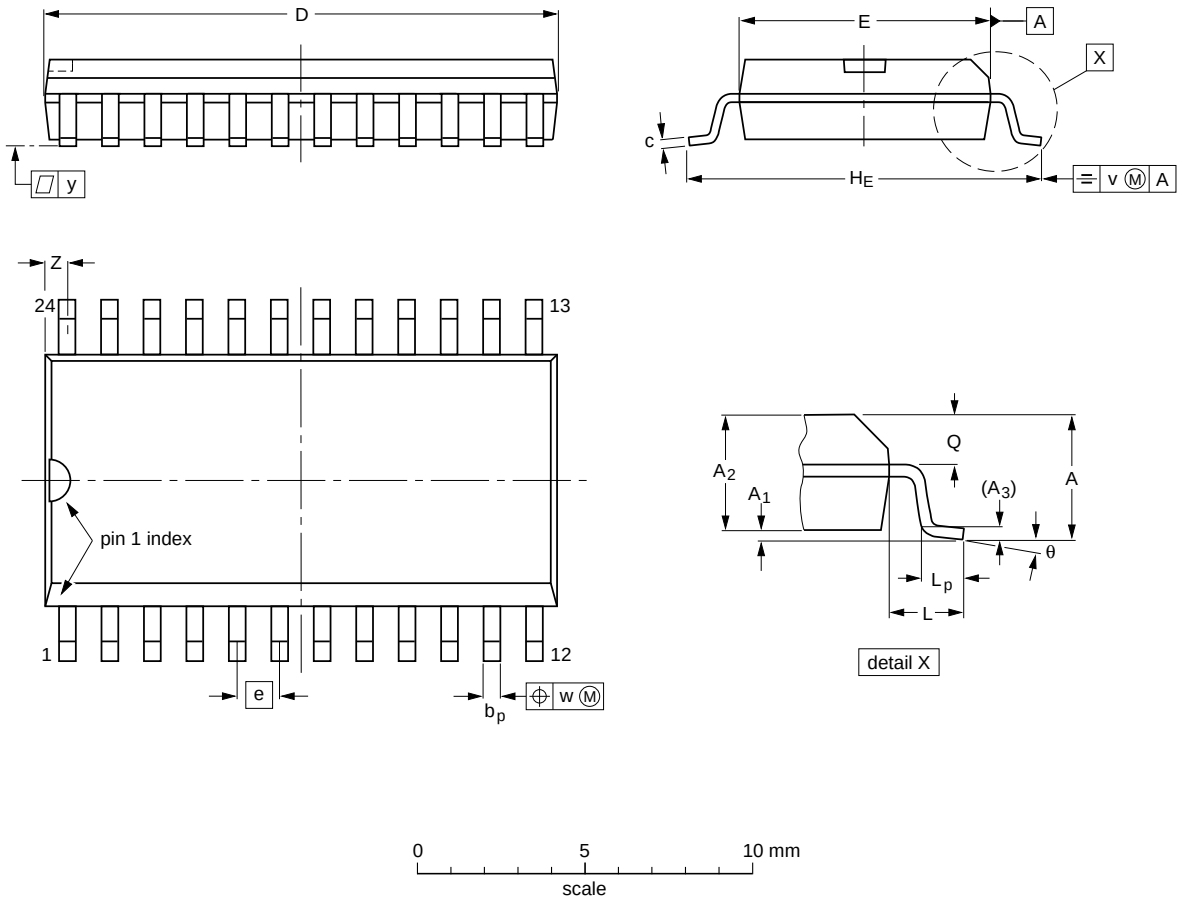
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
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