

# DATA SHEET

## **J108; J109; J110** N-channel silicon junction FETs

Product specification  
Supersedes data of April 1995  
File under Discrete Semiconductors, SC07

1996 Jul 30

# N-channel silicon junction FETs

# J108; J109; J110

### FEATURES

- High speed switching
- Interchangeability of drain and source connections
- Low  $R_{DSon}$  at zero gate voltage ( $<8 \Omega$  for J108).

### APPLICATIONS

- Analog switches
- Choppers and commutators.

### DESCRIPTION

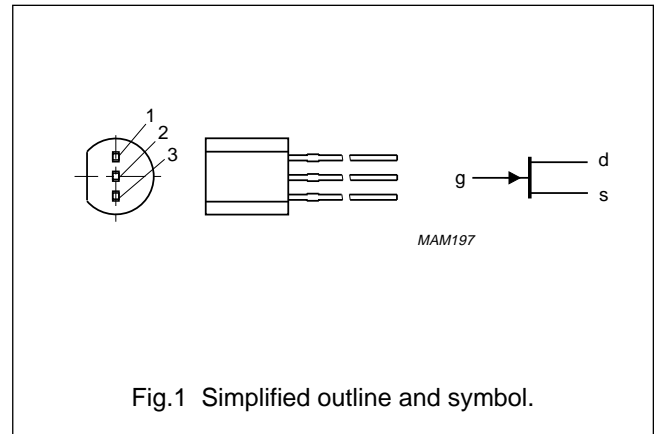
N-channel symmetrical silicon junction field-effect transistors in a TO-92 package.

**CAUTION**

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

### PINNING - TO-92

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	$\pm 25$	V
$V_{GSoff}$	gate-source cut-off voltage	$I_D = 1 \mu A; V_{DS} = 5 V$			
	J108		–3	–10	V
	J109		–2	–6	V
	J110		–0.5	–4	V
$I_{DSS}$	drain current	$V_{GS} = 0; V_{DS} = 5 V$			
	J108		80	–	mA
	J109		40	–	mA
	J110		10	–	mA
$P_{tot}$	total power dissipation	up to $T_{amb} = 50 \text{ }^\circ C$	–	400	mW

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	$\pm 25$	V
$V_{GSO}$	gate-source voltage	open drain	–	–25	V
$V_{GDO}$	gate-drain voltage	open source	–	–25	V
$I_G$	forward gate current (DC)		–	50	mA
$P_{tot}$	total power dissipation	up to $T_{amb} = 50\text{ }^\circ\text{C}$	–	400	mW
$T_{stg}$	storage temperature		–65	150	$^\circ\text{C}$
$T_j$	operating junction temperature		–	150	$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	250	K/W

**STATIC CHARACTERISTICS** $T_j = 25\text{ }^\circ\text{C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = -1\ \mu\text{A}$ ; $V_{DS} = 0$	–	–	–25	V
$V_{GSoff}$	gate-source cut-off voltage	$I_D = 1\ \mu\text{A}$ ; $V_{DS} = 5\ \text{V}$				V
	J108		–3	–	–10	V
	J109		–2	–	–6	V
	J110		–0.5	–	–4	V
$I_{DSS}$	drain current	$V_{GS} = 0$ ; $V_{DS} = 15\ \text{V}$				mA
	J108		80	–	–	mA
	J109		40	–	–	mA
	J110		10	–	–	mA
$I_{GSS}$	gate leakage current	$V_{GS} = -15\ \text{V}$ ; $V_{DS} = 0$	–	–	–3	nA
$I_{DSX}$	drain-source cut-off current	$V_{GS} = -10\ \text{V}$ ; $V_{DS} = 5\ \text{V}$	–	–	3	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 0$ ; $V_{DS} = 100\ \text{mV}$				$\Omega$
	J108		–	–	8	$\Omega$
	J109		–	–	12	$\Omega$
	J110		–	–	18	$\Omega$

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**DYNAMIC CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$C_{is}$	input capacitance	$V_{DS} = 0; V_{GS} = -10\text{ V}; f = 1\text{ MHz}$	15	30	pF
		$V_{DS} = 0; V_{GS} = 0; f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	50	85	pF
$C_{rs}$	reverse transfer capacitance	$V_{DS} = 0; V_{GS} = -10\text{ V}; f = 1\text{ MHz}$	8	15	pF
<b>Switching times; see Fig.2</b>					
$t_d$	delay time	note 1	2	–	ns
$t_{on}$	turn-on time		4	–	ns
$t_s$	storage time		4	–	ns
$t_{off}$	turn-off time		6	–	ns

**Note**

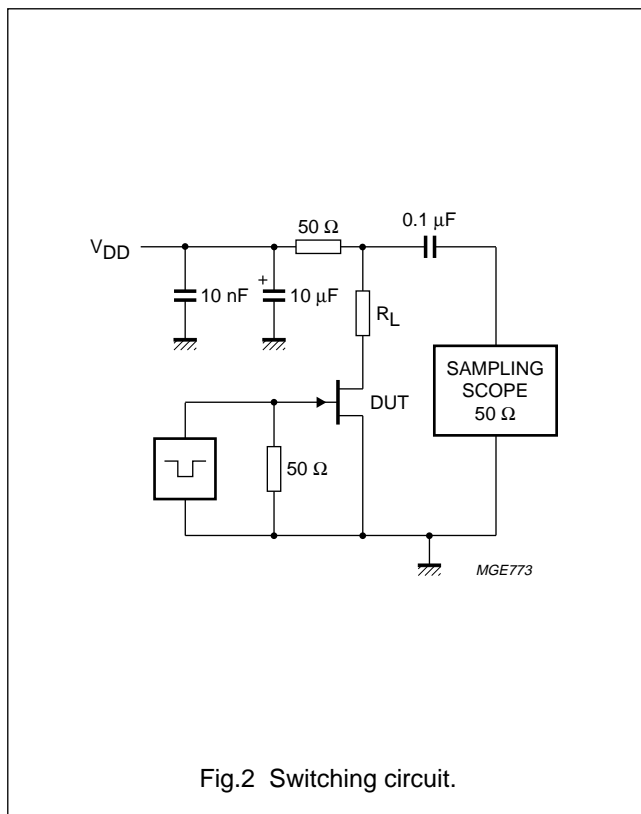
1. Test conditions for switching times are as follows:

$V_{DD} = 1.5\text{ V}; V_{GS} = 0\text{ to }V_{GSoff}$  (all types)

$V_{GSoff} = -12\text{ V}; R_L = 100\text{ }\Omega$  (J108)

$V_{GSoff} = -7\text{ V}; R_L = 100\text{ }\Omega$  (J109)

$V_{GSoff} = -5\text{ V}; R_L = 100\text{ }\Omega$  (J110).



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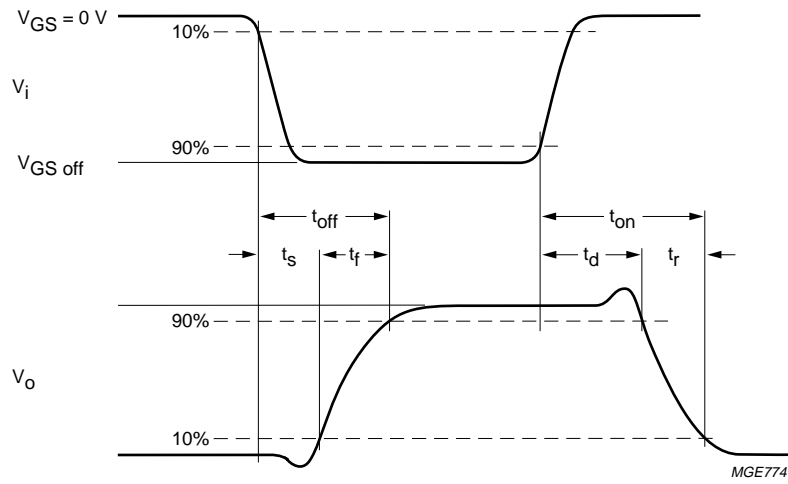


Fig.3 Input and output waveforms.

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## PACKAGE OUTLINE

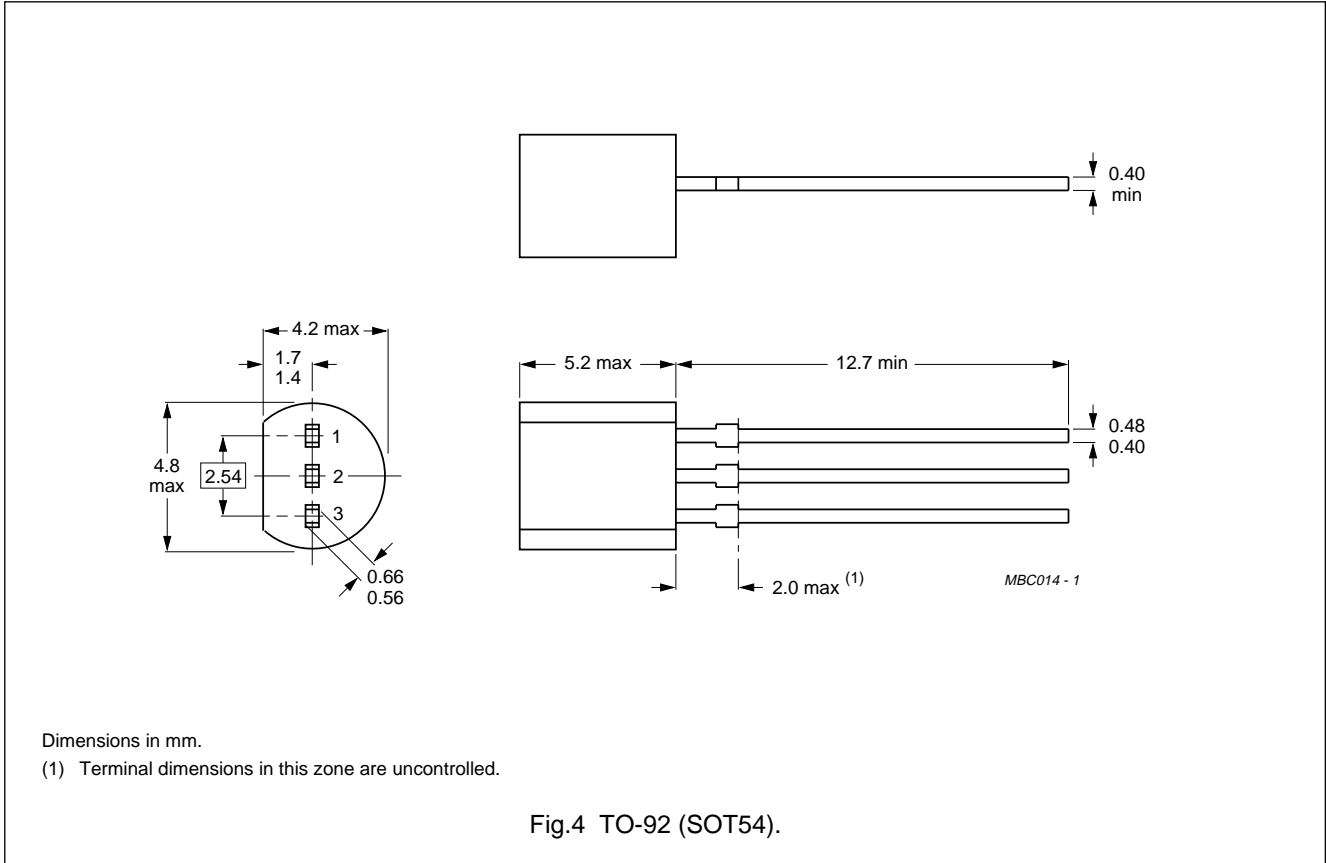


Fig.4 TO-92 (SOT54).

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**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

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