

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT7080 16-bit even/odd parity generator/checker

Product specification
File under Integrated Circuits, IC06

December 1990

16-bit even/odd parity generator/checker

74HC/HCT7080

FEATURES

- Word-length easily expanded by cascading
- Generates either even or odd parity for 16-data bits
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT7080 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7080 are 16-bit parity generators or checkers commonly used to detect errors in high-speed data transmission or data retrieval systems.

The even and odd parity output is available for generating or checking even/odd parity up to 16-bits.

The even/odd parity output (E/\bar{O}) is HIGH when an even number of data inputs (I_0 to I_{15}) are HIGH and the cascade/even-odd-changing input (\bar{X}) is HIGH.

Expansion to larger word sizes is accomplished by connecting the even/odd parity output (E/\bar{O}) to the cascade/even-odd-changing input (\bar{X}) of the final stage.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I_n to E/\bar{O}	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	29	32	ns
	\bar{X} to E/\bar{O}		12	15	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	25	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

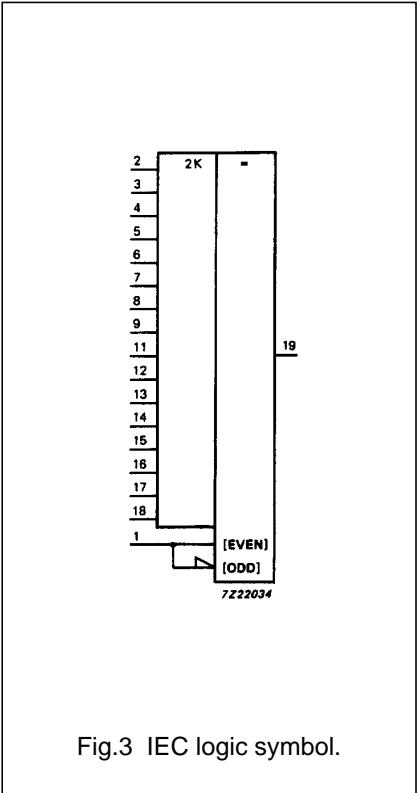
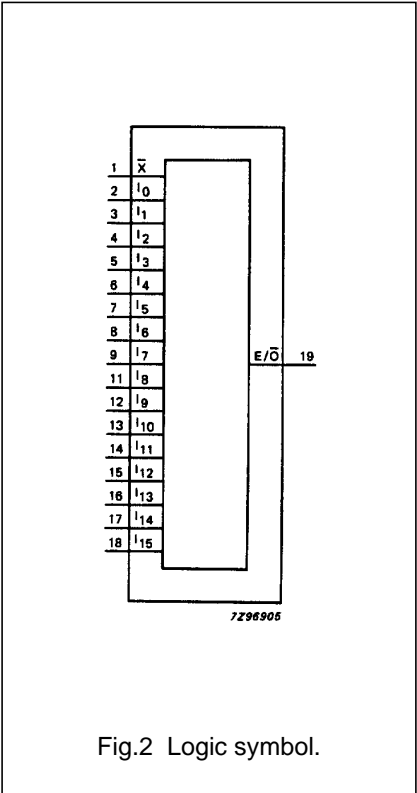
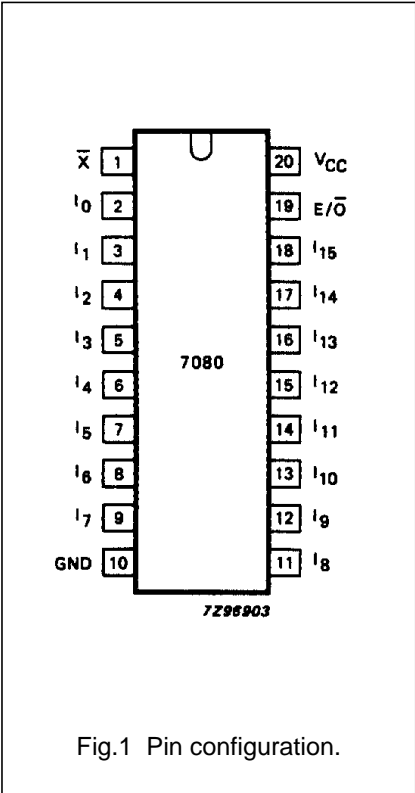
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	\bar{X}	cascade/even-odd-changing input
2, 3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 17, 18	I_0 to I_{15}	data inputs
10	GND	ground (0 V)
19	E/\bar{O}	even/odd parity output
20	V_{CC}	positive supply voltage



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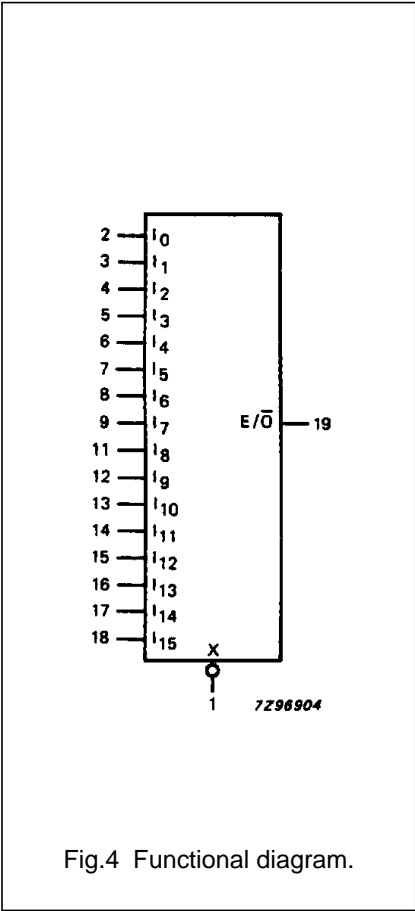


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
I_n	\bar{X}	E/\bar{O}
$\Sigma = E$	H	H
	L	L
$\Sigma \neq E$	H	L
	L	H

Notes

- 1. H = HIGH voltage level
- L = LOW voltage level
- E = even

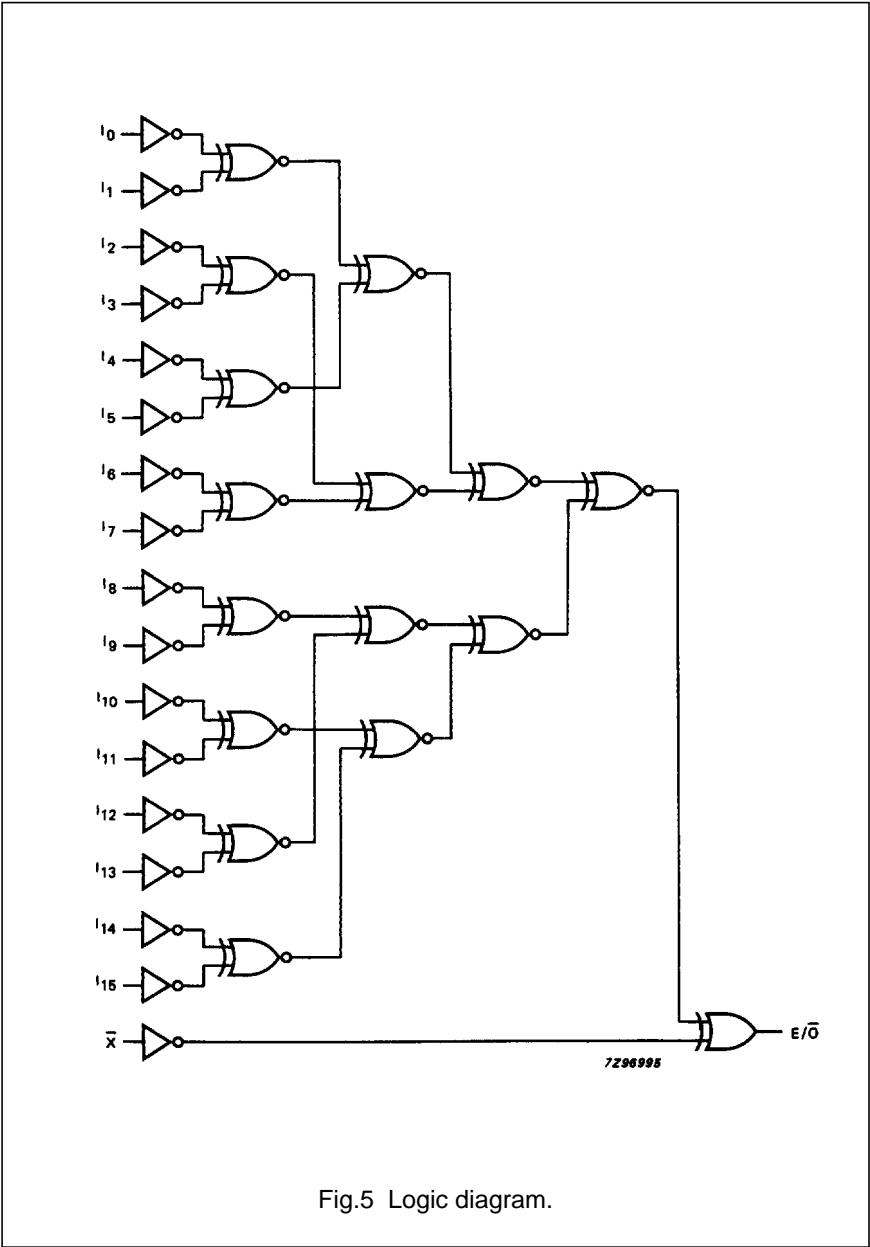


Fig.5 Logic diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay I _n to E/ \overline{O}		91 33 26	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig.7
t _{PHL} / t _{PLH}	propagation delay \overline{X} to E/ \overline{O}		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I _n	1.0
\bar{X}	1.0

AC CHARACTERISTICS FOR 74HCT

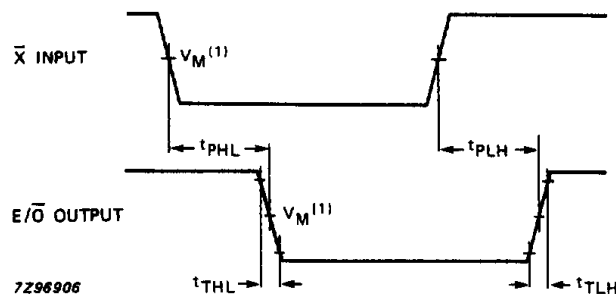
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay I _n to E/ \bar{O}		37	63		79		95	ns	4.5	Fig.7
t _{PHL} / t _{PLH}	propagation delay \bar{X} to E/ \bar{O}		18	32		40		48	ns	4.5	Fig.6
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

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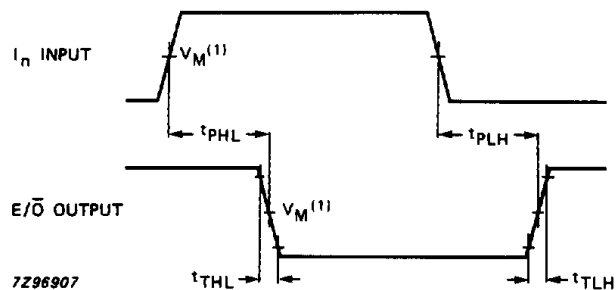
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AC WAVEFORMS



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.6 Waveforms showing the cascade/even-odd-changing input (\bar{X}) to the even/odd parity output (E/\bar{O}) propagation delays and the output transition times.



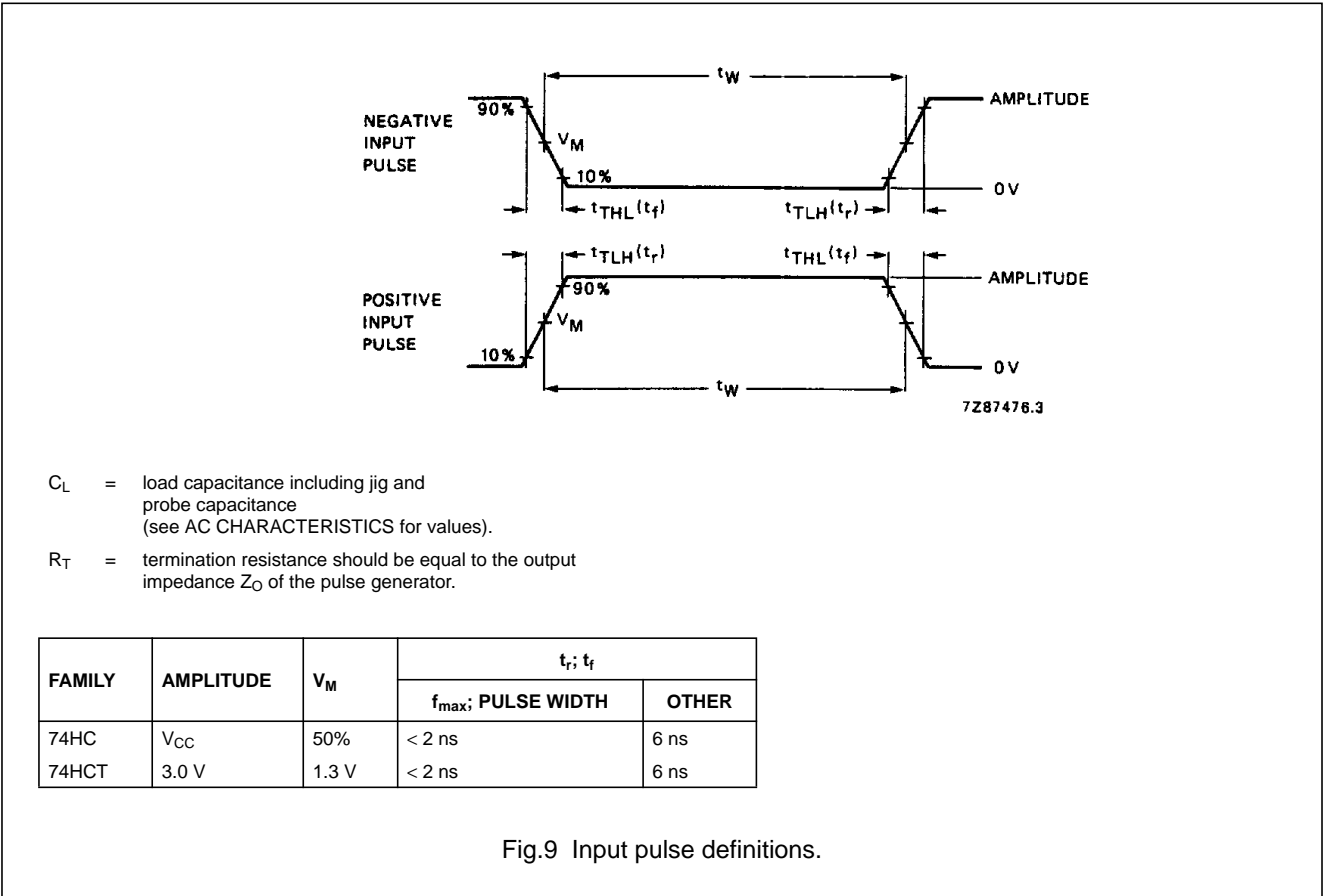
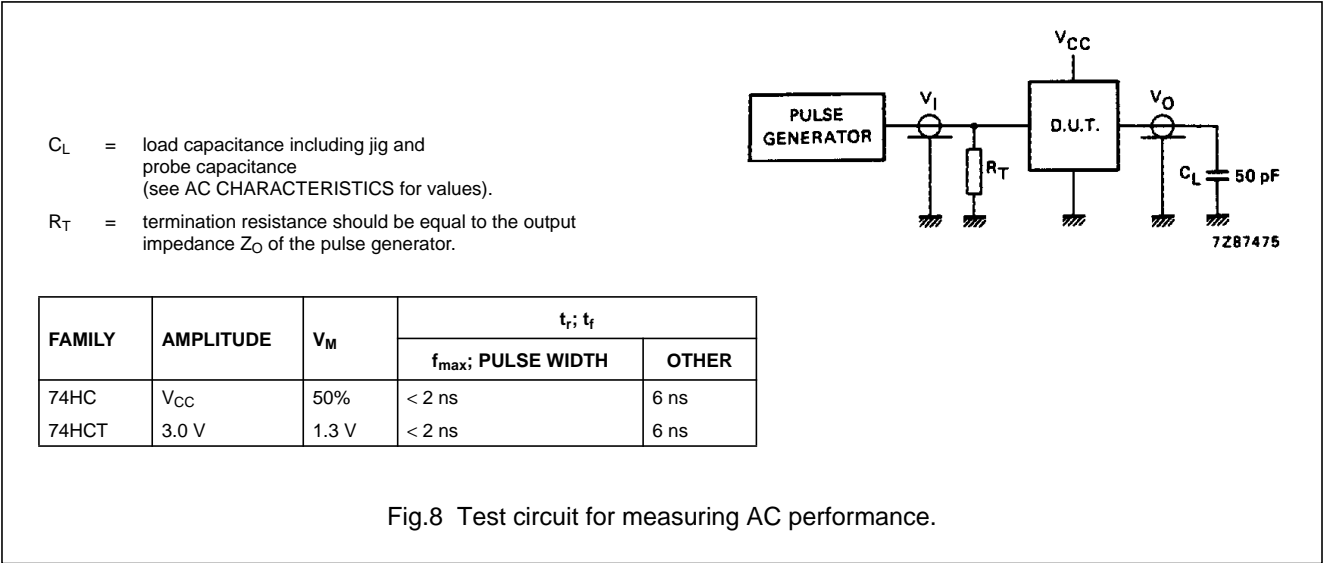
(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.7 Waveforms showing the data inputs (I_n) to the even/odd parity output (E/\bar{O}) propagation delays and the output transition times.

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TEST CIRCUIT AND WAVEFORMS



PACKAGE OUTLINES

See “74HC/HCT/HCU/HCMOS Logic Package Outlines”.