

# DATA SHEET

## **74F552**

Octal registered transceiver with parity  
and flags (3-State)

Product specification

1991 Jan 02

IC15 Data Handbook

# Octal registered transceiver with parity and flags (3-State)

# 74F552

## FEATURES

- 8-bit bidirectional I/O port with handshake
- Register status flag flip-flops
- Separate clock enable and output enable
- Parity generation and parity check
- B outputs and parity output sink 64mA

## DESCRIPTION

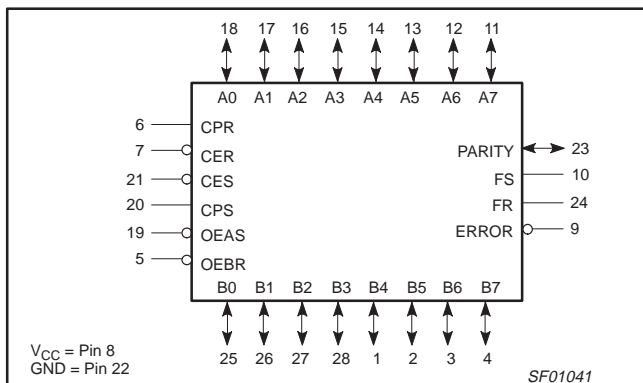
The 74F522 Octal Registered Transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock (CPR, CPS) and Clock Enable ( $\overline{CER}$ ,  $\overline{CES}$ ) inputs, as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the Output Enable returns to High after reading the output port. Each register has a separate Output Enable ( $\overline{OEAS}$ ,  $\overline{OEBR}$ ) for its 3-State buffer. The separate Clocks, Flags and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data is transferred from the A port to the B port, a parity bit is generated. On the other hand, when data is transferred from the B port to the A port, the parity of input data on B0–B7 is checked.

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F552	85MHz	120mA

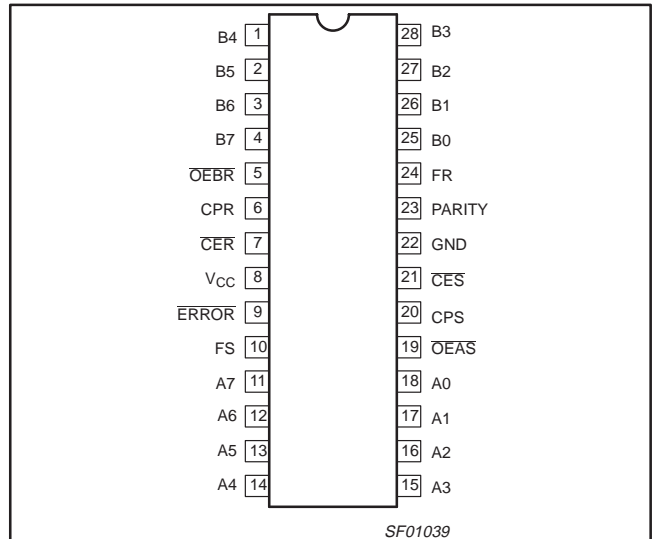
## ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG DWG #
28-Pin Plastic DIP (600mil)	N74F552N	SOT117-2
28-Pin Plastic SOL	N74F552D	SOT136-1

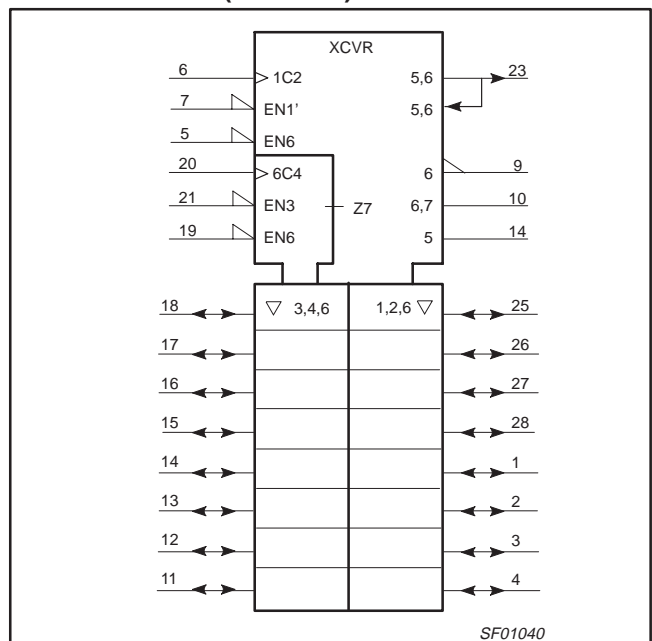
## LOGIC SYMBOL



## PIN CONFIGURATION



## LOGIC SYMBOL (IEEE/IEC)



# Octal registered transceiver with parity and flags (3-State)

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## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0–A7	A Data inputs	3.5/1.0	70µA/0.6mA
B0–B7	B Data inputs	3.5/1.0	70µA/0.6mA
CPR	R registers clock input (active rising edge)	1.0/1.0	20µA/0.6mA
CPS	S registers clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{CER}$	R registers clock Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CES}$	S registers clock Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE\overline{B}R}$	A-to-B Output Enable input (active Low) and clear FS output (active Low)	1.0/2.0	20µA/1.2mA
$\overline{OEAS}$	B-to-A Output Enable input (active Low) and clear FR output (active Low)	1.0/2.0	20µA/1.2mA
PARITY	Parity bit transceiver input	3.5/1.0	70µA/0.6mA
	Parity bit transceiver output	750/106.7	15mA/64mA
$\overline{ERROR}$	Parity check output (active Low)	50/33.3	1.0mA/20mA
A0–A7	A Data outputs	150/40	3.0mA/24mA
B0–B7	B Data outputs	750/106.7	15mA/64mA
FR	A-to-B Status Flag output (active High)	50/33.3	1.0mA/20mA
FS	B-to-A Status Flag output (active High)	50/33.3	1.0mA/20mA

**NOTE:** One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

## FUNCTIONAL DESCRIPTION

Data applied to the A inputs are entered and stored on the rising edge of the CPR clock pulse, provided that the  $\overline{CER}$  is Low; simultaneously, the status flip-flop is set and the A-to-B flag (FR) output goes High. As the  $\overline{CER}$  returns to High, the data will be held in R register. This data entered from the A inputs will appear at the B port I/O pins after the  $\overline{OE\overline{B}R}$  has gone Low. When  $\overline{OE\overline{B}R}$  is Low, a parity bit appears at the PARITY pin, which will be set High when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data is assimilated, the receiving system clears the flag FR, by changing the signal at the  $\overline{OE\overline{B}R}$  pin from Low to High. Data flow from B-to-A proceeds in the same manner described for A-to-B flow. A Low at the  $\overline{CES}$  pin and a Low-to-High transition at the CPS pin enters the B input data and the parity input data into the S register and the parity register respectively and set the flag output FS to High. A Low signal at the  $\overline{OEAS}$  pin enables the A port I/O pins and a Low-to-High transition of the  $\overline{OEAS}$  signal clears the FS flag. When  $\overline{OEAS}$  is Low, the parity check output  $\overline{ERROR}$  will be High if there is an odd number of 1s at the Q outputs of the S register and the parity register.

## R or S REGISTER FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
An or Bn	CPX	$\overline{CEX}$	INTERNAL Q	
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	
X	↑	L	NC	Keep old data

H = High voltage level  
 L = Low voltage level  
 NC= No change  
 X = Don't care  
**X = R or S for CPX and CEX**  
 ↑ = Low-to-High transition  
 † = Not Low-to-High transition

## OUTPUT CONTROL TABLE

INPUT	OUTPUTS		OPERATING MODE
	$\overline{OE\overline{X}}$	INTERNAL Q	
H	X	Z	Disable outputs
L	L	L	Enable output
L	H	H	

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
**XX= AS or BR**  
 Z = High impedance "off" state

# Octal registered transceiver with parity and flags (3-State)

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**R or S FLAG FUNCTION TABLE**

INPUTS			OUTPUTS	OPERATING MODE
CEX	CPX	OEEX	FR or FS	
H	X	↑	NC	Hold flag
L	↑	↑	H	Set flag
X	X	↑	L	Clear flag

H = High voltage level  
 L = Low voltage level  
 NC= No change  
 X = Don't care  
**X = R or S for CPX and CEX**  
**XX= AS or BR**  
 ↑ = Low-to-High transition  
 ↑̂ = Not Low-to-High transition

**PARITY GENERATION FUNCTION TABLE**

INPUTS		OUTPUTS		OPERATING MODE
OE̅BR	CPR	Number of Highs in the Q outputs of the R register	PARITY	
H	X	X	Z	Hold flag
L	↑	0,2,4,6,8	H	Load data
L	↑	1,3,5,7	L	

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 Z = High impedance "off" state  
 ↑ = Low-to-High transition

**PARITY CHECK FUNCTION TABLE**

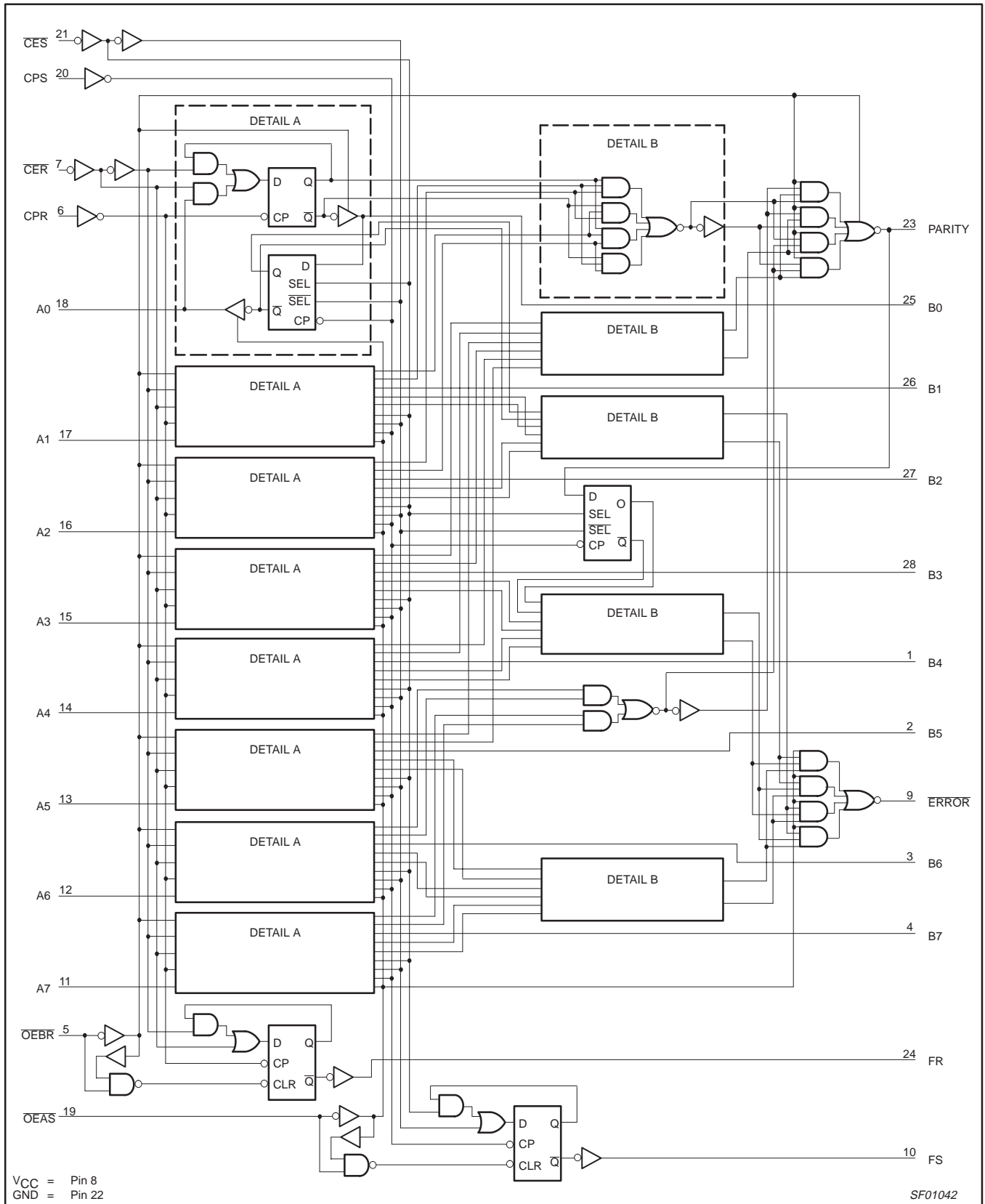
INPUTS			OUTPUTS		OPERATING MODE
OEAS	CPS	PARITY	Number of Highs in the Q outputs of the R register	ERROR	
H	X	X	X	H	Parity check
L	↑	L	0,2,4,6,8	L	
L	↑	L	1,3,5,7	H	
L	↑	H	0,2,4,6,8	H	
L	↑	H	1,3,5,7	L	

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 ↑ = Low-to-High transition

# Octal registered transceiver with parity and flags (3-State)

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## LOGIC DIAGRAM



SF01042

## Octal registered transceiver with parity and flags (3-State)

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT	
$V_{CC}$	Supply voltage	-0.5 to +7.0	V	
$V_{IN}$	Input voltage	-0.5 to +7.0	V	
$I_{IN}$	Input current	-30 to + $V_{CC}$	mA	
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to + $V_{CC}$	V	
$I_{OUT}$	Current applied to output in Low output state	FR, FS, ERROR	40	mA
		A0-A7	48	mA
		B0-B7, PARITY	128	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C	
$T_{stg}$	Storage temperature	-65 to +150	°C	

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current	FR, FS, ERROR		-1	mA
		A0-A7		-3	mA
		B0-B7, PARITY		-15	mA
$I_{OL}$	Low-level output current	FR, FS, ERROR		20	mA
		A0-A7		24	mA
		B0-B7, PARITY		64	mA
$T_{amb}$	Operating free-air temperature range	0		70	°C

## Octal registered transceiver with parity and flags (3-State)

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**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>NO TAG</sup>		LIMITS			UNIT	
					MIN	TYP NO TAG	MAX		
$V_{OH}$	High-level output voltage	FR, FS, $\overline{\text{ERROR}}$	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}$	$I_{OH} = -1\text{mA}$	$\pm 10\%V_{CC}$	2.5			V
					$\pm 5\%V_{CC}$	2.7	3.4		V
		A0–A7		$I_{OH} = -3\text{mA}$	$\pm 10\%V_{CC}$	2.4			V
					$\pm 5\%V_{CC}$	2.7	3.3		V
		B0–B7, PARITY		$I_{OH} = -15\text{mA}$	$\pm 10\%V_{CC}$	2.0			V
					$\pm 5\%V_{CC}$	2.0			V
$V_{OL}$	Low-level output voltage	FR, FS, $\overline{\text{ERROR}}$	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}$	$I_{OL} = 20\text{mA}$	$\pm 10\%V_{CC}$		0.30	0.50	V
					$\pm 5\%V_{CC}$		0.30	0.50	V
		A0–A7		$I_{OL} = 24\text{mA}$	$\pm 10\%V_{CC}$		0.35	0.50	V
					$\pm 5\%V_{CC}$		0.35	0.50	V
		B0–B7, PARITY		$I_{OL} = 48\text{mA}$	$\pm 10\%V_{CC}$		0.38	0.55	V
					$\pm 5\%V_{CC}$		0.42	0.55	V
$V_{IK}$	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = I_{IK}$			-0.73	-1.2	V	
$I_I$	Input current at maximum input voltage	others	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$				100	$\mu\text{A}$	
		A0–A7, B0–B7, PARITY	$V_{CC} = 5.5\text{V}, V_I = 5.5\text{V}$				1	mA	
$I_{IH}$	High-level input current	others except A0–A7, B0–B7, PARITY	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$				20	$\mu\text{A}$	
$I_{IL}$	Low-level input current	others	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$				-0.6	mA	
		$\overline{\text{OEAS}}, \overline{\text{OEBA}}$					-1.2	mA	
$I_{OZH} + I_{IH}$	Off-state output current High-level voltage applied	A0–A7, B0–B7, PARITY	$V_{CC} = \text{MAX}, V_O = 2.7\text{V}$				70	$\mu\text{A}$	
$I_{OZL} + I_{IL}$	Off-state output current Low-level voltage applied		$V_{CC} = \text{MAX}, V_O = 0.5\text{V}$				-600	$\mu\text{A}$	
$I_{OS}$	Short-circuit output current <sup>NO TAG</sup>	A0–A7, FS, FR, $\overline{\text{ERROR}}$	$V_{CC} = \text{MAX}$		-60		-150	mA	
		B0–B7, PARITY			-100		-225	mA	
$I_{CC}$	Supply current (total)	$I_{CCH}$	$V_{CC} = \text{MAX}$			115	170	mA	
		$I_{CCL}$				125	185	mA	
		$I_{CCZ}$				120	180	mA	

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{\text{amb}} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  should be performed last.

## Octal registered transceiver with parity and flags (3-State)

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum Clock Frequency	Waveform 1	70	85		60		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CPS to An or CPR to Bn	Waveform 1	3.5 4.0	5.0 6.0	8.0 9.0	3.0 3.5	8.5 9.0	ns ns
t <sub>PLH</sub>	Propagation delay CPS to FS or CPR to FR	Waveform 1	3.0	5.0	7.5	2.5	8.5	ns
t <sub>PHL</sub>	Propagation delay OEAS to FS or OE $\overline{\text{BR}}$ to FR	Waveform 2	4.0	6.0	8.5	3.5	9.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CPS to ERROR	Waveform 4	6.5 7.5	13.0 11.5	16.5 15.0	6.0 7.0	18.0 16.0	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CPR to PARITY	Waveform 4	6.5 10.5	8.5 13.5	11.0 17.0	5.5 10.0	12.5 18.0	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay OEAS to ERROR	Waveform NO TAG	3.5 3.0	5.5 5.0	8.0 7.0	3.0 2.5	8.5 8.0	ns ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time OEAS to An or OE $\overline{\text{BR}}$ to Bn	Waveform NO TAG Waveform NO TAG	2.5 4.0	4.0 6.5	7.0 9.5	2.0 4.0	8.0 10.5	ns ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time OEAS to An or OE $\overline{\text{BR}}$ to Bn	Waveform NO TAG Waveform NO TAG	2.0 2.0	4.0 3.5	7.0 7.0	1.5 1.5	8.5 7.5	ns ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time OE $\overline{\text{BR}}$ to PARITY	Waveform NO TAG Waveform NO TAG	2.0 4.0	4.0 5.5	7.0 8.0	2.0 3.0	7.5 9.0	ns ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time OE $\overline{\text{BR}}$ to PARITY	Waveform NO TAG Waveform NO TAG	2.0 2.0	4.0 4.0	7.0 7.5	2.0 2.0	7.5 8.0	ns ns

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low An or Bn or PARITY to CPS or CPR	Waveform 5	7.5 4.5			8.5 5.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low An or Bn or PARITY to CPS or CPR	Waveform 5	0 0			0 0		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low CES to CPS or CER to CPR	Waveform 5	7.0 7.0			7.5 7.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low CES to CPS or CER to CPR	Waveform 5	0 0			0 0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CPS or CPR Pulse width, High or Low	Waveform 1	5.0 6.5			6.5 7.5		ns
t <sub>REC</sub>	Recovery time OE $\overline{\text{BR}}$ to CPR or OEAS to CPS	Waveform 6	14.5			16.5		ns



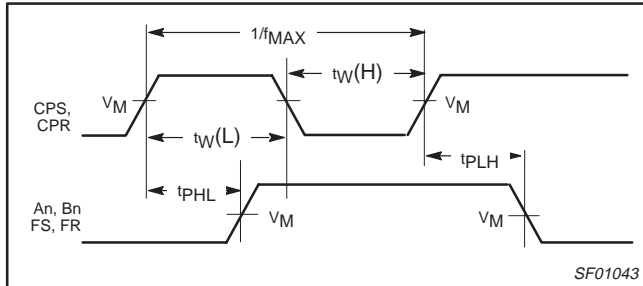
# Octal registered transceiver with parity and flags (3-State)

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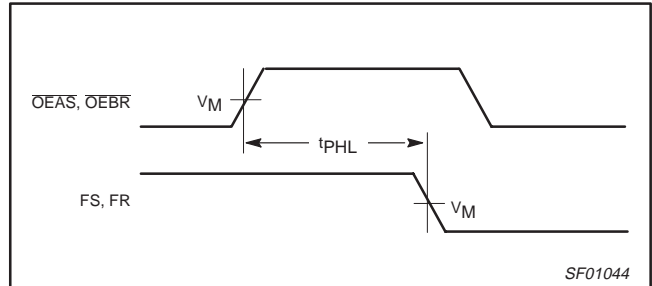
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .

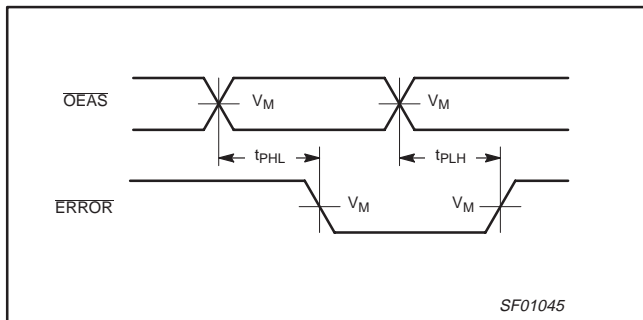
The shaded areas indicate when the input is permitted to change for predictable output.



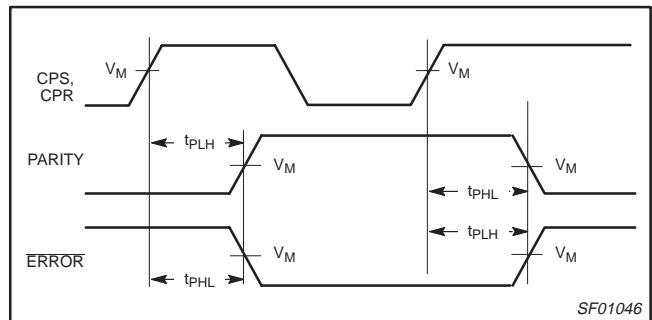
**Waveform 1. Propagation Delay, Clock Input to Output and Maximum Clock Frequency**



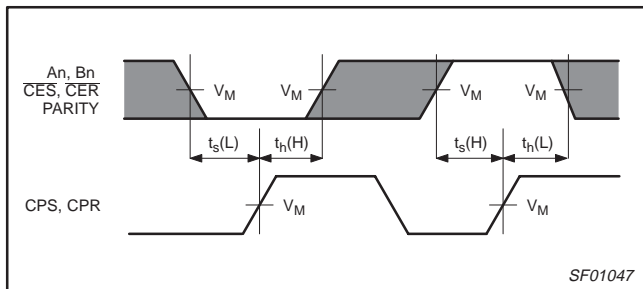
**Waveform 2. Propagation Delay, Output Enable to Flag Output**



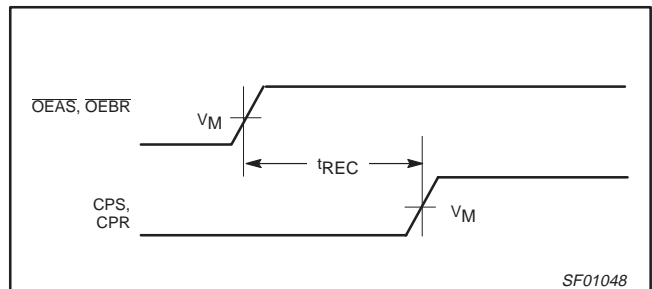
**Waveform 3. Propagation Delay, Output Enable to ERROR**



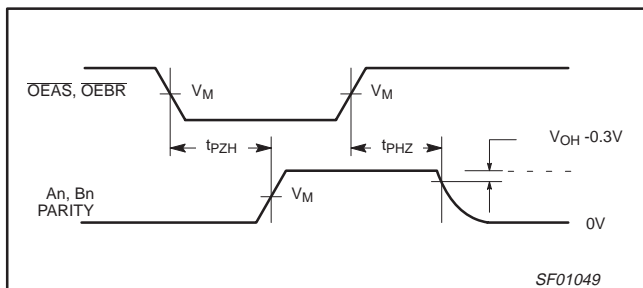
**Waveform 4. Propagation Delay, Clock to PARITY and ERROR**



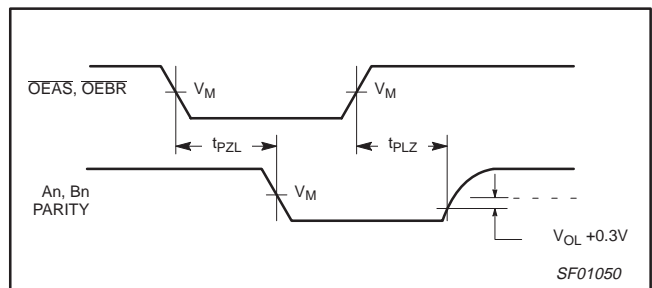
**Waveform 5. Data Setup and Hold Times**



**Waveform 6. Recovery Time from Output Enable to Clock**



**Waveform 7. 3-State Output Enable Time to High Level and Output Disable Time from High Level**

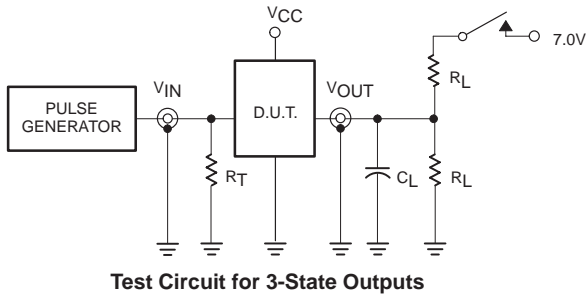


**Waveform 8. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

# Octal registered transceiver with parity and flags (3-State)

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## TEST CIRCUIT AND WAVEFORM



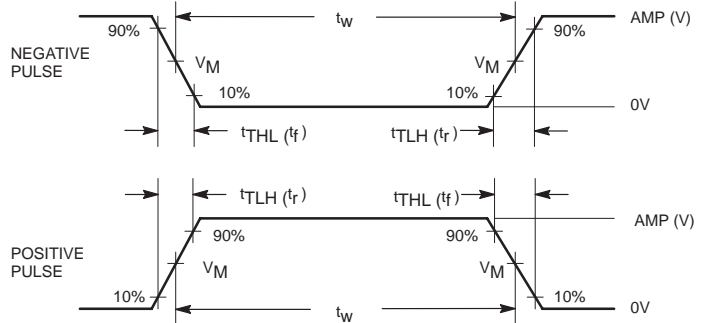
Test Circuit for 3-State Outputs

### SWITCH POSITION

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

### DEFINITIONS:

- $R_L$  = Load resistor; see AC electrical characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

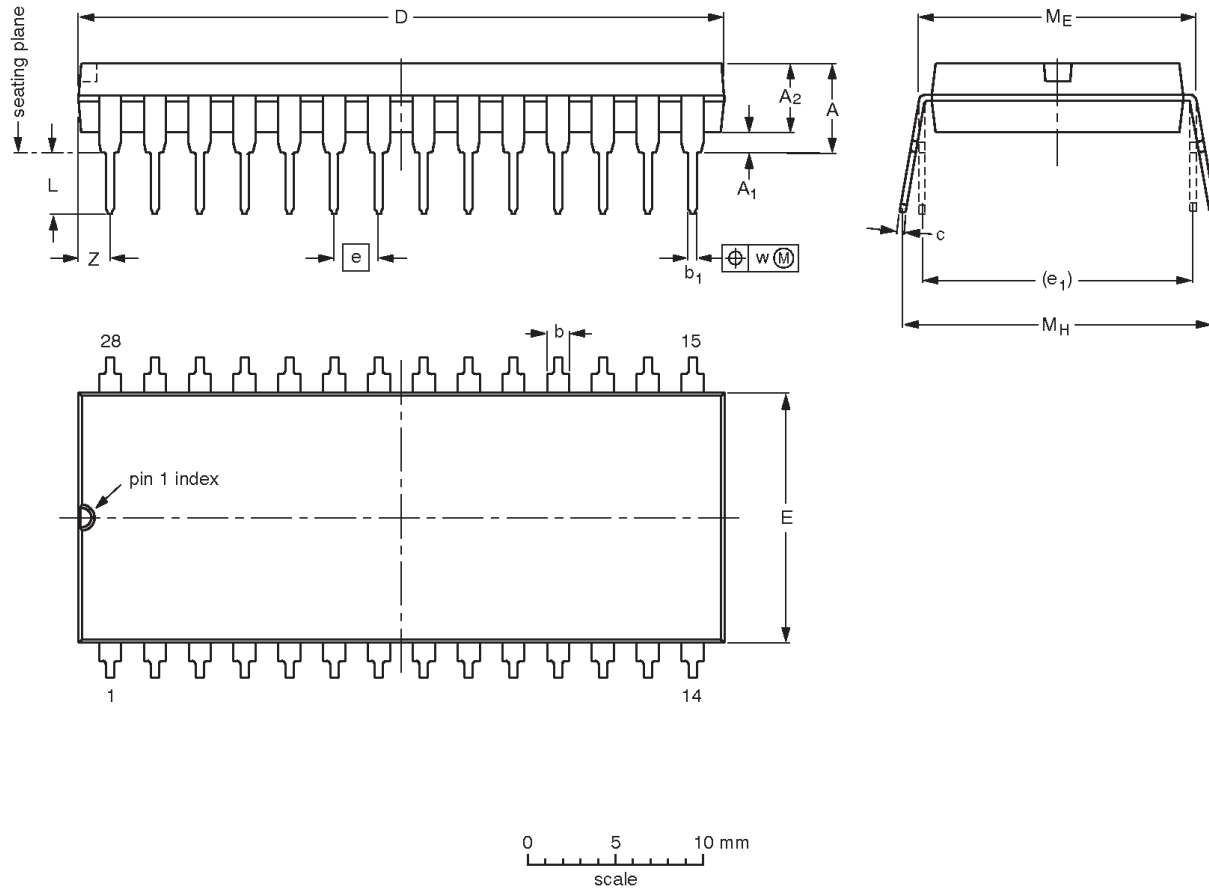
SF00777

# Octal registered transceiver with parity and flags (3-State)

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DIP28: plastic dual in-line package; 28 leads (600 mil); long body

SOT117-2



**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	5.08	0.51	3.94	1.63 1.14	0.56 0.43	0.38 0.25	37.08 35.94	14.22 13.84	2.54	15.24	3.51 3.05	15.75 15.24	17.65 15.24	0.25	2.10
inches	0.200	0.020	0.155	0.064 0.045	0.022 0.017	0.015 0.010	1.460 1.415	0.560 0.545	0.100	0.600	0.138 0.120	0.62 0.60	0.695 0.600	0.01	0.083

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

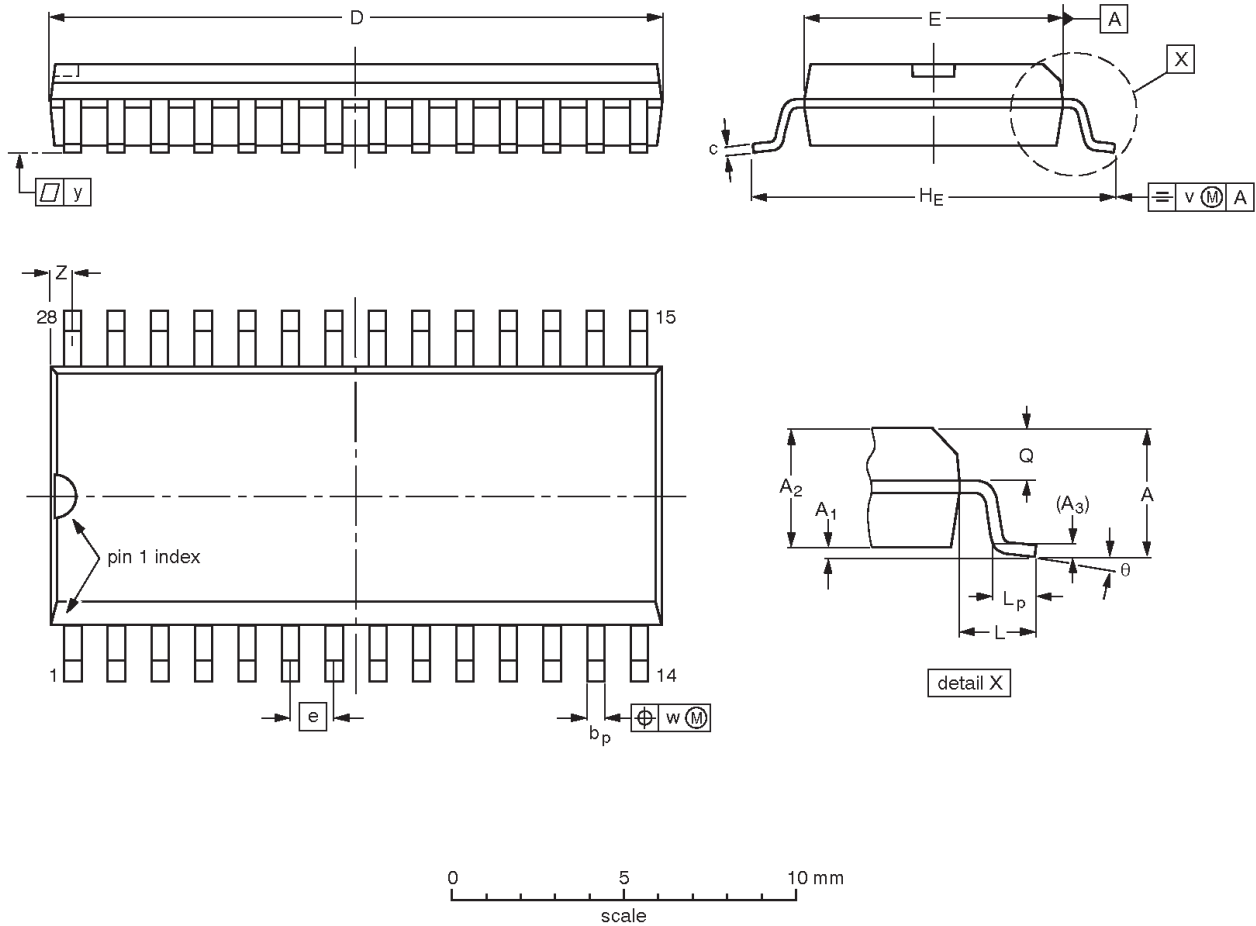
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-2		MS-011AB				95-03-11

# Octal registered transceiver with parity and flags (3-State)

## 74F552

**SO28:** plastic small outline package; 28 leads; body width 7.5mm

**SOT136-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	$\theta$
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				95-01-24 97-05-22

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Octal registered transceiver with parity and flags (3-State)

74F552

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**NOTES**

## Octal registered transceiver with parity and flags (3-State)

74F552

**Data sheet status**

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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