

DATA SHEET

74F112

Dual J-K negative edge-triggered flip-flop

Product specification

1990 Feb 09

IC15 Data Handbook

Dual J-K negative edge-triggered flip-flop

74F112

FEATURE

- Industrial temperature range available (-40°C to +85°C)

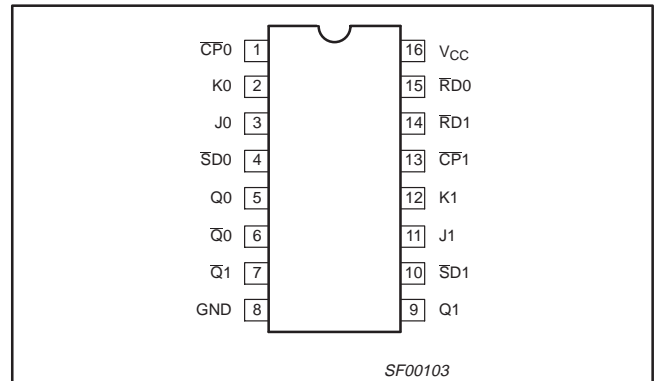
DESCRIPTION

The 74F112, Dual Negative Edge-Triggered JK-Type Flip-Flop, feature individual J, K, Clock (\overline{CP}_n), Set (\overline{SD}) and Reset (\overline{RD}) inputs, true (Q_n) and complementary (\overline{Q}_n) outputs.

The \overline{SD} and \overline{RD} inputs, when Low, set or reset the outputs as shown in the Function Table, regardless of the level at the other inputs.

A High level on the clock (\overline{CP}_n) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the \overline{CP}_n is High and flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the \overline{CP}_n .

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F112	100MHz	15mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^\circ C$ to $+70^\circ C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = -40^\circ C$ to $+85^\circ C$	
16-pin plastic DIP	N74F112N	I74F112N	SOT38-4
16-pin plastic SO	N74F112D	I74F112D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/1.0	20µA/0.6mA
K0, K1	K inputs	1.0/1.0	20µA/0.6mA
$\overline{SD}_0, \overline{SD}_1$	Set inputs (active Low)	1.0/5.0	20µA/3.0mA
$\overline{RD}_0, \overline{RD}_1$	Reset inputs (active Low)	1.0/5.0	20µA/3.0mA
$\overline{CP}_0, \overline{CP}_1$	Clock Pulse input (active falling edge)	1.0/4.0	20µA/2.4mA
Q0, \overline{Q}_0 ; Q1, \overline{Q}_1	Data outputs	50/33	1.0mA/20mA

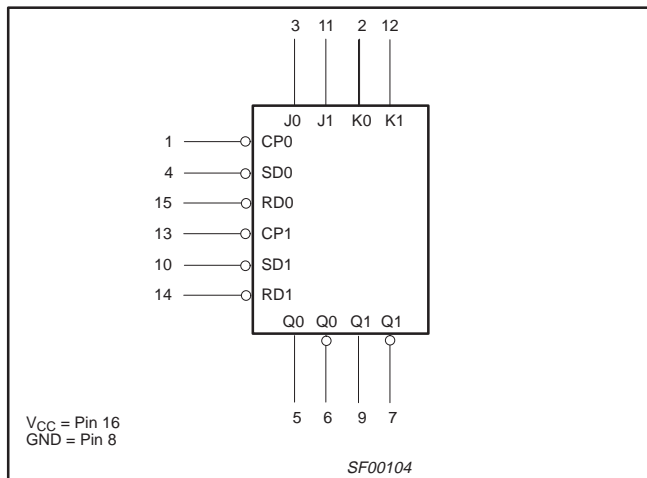
NOTE:

One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

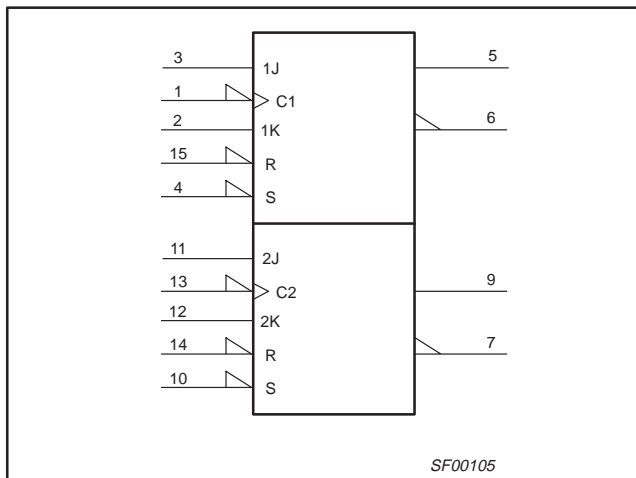
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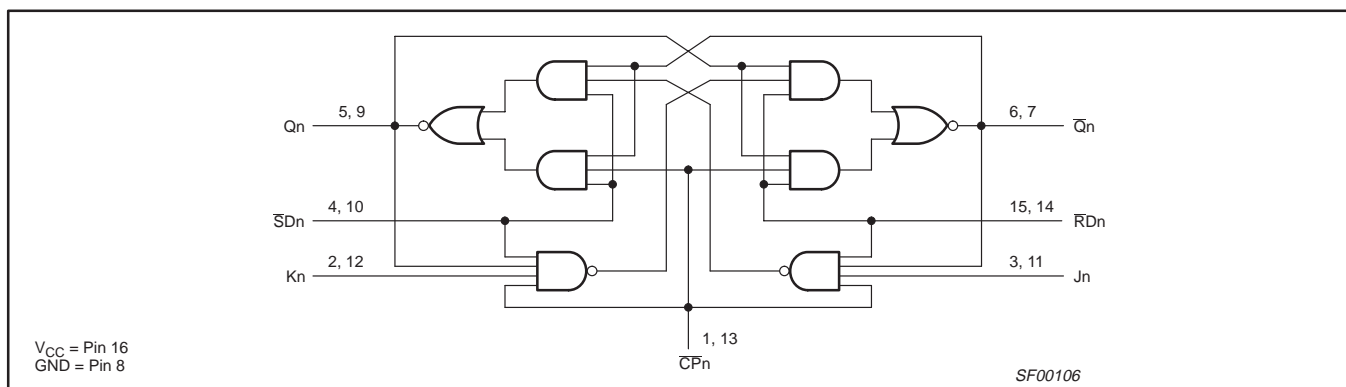
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
SD	RD	CP	J	K	Q	Q̄	
L	H	X	X	X	H	L	Asynchronous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H*	H*	Undetermined *
H	H	↓	h	h	q̄	q	Toggle
H	H	↓	l	h	L	H	Load "0" (Reset)
H	H	↓	h	l	H	L	Load "1" (Set)
H	H	↓	l	l	q	q̄	Hold "no change"
H	H	H	X	X	Q	Q̄	Hold "no change"

H = High voltage level

h = High voltage level one setup time prior to High-to-Low clock transition

L = Low voltage level

l = Low voltage level one setup time prior to High-to-Low clock transition

q = Lower case letters indicate the state of the reference output prior to the High-to-Low clock transition

X = Don't care

↓ = High-to-Low clock transition

* = Both outputs will be High while both SD and RD are Low, but the output states are unpredictable if SD and RD go High simultaneously.

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT	
V_{CC}	Supply voltage		-0.5 to +7.0	V	
V_{IN}	Input voltage		-0.5 to +7.0	V	
I_{IN}	Input current		-30 to +5	mA	
V_{OUT}	Voltage applied to output in High output state		-0.5 to V_{CC}	V	
I_{OUT}	Current applied to output in Low output state		40	mA	
T_{amb}	Operating free-air temperature range		Commercial range	0 to +70	°C
			Industrial range	-40 to +85	°C
T_{stg}	Storage temperature range		-65 to +150	°C	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT	
		MIN	NOM	MAX		
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{IH}	High-level input voltage	2.0			V	
V_{IL}	Low-level input voltage			0.8	V	
I_{IK}	Input clamp current			-18	mA	
I_{OH}	High-level output current			-1	mA	
I_{OL}	Low-level output current			20	mA	
T_{amb}	Operating free-air temperature range		Commercial range	0	+70	°C
			Industrial range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT	
			MIN	TYP ²	MAX		
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$	2.5		V	
		$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 5\%V_{CC}$	2.7	3.4		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35	V	
		$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\%V_{CC}$		0.35		
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$			100	μA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$			20	μA	
I_{IL}	Low-level input current	Jn, Kn			-0.6	mA	
		$\overline{\text{CPn}}$	$V_{CC} = \text{MAX}, V_I = 0.5V$			-2.4	mA
		$\overline{\text{SDn}}, \text{RDn}$				-3.0	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$		-60	-150	mA	
I_{CC}	Supply current (total) ⁴	$V_{CC} = \text{MAX}$		15	21	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Measure I_{CC} with the clock input grounded and all outputs open, with the Q and \overline{Q} outputs High in turn.

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AC ELECTRICAL CHARACTERISTICS

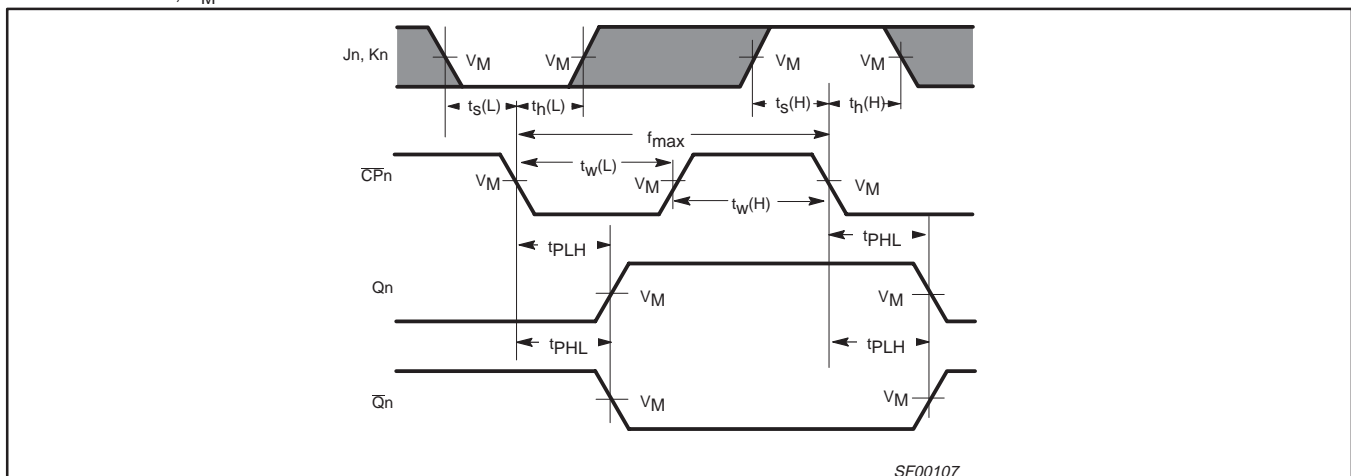
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$V_{CC} = +5.0V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$			$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$		$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = -40^{\circ}C \text{ to } +85^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
f_{MAX}	Maximum clock frequency	Waveform 1	85	100		80		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\bar{Q}n$	Waveform 1	2.0 2.0	5.0 5.0	6.5 6.5	2.0 2.0	7.5 7.5	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{S}Dn, \bar{R}D$ to Qn or $\bar{Q}n$	Waveform 2,3	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	1.5 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$V_{CC} = +5.0V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$			$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$		$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = -40^{\circ}C \text{ to } +85^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
$t_{S(H)}$ $t_{S(L)}$	Setup time, High or Low Jn, Kn to $\bar{C}P$	Waveform 1	4.0 3.5			5.0 4.0			5.0 4.0	ns
$t_{H(H)}$ $t_{H(L)}$	Hold time, High or Low Jn, Kn to $\bar{C}P$	Waveform 1	0.0 0.0			0.0 0.0			0.0 0.0	ns
$t_{W(H)}$ $t_{W(L)}$	$\bar{C}P$ Pulse width High or Low	Waveform 1	4.5 4.5			5.0 5.0			5.0 5.0	ns
$t_{W(L)}$	$\bar{S}Dn, \bar{R}D$ Pulse width Low	Waveform 2,3	4.5			5.0			5.0	ns
t_{REC}	Recovery time $\bar{S}Dn, \bar{R}D$ to $\bar{C}P$	Waveform 2,3	4.5			5.0			5.0	ns

AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

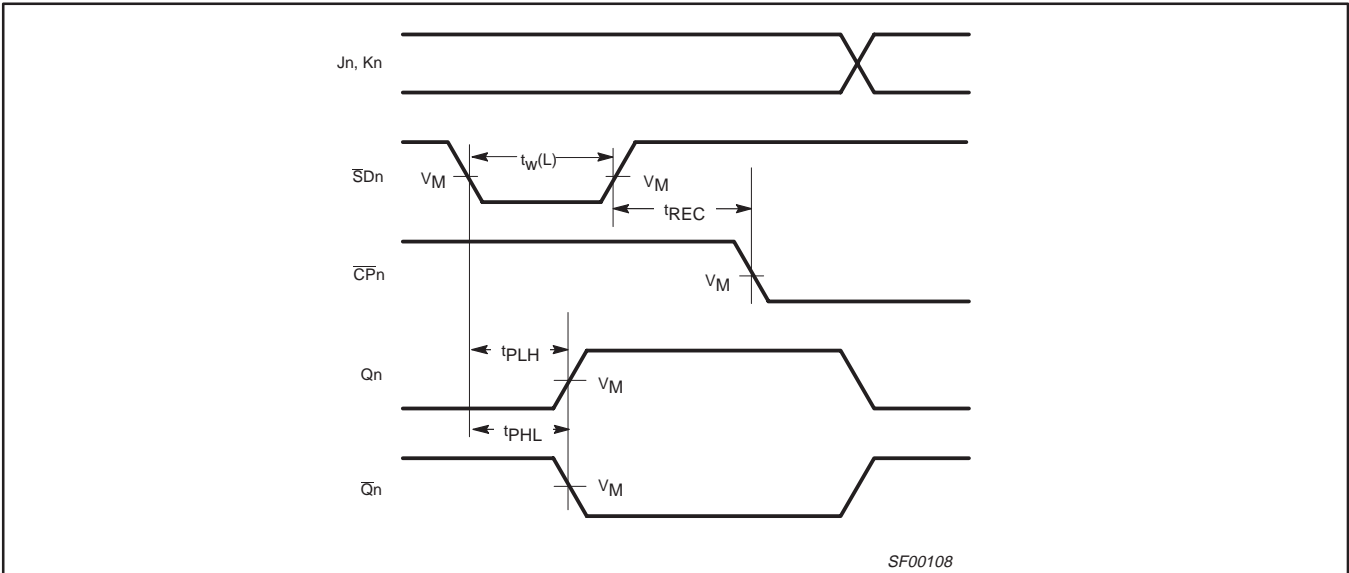


The shaded areas indicate when the input is permitted to change for predictable output performance.

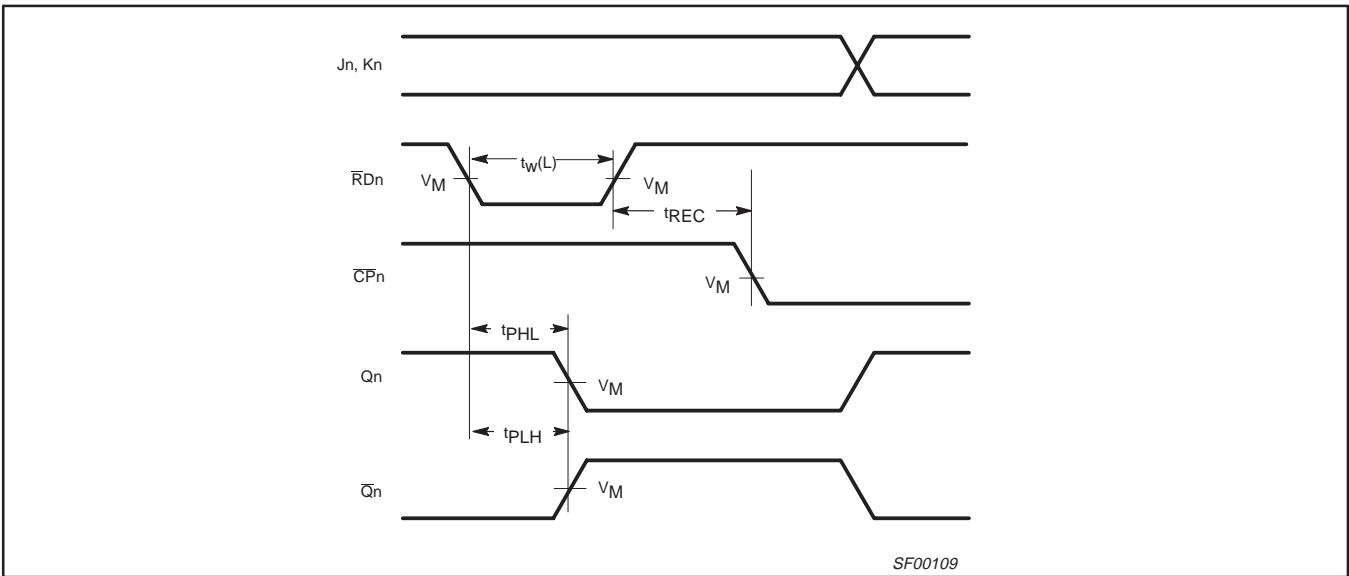
Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, and Clock Pulse Width

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Waveform 2. Propagation Delay for Set to Output, Set Pulse Width, and Recovery Time for Set to Clock

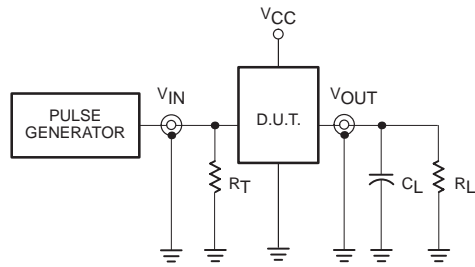


Waveform 3. Propagation Delay for Reset to Output, Reset Pulse Width, and Recovery Time for Reset to Clock

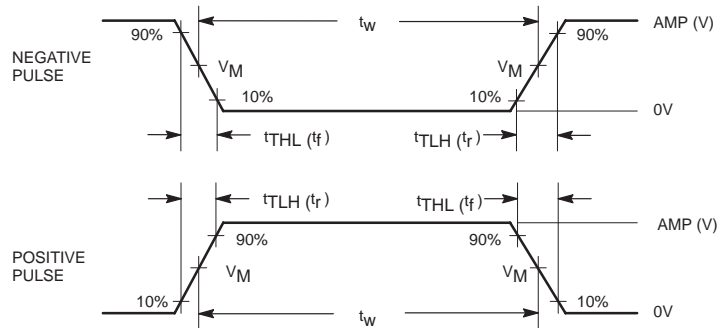
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TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

- R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

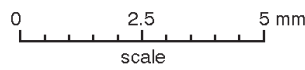
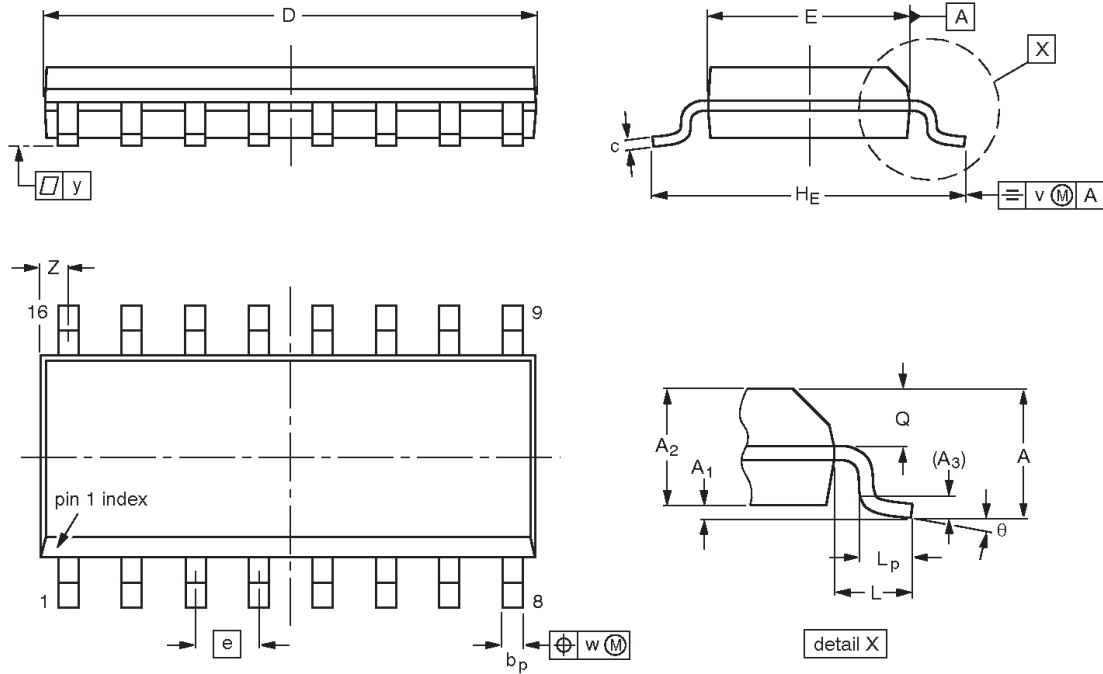
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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