

Phase-Locked Loop Clock Driver

Product Features

- High-Performance Phase-Locked-Loop Clock Distribution for Networking, ATM, 100/134 MHz Registered DIMM Synchronous DRAM modules for server/workstation/PC applications
- Zero Input-to-Output delay
- Low jitter: Cycle-to-Cycle jitter ± 100 ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Packaged in Plastic 8-pin SOIC Package (W) Pb-free and Green Available
- Wide range of Clock Frequencies

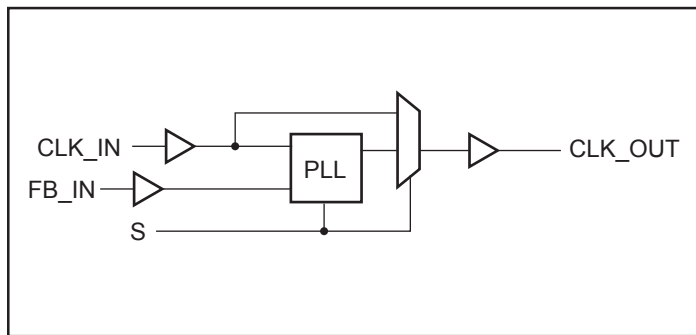
Product Description

The PI6C2401 features a low-skew, low-jitter, phase-locked loop (PLL) clock driver. By connecting the feedback CLK_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero.

Application

If the system designer needs more than 16 outputs with the features just described, using two or more zero-delay buffers such as PI6C2509Q, and PI6C2510Q, is likely to be impractical. The device-to-device skew introduced can significantly reduce the performance. Pericom recommends the use of a zero-delay buffer and an eighteen output non-zero-delay buffer. As shown in Figure 1, this combination produces a zero-delay buffer with all the signal characteristics of the original zero-delay buffer, but with as many outputs as the non-zero-delay buffer part. For example, when combined with an eighteen output non-zero delay buffer, a system designer can create a seventeen-output zero-delay buffer.

Logic Block Diagram



Product Pin Configuration

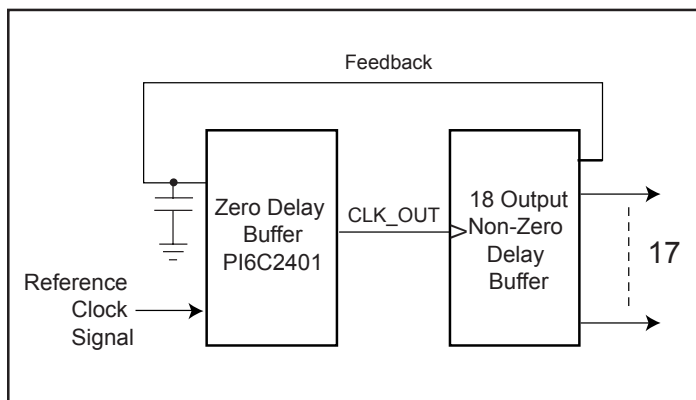
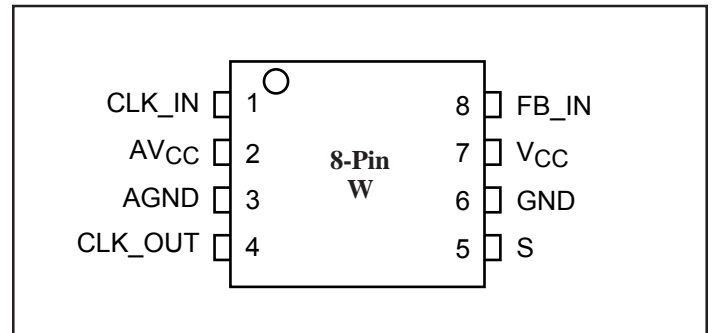


Figure 1. This Combination Provides Zero-Delay Between the Reference Clocks Signal and 17 Outputs

Control Input

S	Output Source	PLL Shutdown
1	PLL	N
0	CLK_IN	Y

Pin Functions

Pin Name	Pin Number	Type	Description
CLK_IN	1	I	Reference Clock input. CLK_IN allows spread spectrum clock input.
AVCC	2	Power	Analog power supply.
AGND	3	Ground	Analog ground.
CLK_OUT	4	O	Clock outputs. The output provides low-skew copies of CLK_IN and has an embedded series-damping resistor.
S	5	I	Control Input S. S is used to bypass the PLL for test purposes. When S is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs.
GND	6	Ground	Ground.
VCC	7	Power	Power supply.
FB_IN	8	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.

DC Specifications (Absolute maximum ratings over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V _I	Input voltage range	-0.5	V _{CC} + 0.5	V
V _O	Output voltage range			
V _{I_DC}	DC input voltage		+5.0	
IO_DC	DC output current		100	mA
Power	Maximum power dissipation at T _A = 55°C in still air		1.0	W
T _{STG}	Storage temperature	-65	150	°C

Note: Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

Parameter	Test Conditions	VCC	Min.	Typ.	Max.	Units
I _{CC}	V _I = V _{CC} or GND; I _O = 0 ⁽¹⁾	3.6V			10	μA
C _I	V _I = V _{CC} or GND	3.3V		4		pF
C _O	V _O = V _{CC} or GND			6		

Note:

1. Continuous output current

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V _{CC}	Supply voltage	3.0	3.6	V
V _{IH}	High level input voltage	2.0		
V _{IL}	Low level input voltage		0.8	
V _I	Input voltage	0	V _{CC}	
T _A	Operating free-air temperature	0	70	°C

Electrical Characteristics

 (Over recommended operating free-air temperature range Pull Up/Down Currents, V_{CC} = 3.0V)

Symbol	Parameter	Condition	Min.	Max.	Units
I _{OH}	Pull-up current	V _{OUT} = 2.4V		-12	mA
		V _{OUT} = 2.0V		-18	
I _{OL}	Pull-down current	V _{OUT} = 0.8V	18		
		V _{OUT} = 0.55V	12		

AC Specifications Timing Requirements

(Over recommended ranges of supply voltage and operating free-air temperature)

Symbol	Parameter	Min.	Max.	Units
F _{CLOCK}	Clock frequency	25	134	MHz
D _{CYI}	Input clock duty cycle	40	60	%
	Stabilization Time after power up		1	ms

Switching Characteristics

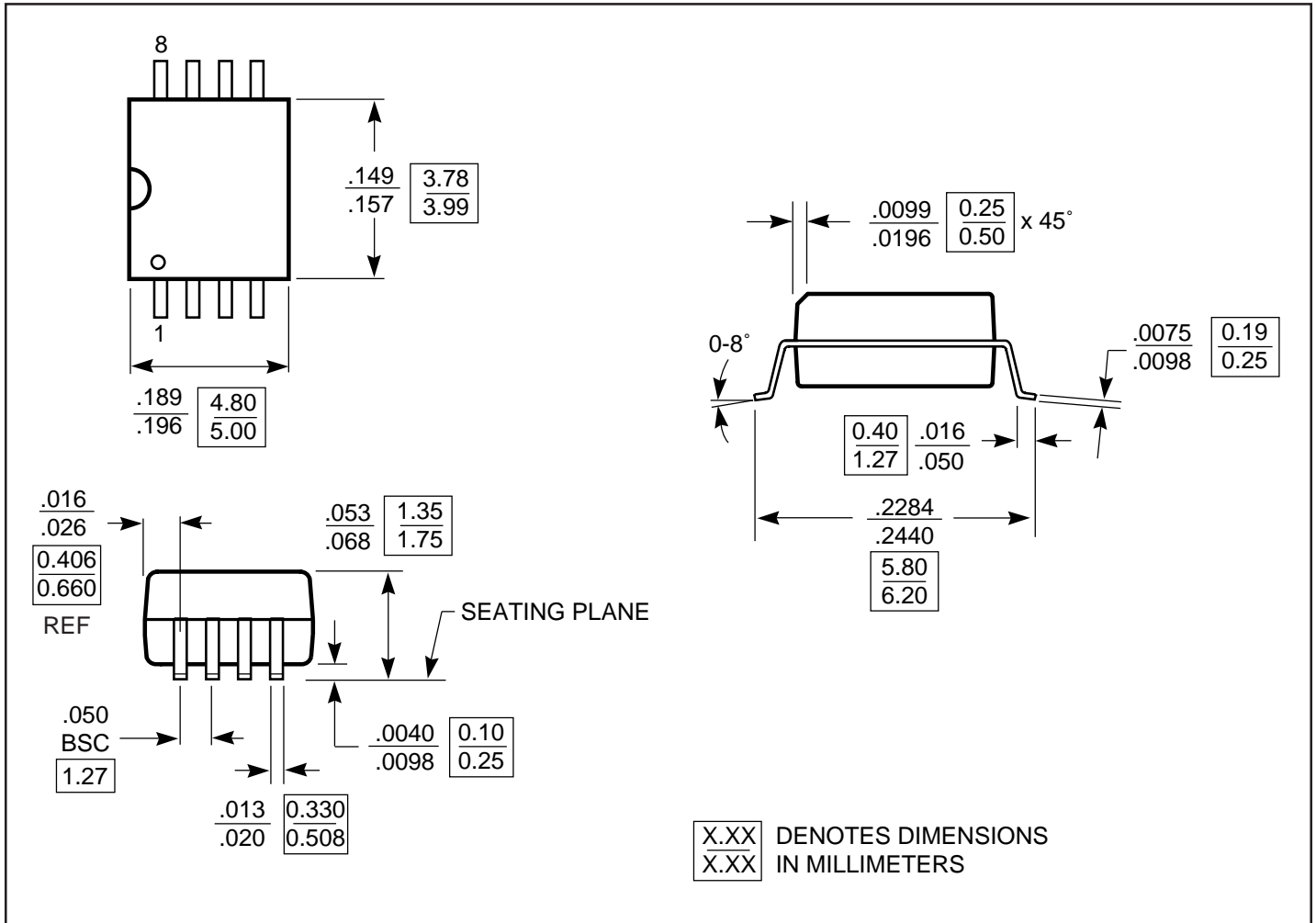
 (Over recommended ranges of supply voltage and operating free-air temperature, C_L=30pF)

Parameter	From	To	V _{CC} = 3.3V ± 0.3V, 0-70 °C			Units
			Min.	Typ.	Max.	
t _{phase error without jitter}	CLK_IN ↑ at 100 MHz and 66 MHz	FB_IN ↑			+175	ps
Jitter, cycle-to-cycle	At 100 MHz and 66 MHz	CLK_OUT	-150		+150	
Duty cycle			35		65	%
t _r , rise-time, 0.4V to 2.0V		CLK_OUT		1.0		ns
t _f , fall-time, 2.0V to 0.4V				1.1		

Note: These switching parameters are guaranteed by design.

Package Mechanical Information

Plastic 8-pin SOIC Package



Ordering Information

Ordering Code	Package Code	Package Type	Operating Range
PI6C2401W	W	8-pin 150-mil SOIC	Commercial
PI6C2401WE	W	Pb-free and Green 8-pin 150-mil SOIC	Commercial