MN89303A

SVGA Display Controller

■ Overview

The MN89303A is an LCD/CRT display controller with IBM™ VGA-compatible registers. It features all the necessary interfaces for a compact display system: ISA bus interface, local bus interface, DRAM interface, and LCD panel interface. The built-in graphics acceleration functions include support for hardware cursor.

Note: IBM™ and VGA are registered trademarks of International Business Machines Corporation.

■ Features

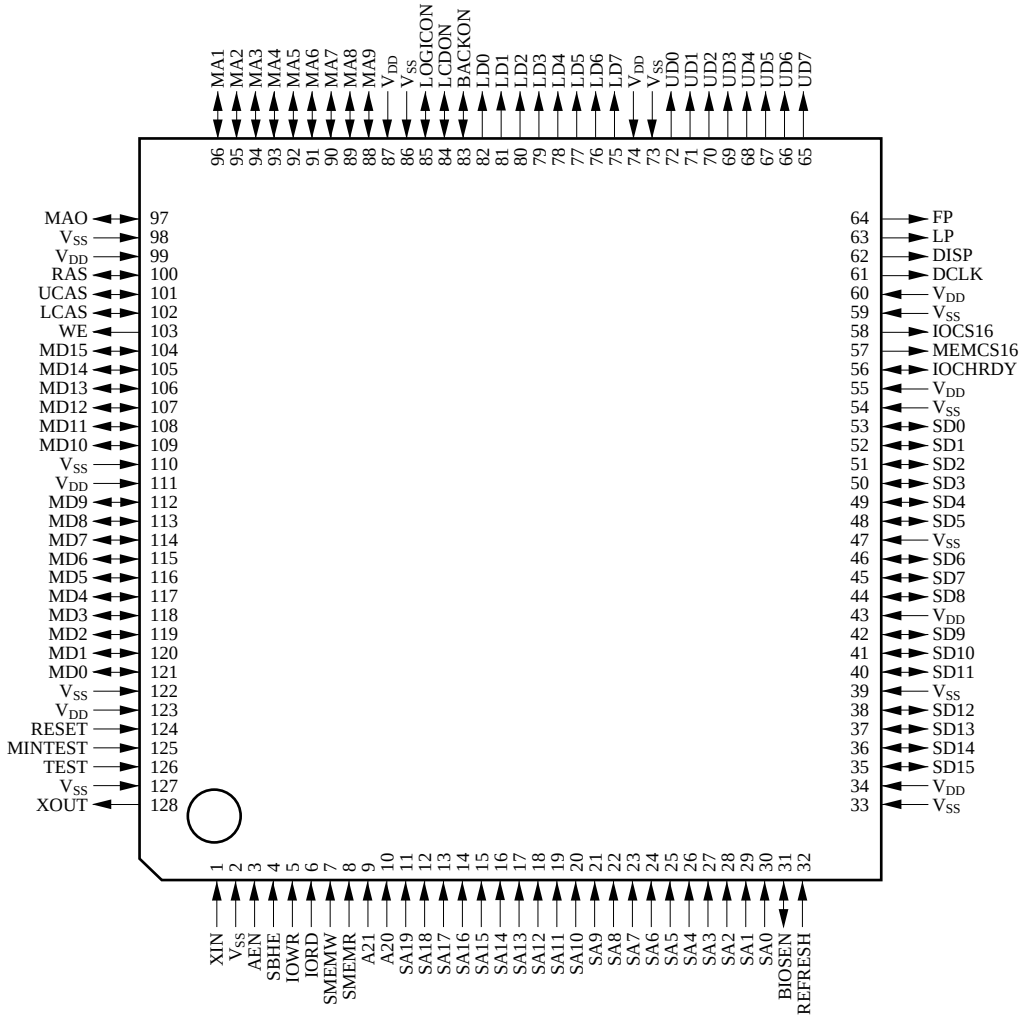
- Monochrome STN LCD panel support
  - Maximum display size: 800 × 600
  - Support for single and dual panels
  - 16-monochrome gradation
- Color STN LCD panel support
  - Maximum display size: 800 × 600
  - Support for single and dual panels
  - 16-gradation for each color (RGB)
- Color TFT LCD panel support
  - Maximum display size: 800 × 600
  - 4-bit output for each color (RGB)
- Maximum number of colors in concurrent display
  - 640 × 480: 256/4096 palette (TFT, STN)
  - 800 × 600: 256/4096 palette (TFT, STN)
- Built-in graphics acceleration functions
  - Hardware cursor (16 × 16 or 32 × 32)
- Built-in automatic display centering
- Built-in gradation control table (rewritable) for optimizing gradation to match panel
- DRAM interface with 16-bit bus
  - Choice of DRAM access timing to match system performance (EDO/normal)
  - Support for 2CAS/2WE mode
  - Refresh control
- Host interfaces
  - ISA bus (16-bit)
  - i386/i486 local bus (16-bit)

Note: i386 and i486 are trademarks of Intel Corporation.

■ Applications

- Point-of-sale terminals, Factory automation terminals, word processors, and other terminals

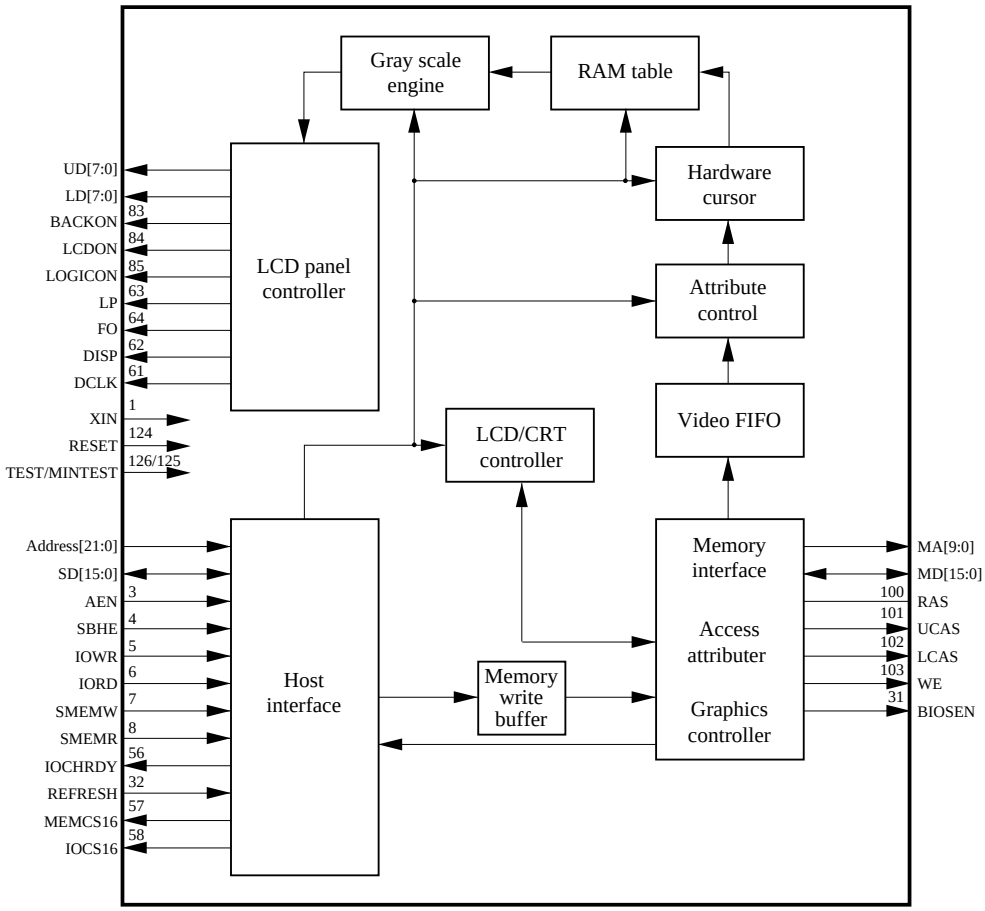
■ Pin Assignment



(TOP VIEW)
QFH128-P-1818

Note: Never leave V_{DD} and V_{SS} pins open.

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	I/O	Level	Function Description
3	AEN	I	TTL	Address Enable "H" level input from this pin indicates that a DMA transfer is in progress, so the chip does not respond to I/O access.
4	SBHE	I	TTL	Byte High Enable This input indicates the state of the 16-bit bus.
5	IOWR	I	TTL	I/O Write This input indicates an I/O write request.
6	IORD	I	TTL	I/O Read This input indicates an I/O read request.
7	SMEMW	I	TTL	Memory Write This input indicates a memory write request dedicated for an address space in the first megabyte (000000 to 0FFFFFH).
8	SMEMR	I	TTL	Memory Read This input indicates a memory read request dedicated for an address space in the first megabyte (000000 to 0FFFFFH).
9 to 10	A[21:20]	I	TTL	Address[21:20] These inputs give the address 21:20.
11 to 30	SA[19:0]	I	TTL	Address[19:0] These inputs give the address 19:0.
35 to 53	SD[15:0]	I/O	TTL	Data[15:0] These pins represent the host data bus.
56	IOCHRDY	I/O	TTL	I/O Channel Ready This pin is "L" level when I/O or memory access is given wait state.
57	MEMCS16	O	TTL	Memory Chip Select 16 This output indicates to the system that 16-bit memory access is available.
58	IOCS16	O	TTL	I/O Chip Select 16 This output indicates to the system that 16-bit I/O access is available.
32	REFRESH	I	TTL	Refresh "L" level input indicates that the system is refreshing its DRAM.
88 to 97	MA[9:0]	O	CMOS	Memory Address These outputs give the address of the display memory.
100	RAS	O	CMOS	Row Address Strobe (RAS) This output is the strobe signal for the row address latch.
101	UCAS	O	CMOS	Upper Column Address Strobe (UCAS) This output is the strobe signal for the upper column address latch. In the 2WE mode, however, it functions as the CAS signal.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Level	Function Description
102	LCAS	O	CMOS	Lower Column Address Strobe (LCAS) This output is the strobe signal for the lower column address latch. In the 2WE mode, however, it functions as the LWE signal.
103	WE	O	CMOS	Write Enable This output is the data write signal. In the 2WE mode, however, it functions as the UWE signal.
104 to 121	MD[15:0]	I/O	TTL	Memory Data These pins represent the data bus to the DRAM.
31	BIOSEN	O	CMOS	BIOS Enable This output enables ROM BIOS output.
83	BACKON	O	CMOS	Backlight ON This output requests backlighting. "L" level: OFF; "H" level: ON
84	LCDON	O	CMOS	LCD Drive ON This output requests power-ON for the LCD panel. "L" level: OFF; "H" level: ON
85	LOGICON	O	CMOS	LCD Logic ON This output requests power-ON for LCD panel logic circuits. "L" level: OFF; "H" level: ON
63	LP	O	CMOS	Line Pulse This output provides pulses indicating the end of a line of the LCD panel.
64	FP	O	CMOS	Frame Pulse This output provides pulses indicating the start of a frame of the LCD panel.
62	DISP	O	CMOS	Display Enable This output enables the LCD display. An external RAMDAC uses this signal as a blanking signal. A TFT LCD uses it as an enable signal.
61	DCLK	O	CMOS	Data Shift Clock This pin provides a data shift clock signal for an STN LCD panel. It also outputs a dot clock signal on a TFT LCD panel or external RAMDAC display mode.
65 to 72	UD[7:0]	O	CMOS	Upper Data[7:0]
75 to 82	LD[7:0]	O	CMOS	Lower Data[7:0] This pins provide display data. Usage varies with the LCD panel type.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Level	Function Description
124	RESET	I	TTL	Reset "H" level input from this pin initializes the chip. If the host is in a i386 mode, the chip aligns the clock phase with this signal.
96 to 97	MA[1:0]	I	CMOS	Host Type During a reset, these pins select the host type. MA[1:0] Host Type 0 0 ISA 0 1 386SX 1 0 386DX 1 1 486
126/125	TEST/ MINTEST		CMOS	Chip Test Condition This pin selects the chip test mode.
1/128	XIN/ XOUT	I/O		Clock IN/OUT These pins are the clock I/O pins. Connect them to a crystal oscillator.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	– 0.3 to +7.0	V
Input pin voltage	V_I	– 0.3 to V_{DD}+0.3	V
Output pin voltage	V_O	– 0.3 to V_{DD}+0.3	V
Power dissipaiton	P_D	1000	mW
Operating ambient temperature	T_{opr}	0 to +70	˚C
Storage temperature	T_{stg}	– 55 to +150	˚C

■ Recommended Operating Conditions

Parameter	Symbol	Conditions	min	typ	max	Unit
Power supply voltage	V_{DD}		4.75	5.00	5.25	V
Ambient temperature	Ta		0		70	˚C
Rise time for input	t_r		0		150	ns
Fall time for input	t_f		0		150	ns
Oscillation frequency	f_{OSC}	At self-excited operation	25		33	MHz
Operating frequency	f_{opr1}	At self-excited operation	25		33	MHz
Operating frequency	f_{opr2}	Using external input	0		33	MHz

■ Electrical Characteristics

V_{DD}=4.75 to 5.25V, V_{SS}=0.00V, f=33MHz, Ta=0 to 70˚C

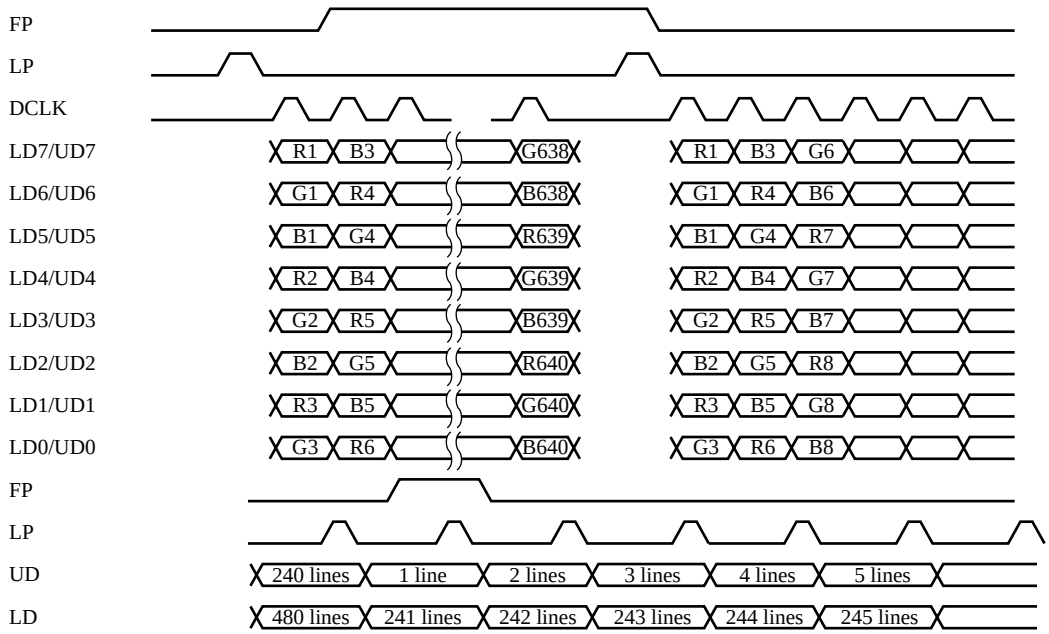
Parameter	Symbol	Conditions	min	typ	max	Unit
Power supply current during operation	I_{DD0}	V_I=V_{DD} or V_{SS} ,V_{DD}=5.0V			120	mA
Power supply current in the SUSPEND mode	I_{DD1}	V_I=V_{DD} or V_{SS} ,V_{DD}=5.0V			15	mA
Power supply current in the STANDBY mode	I_{DD2}	V_I=V_{DD} or V_{SS} ,V_{DD}=5.0V			40	mA
"H" level input voltage 1 TEST ,AEN ,SBHE , IOWR ,IORD ,SMEMW , SMEMR ,REFRESH , A21 to 20 ,SA19 to 0 , SD15 to 0 ,MD15 to 0 , BIOSEN ,IOCHRDY	V_{IH1}		2.0		V_{DD}	V
"H" level input voltage 2 MINTEST ,RAS ,UCAS , LCAS ,BACKON , LCDON ,LOGICON , MA9 to 0	V_{IH2}		V_{DD} × 0.7		V_{DD}	V
"L" level input voltage 1 TEST ,AEN ,SBHE , IOWR ,IORD ,SMEMW , SMEMR ,REFRESH , A21 to 20 ,SA19 to 0 , SD15 to 0 ,MD15 to 0 , BIOSEN ,IOCHRDY	V_{IL1}		0		0.8	V
"L" level input voltage 2 MINTESTRAS UCAS , LCAS ,BACKON , LCDON ,LOGICON , MA9 to 0	V_{IL2}		0		V_{DD} × 0.3	V
Input leakage current 1 TEST ,MINTEST	I_{LI1}	V_I=V_{DD} or V_{SS}			±20	µA
Input leakage current 2 AEN ,SBHE ,IOWR , IORD ,SMEMW , SMEMR ,REFRESH , A21 to 20 ,SA19 to 0 , RESET	I_{LI2}	V_I=V_{DD} or V_{SS}			±10	µA
Pull-down resistance	R_{PD1}	V_I=V_{DD} ,V_{DD}=5.0V	12	30	75	kΩ
Input threshold voltage RESET	V_{tHL} V_{tLH}	V_{DD}=4.75 to 5.25V		1.0 1.8		V

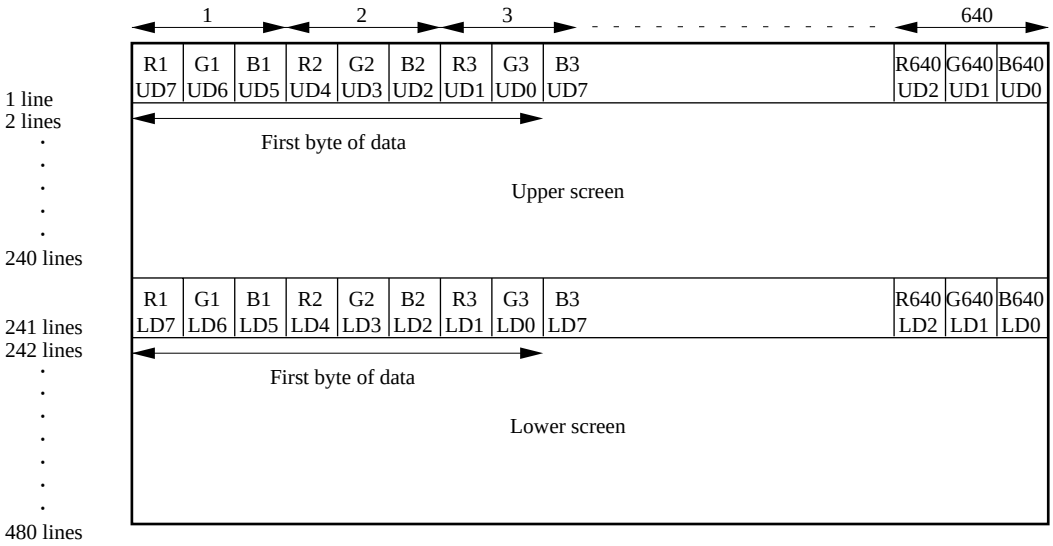
■ Electrical Characteristics (continued)

V_{DD}=4.75 to 5.25V, V_{SS}=0.00V, f=33MHz, Ta=0 to 70˚C

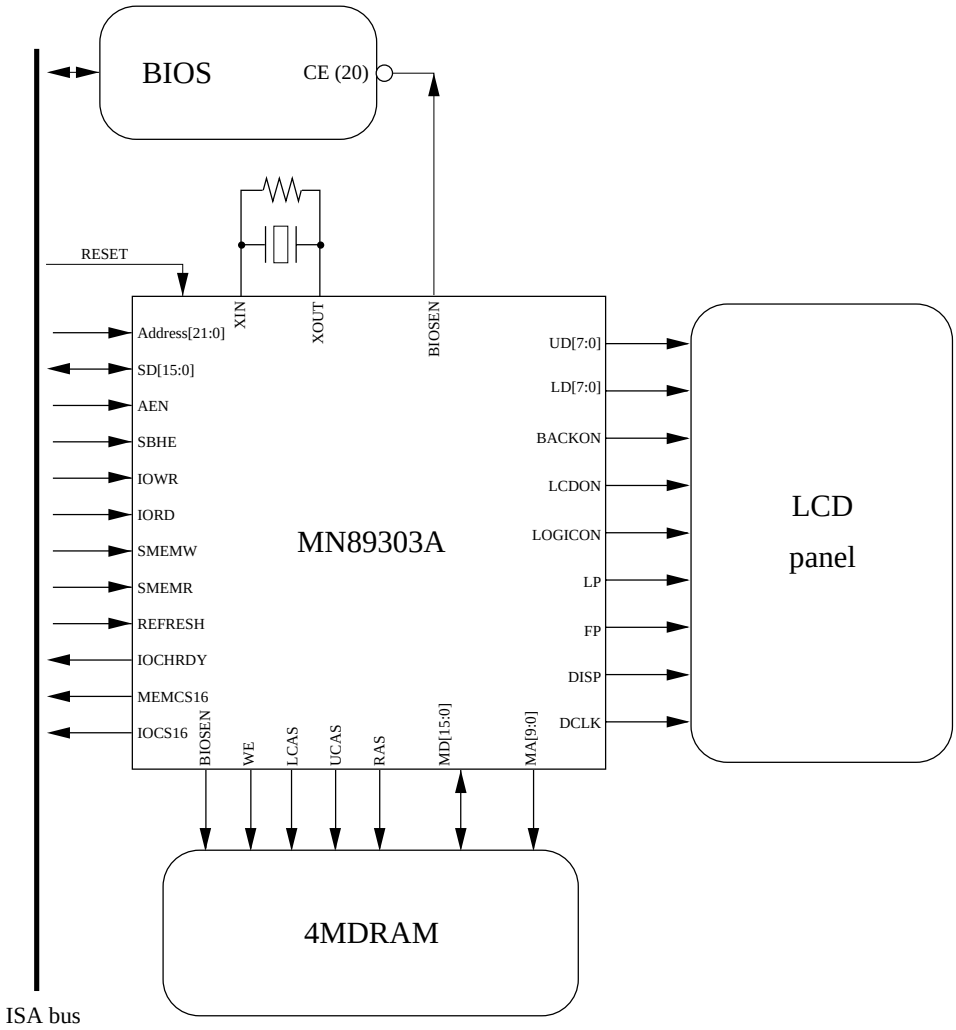
Parameter	Symbol	Conditions	min	typ	max	Unit
"H" level output voltage 1 BACKON ,LCDON , LOGICON ,SD15 to 0 , MD15 to 0 ,BIOSEN	V_{OH1}	I_O=–2.0mA V_I=V_{DD} or V_{SS}	V_{DD}– 0.6			V
"H" level output voltage 2 DCLK ,DISP ,LP ,FP , UD7 to 0 ,LD7 to 0 , WE ,MA9 to 0 ,RAS , UCAS ,LCAS	V_{OH2}	I_O=–8.0mA V_I=V_{DD} or V_{SS}	V_{DD}– 0.6			V
"H" level output voltage 3 IOCHRDY	V_{OH3}	I_O=–12.0mA V_I=V_{DD} or V_{SS}	V_{DD}– 0.6			V
"H" level output voltage 4 IOCS16 ,MEMCS16	V_{OH4}	I_O=–16.0mA V_I=V_{DD} or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage 1 BACKON ,LCDON , LOGICON	V_{OL1}	I_O=2.0mA V_I=V_{DD} or V_{SS}			0.4	V
"L" level output voltage 2 SD15 to 0 ,MD15 to 0 , BIOSEN	V_{OL2}	I_O=4.0mA V_I=V_{DD} or V_{SS}			0.4	V
"L" level output voltage 3 DCLK ,DISP ,LP ,FP , UD7 to 0 ,LD7 to 0 , WE ,MA9 to 0 ,RAS , UCAS ,LCAS	V_{OL3}	I_O=0.8mA V_I=V_{DD} or V_{SS}			0.4	V
"L" level output voltage 4 IOCHRDY	V_{OL4}	I_O=12.0mA V_I=V_{DD} or V_{SS}			0.4	V
"L" level output voltage 5 IOCS16 ,MEMCS16	V_{OL5}	I_O=16.0mA V_I=V_{DD} or V_{SS}			0.4	V
Output leakage current IOCS16 ,BACKON , MA9 to 0 ,MEMCS16 , UCAS ,LCAS ,RAS , LOGICON ,LCDON , SD15 to 0 ,MD15 to 0 , BIOSEN ,IOCHRDY	I_{LO}	V_O=High-impedance state V_I=V_{DD} or V_{SS} V_O=V_{DD} or V_{SS}			±10	µA

■ Timing Chart for LCD Panel Outputs





■ Application Circuit Example



■ Package Dimensions (Unit: mm)

QFH128-P-1818