MN85571AC

Single-Chip Audio/Video MPEG2 Encoder

■ Overview

The MN85571AC is an audio/video encoder that performs video compression in conformance with the ISO/IEC 13818-2 (MPEG2 video) and ISO/IEC 11172-2 (MPEG1 video) standards and audio compression in conformance with the Dolby Digital* system. It also can multiplex the compressed audio and video signals.

Note) 1. *: Dolby Digital is a registered trademark of Dolby Laboratories.
Neither the supply of this product that implements Dolby technologies nor the use of this product in end user products or other end products implies the recognition of any implicit rights or licenses based on patents or other intellectual property belonging to Dolby Laboratories. Licenses to use this product must be acquired from Dolby Laboratories.

2. Use of this product in MPEG2-related products requires patent licenses from the following company.
MPEG LA, LLC 250 Steel Street, Denver, Colorado USA 80206

■ Features

- Video encoding
  - Image compression technique: Compression in conformance with the ISO/IEC 13818-2 (MPEG2 video) and ISO/IEC 11172-2 (MPEG1 video) standards
  - Generation of image sizes for the DVD video recording standards from ITU-R BT.656 (D1 parallel input) conforming signals
  - Functions for conversion of horizontal and vertical resolutions.
  - Special quantization processing and filtering (time, horizontal, and vertical axes)
- Audio encoding
  - Encoding techniques: Dolby Digital and linear PCM
  - Sampling frequency: 48 kHz
  - Number of channels: 2 channels (left and right)
  - Digital input interface: One system (supports both master and slave mode operation)
- External components
  - External host for initialization and user-specific settings, and buffer memories (One 32-bit 64M SDRAM or two 16)
  - Power supply system: Two supply voltages: 3.3 V (I/O supply voltage and internal PLL circuit supply voltage), 1.8 V (internal circuit supply voltage)

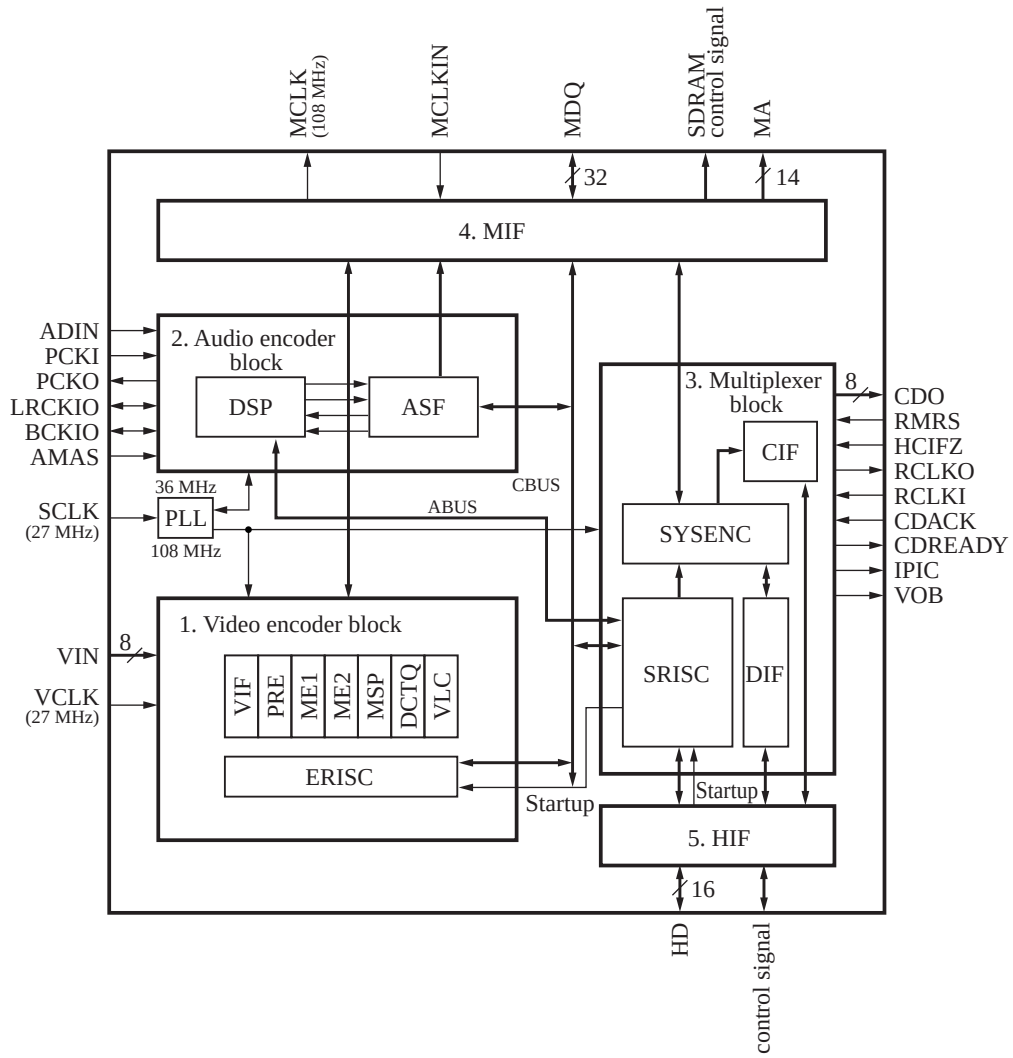
■ Applications

- Used in the encoder block in AV recording equipment that uses the MPEG2 technique, such as DVD recorders.

■ Block Diagram

The MN85571AC consists of the 5 blocks listed below.

1. Video encoder block. This block is based on the MN85560 MPEG2 video encoder, but provides additional functionality as well.
2. Audio encoder block. This block is based on the MN67735JA Dolby Digital encoder core.
3. Multiplexer block. This block multiplexes the encoded video and audio data.
4. SDRAM interface block (MIF). This block handles data exchange with external SDRAM.
5. Host interface block (HIF). This block handles data exchange with and accepts control commands from an external host.



Note) The MN85571AC includes two RISC microcontrollers (for video encoding and data multiplexing) and one DSP for audio encoding. The microcode for these two RISC microcontrollers must be downloaded to the on-chip instruction memory before the MN85571AC is used. The DSP microcode is stored in on-chip ROM, and does not need to be downloaded.

■ Internal Resource Mapping

The MN85571AC has two types of internal resources that are accessed by the external host with different methods.

1) Direct addressing resources (registers only)

These resources are mainly used for controlling this device and indicating the internal state of the device. These are 16-bit registers.

2) Indirect addressing resources (registers and memory)

These are memory and other resources that mainly consist of parameter setting registers used at initialization and memory that holds microcode.

1. Direct addressing resources

These are accessed by specifying the address to the external pins HA[3:0].
Table 1 shows the address mapping for the direct addressing resources.

Table 1. Direct Addressing Register Mapping

HA[3 : 0]	Register	r/w	Function
%0000	CHIPCTL0	r/w	Control signal register 0 (reset, mode, srisc en)
%0001	Reserved		
%0010	CHIPST0	r	Status register 0 (interrupt)
%0011	CHIPST1	r	Status register 1 (mode, busy)
%0100	STMSK	r/w	Status report signal mask register
%0101	Reserved		
%0110	INADR0	r/w	Indirect access address register
%0111	Reserved		
%1000	INDAT0	r/w	Indirect access data register
%1001	Reserved		
%1010	DIFACC	r/w	DIF access register
%1011	DIFPTR	r/w	DIF access address register
%1100	DIFDAT	r/w	DIF access data register
%1101	Reserved		
%1110	DMAACC	r	DMA access register
%1111	Reserved		

Note) 1. CHIPCTL0 is only reset by a hardware reset (setting the external pin NRST low).
2. Chip operation is not guaranteed after access to any of the reserved direct addressing registers.
3. The symbols r and w indicate read and write as seen from the external host.
The symbol r alone indicates a read-only register, and r/w indicates the both read and write are possible.
4. Accesses to registers other than CHIPCTL0 are invalid in the reset state (software reset).
All register accesses are invalid in the hardware reset state.
5. The CHIPCTL0, CHIPST0, CHIPST1, STMASK, INADR0, and DIFPTR registers can all be read in the hold, slave, and run states.

■ Internal Resource Mapping (continued)

2. Indirect addressing resources (registers and initial load memory)

These internal resources are accessed by storing the address of the indirect addressing resource in the INADR0 indirect access address register and reading or writing the INDAT0 indirect access data register. Other than the registers used for communication with the external host and the SRISC, these resources can only be accessed in the slave state. While these resources have a structure that consists of 16 bits per address, indirect addressing access writes must be performed in 32-bit units. Tables 2 and 3 show the address maps.

Table 2. Indirect Addressing Resources Address Map Overview

indir adr *1	Description
$0000 – $01FF	Communication registers, parameter registers, and other registers
$0200 – $03FF	Video input intensity conversion data memory (ITDM) A: 256 words × 8 bits *2
$0400 – $05FF	Video input intensity conversion data memory (ITDM) A: 256 words × 8 bits *2
$0600 – $0FFF	Reserved
$1000 – $17FF	Video encoding block RISC data memory (VDM): 1K words × 16 bits *2
$1800 – $3FFF	Reserved
$4000 – $7FFF	Video encoding block RISC instruction memory (VIRAM): 8K words × 32 bits
$8000 – $8FFF	Reserved
$9000 – $9FFF	Multiplexing block RISC data memory (SDM): 2K words × 16 bits *2
$A000 – $CFFF	Multiplexing block RISC instruction memory (SIRAM): 6K words × 24 bits 24 bits
$D000 – $FFFF	Reserved

Note) *1: The notation indir adr indicates the value stored in the INADR0 indirect access address register when accessing an indirect addressing resource.

*2: Data only exists at even addresses.

Table 3. Indirect Addressing Resources (Registers) Address Map

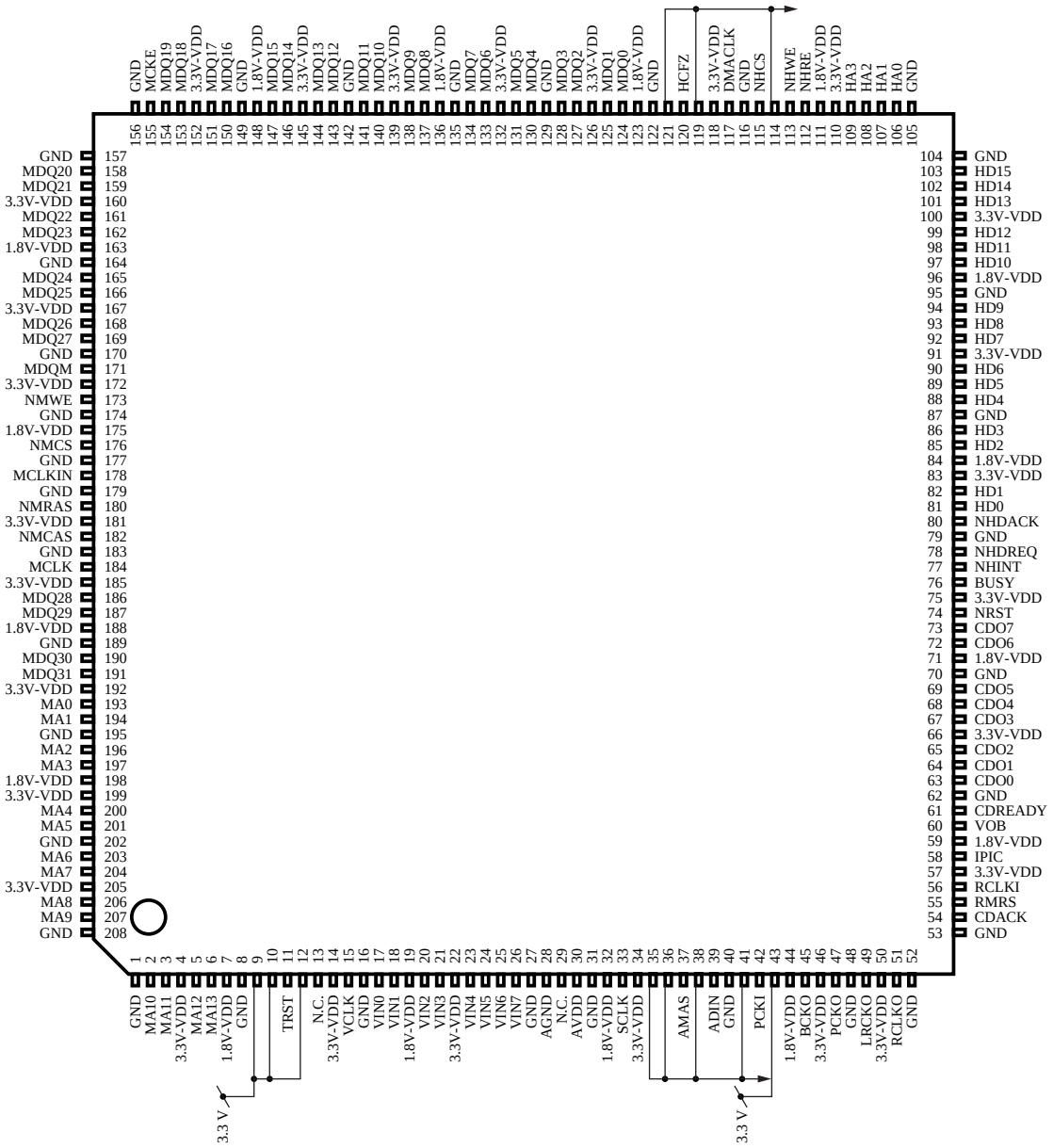
indir adr *	Description	Name	Run/Hold	Slave
$0000 – $000F	External host/SRIC communication register	hifreg	●	×
$0010 – $0013	Reserved		×	×
$0014	Video input block parameter register	vifreg	×	W
$0015 – $001F	Reserved		×	×
$0020	DMA data I/O block parameter register	difreg	×	W
$0021	Reserved		×	×
$0022 – $0025	Code output block parameter register	cifreg	×	W
$0026 – $01FF	Reserved		×	×

Note) 1. *: The notation indir adr indicates the value stored in the INADR0 indirect access address register when accessing an indirect addressing resource.

2. ●: Both read and write access allowed. W: Write access allowed (Cannot be read.) ×: No access is allowed. Chip operation is not guaranteed if registers for which access is only allowed in the slave state are accessed in either the run or hold states.

Chip operation is not guaranteed if areas indicated as reserved are accessed.

■ Pin Arrangement



(TOPVIEW)

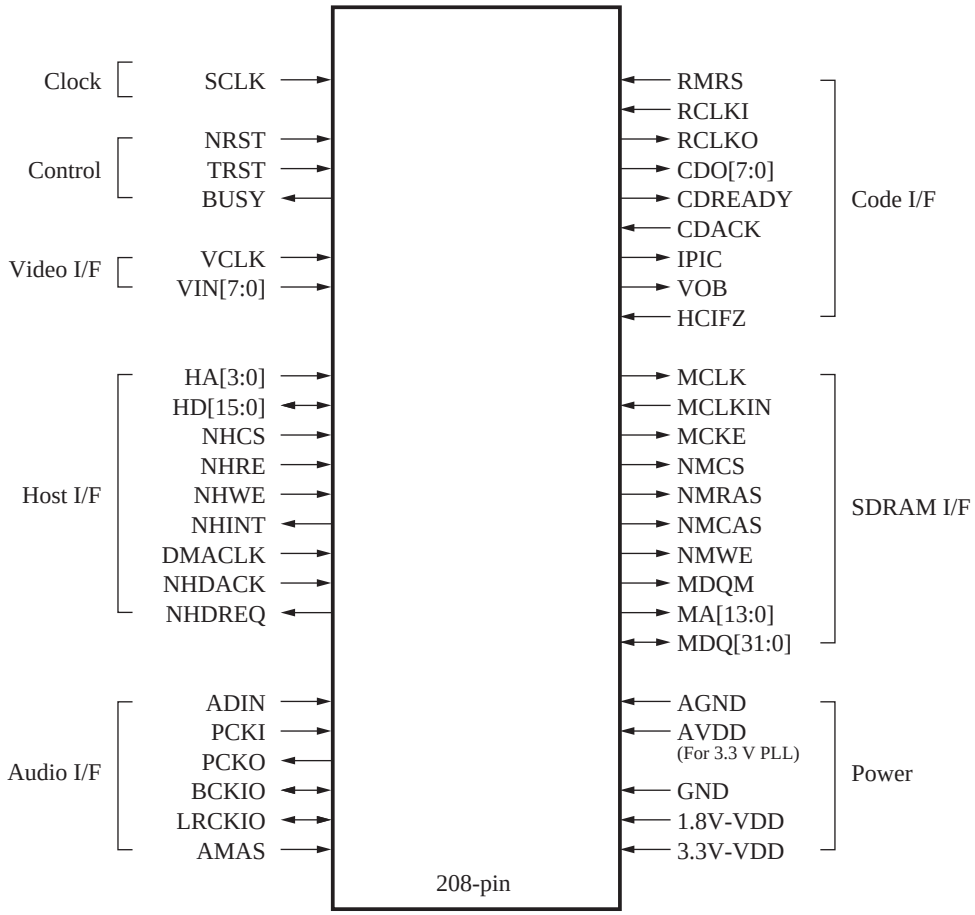
Note) The same signal must be input to both the NRST and TRST pins.

■ Signal and Control Timing

• Signal Overview

The MN85571AC I/O signals can be classified by function as shown below.
See the Pin Descriptions section for details on these signals.

All signal pins conform to the LVTTL standard.



■ Pin Descriptions

Type	Pin Name	I/O	Description
Clock	SCLK	I	System clock input
Control	NRST	I	Chip initialization reset input signal 1
Control	TRST	I	Chip initialization reset input signal 2
Control	BUSY	O	Chip status output signal
Video I/F	VCLK	I	Video data input clock
Video I/F	VIN[7:0]	I	Video data input signal
Host I/F	HA[3:0]	I	Host interface address signal
Host I/F	HD[15:0]	I/O	Host interface data I/O
Host I/F	NHCS	I	Host interface chip select signal
Host I/F	NHRE	I	Host interface read enable signal
Host I/F	NHWE	I	Host interface write enable signal
Host I/F	NHINT	O	Host interface interrupt occurrence report signal
Host I/F	DMACLK	I	DMA I/O block 1 bus mode clock input
Host I/F	NHDACK	I	Code output enable signal (DMA mode)
Host I/F	NHDREQ	O	DMA transfer request signal
Audio I/F	ADIN	I	PCM data input (audio data input)
Audio I/F	PCKI	I	PCM master clock input
Audio I/F	PCKO	O	PCM master clock output
Audio I/F	BCKIO	I/O	Bit clock (64 fs or 32 fs) I/O (pulled up)
Audio I/F	LRCKIO	I/O	Left/right channel discrimination clock (fs) I/O (pulled up)
Audio I/F	AMAS	I	Master mode/slave mode switching control
Code I/F	RMRS	I	RCLK clock I/O switching
Code I/F	RCLKI	I	Code output clock input (Used in RSLAVE mode, pulled up.)
Code I/F	RCLKO	O	Code output clock output (Used in RMASTER mode.)
Code I/F	CDO[7:0]	O	Serial code output signal
Code I/F	CDREADY	O	Serial code output ready signal
Code I/F	CDACK	I	Serial code output request signal
Code I/F	IPIC	O	Pack flag that includes the VOBU start I Picture
Code I/F	VOB	O	VOB start pack flag
Code I/F	HCIFZ	I	Code output pin initial state control
SDRAM I/F	MCLK	O	External memory (SDRAM) clock output
SDRAM I/F	MCLKIN	I	Clock input for data transfer between external memory and this product
SDRAM I/F	MCKE	O	External memory (SDRAM) CKE output
SDRAM I/F	NMCS	O	External memory (SDRAM) chip select output
SDRAM I/F	NMRAS	O	External memory (SDRAM) RAS output
SDRAM I/F	NMCAS	O	External memory (SDRAM) CAS output

■ Pin Descriptions (continued)

Type	Pin Name	I/O	Description
SDRAM I/F	NMWE	O	External memory (SDRAM) write enable output
SDRAM I/F	MDQM	O	External memory (SDRAM) data output buffer control
SDRAM I/F	MA[13:0]	O	External memory (SDRAM) address output
SDRAM I/F	MDQ[31:0]	I/O	External memory (SDRAM) data I/O (pulled up)
Power	AVDD	I	PLL system power supply (3.3 V)
Power	AGND	I	PLL system ground
Power	3.3V-VDD	I	3.3 V system power supply
Power	1.8V-VDD	I	1.8 V system power supply
Power	GND	I	Ground

■ Electrical Characteristics

1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage 1	3.3V-VDD	– 0.3 to +4.6	V
Supply voltage 2	1.8V-VDD	– 0.3 to +2.5	V
Supply voltage 3	AVDD	– 0.3 to +4.6	V
Input voltage	VI	– 0.3 to 3.3 V-VDD + 0.3 (Upper limit: 4.6)	V
Output voltage	VO	– 0.3 to 3.3 V-VDD + 0.3 (Upper limit: 4.6)	V
Average output current	IO	±24	mA
Power dissipation	PD	2.3 (4 layers)	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–40 to +125	°C

Note) 1. The absolute maximum ratings are limit values for stresses applied to the chip so that the chip will not be destroyed. Operation is not guaranteed within these ranges.

2. All of the 3.3 V VDD pins, 1.8 V VDD pins, and VSS pins must be connected externally to the 3.3 V power supply, 1.8 V power supply, and ground, respectively.

3. Connect bypass capacitors (at least 0.1 µF) between the 3.3 V VDD and VSS pins, between the 1.8 V VDD and VSS pins, and between the AVDD and VSS pins.

4. The power supply voltages must be applied in the following order: first apply the 3.3 V system level (3.3V-VDD, AVDD), and then apply the 1.8 V system level (1.8V-VDD).
When removing power from this IC, first remove the 1.8 V system level (1.8V-VDD) and then remove the 3.3 V system level (3.3V-VDD, AVDD).

2. Recommended Operating Conditions at VSS = 0 V, AVSS = 0 V

Item	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage 1	3.3V-VDD		3.0	3.3	3.6	V
Supply voltage 2	1.8V-VDD		1.65	1.80	1.95	V
Supply voltage 3	AVDD		3.0	3.3	3.6	V
Ambient temperature	T_a		0	—	70	°C
System clock frequency	SCLK	3.3V-VDD = 3.0 V to 3.6 V AVDD = 3.0 V to 3.6 V DUTY: 50%±10% Jitter: ±50 ppm *1	—	—	27.0	MHz
Video data input clock frequency	VCLK	3.3V-VDD = 3.0 V to 3.6 V DUTY: 50%±10% Jitter: ±50 ppm *1	—	—	27.0	MHz
Code data output clock frequency *2	RCLKI	3.3V-VDD = 3.0 V to 3.6 V DUTY: 50%±10%	—	—	33.0	MHz
DMA transfer clock frequency	DMACLK	3.3V-VDD = 3.0 V to 3.6 V DUTY: 50%±10%	—	—	33.0	MHz
PCM master clock frequency	PCKI	3.3V-VDD = 3.0 V to 3.6 V DUTY: 50%±10%	—	—	18.432	MHz

Note) ∗1: When TS output is used, the PCR counter SCLK and VCLK jitter must be held within ±30 ppm as stipulated by the ISO/IEC 13818-1 standard.

∗2: The value shown for RCLKI is the stipulated value for forward clock input standalone mode. The maximum value for reverse clock input standalone mode is 16 MHz.

■ Interfaces

1. Host interface

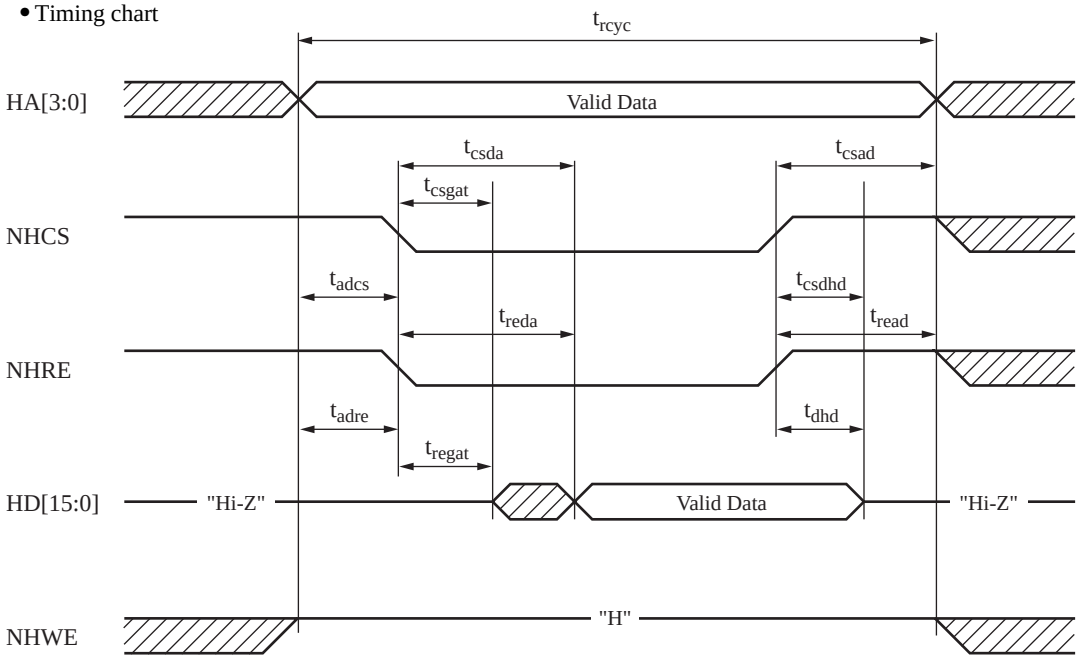
Accesses to this product's internal resources from an external host take place using the host interface block (HIF). There are two techniques for accessing resources over the host interface as follows.

1) Direct addressing access
2) Indirect addressing access

1) Direct addressing access

[Read]

• Timing chart



• AC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Read cycle time	t_{rcyc}	200	—	—	ns
HA[3:0] setup time from the NHCS falling edge	t_{adcs}	0	—	—	ns
HA[3:0] setup time from the NHRE falling edge	t_{adre}	0	—	—	ns
HD[15:0] bus drive start time from the NHCS falling edge	t_{csgat}	—	—	2	ns
HD[15:0] bus drive start time from the NHRE falling edge	t_{regat}	—	—	2	ns
HD[15:0] valid data output time from the NHCS falling edge	t_{csda}	—	—	135	ns
HD[15:0] valid data output time from the NHRE falling edge	t_{reda}	—	—	135	ns
HA[3:0] hold time from the NHCS rising edge	t_{csad}	40	—	—	ns
HA[3:0] hold time from the NHRE rising edge	t_{read}	40	—	—	ns
HD[15:0] valid data hold time from the NHCS rising edge	t_{csdhd}	2	—	—	ns
HD[15:0] valid data hold time from the NHRE rising edge	t_{dhd}	2	—	—	ns

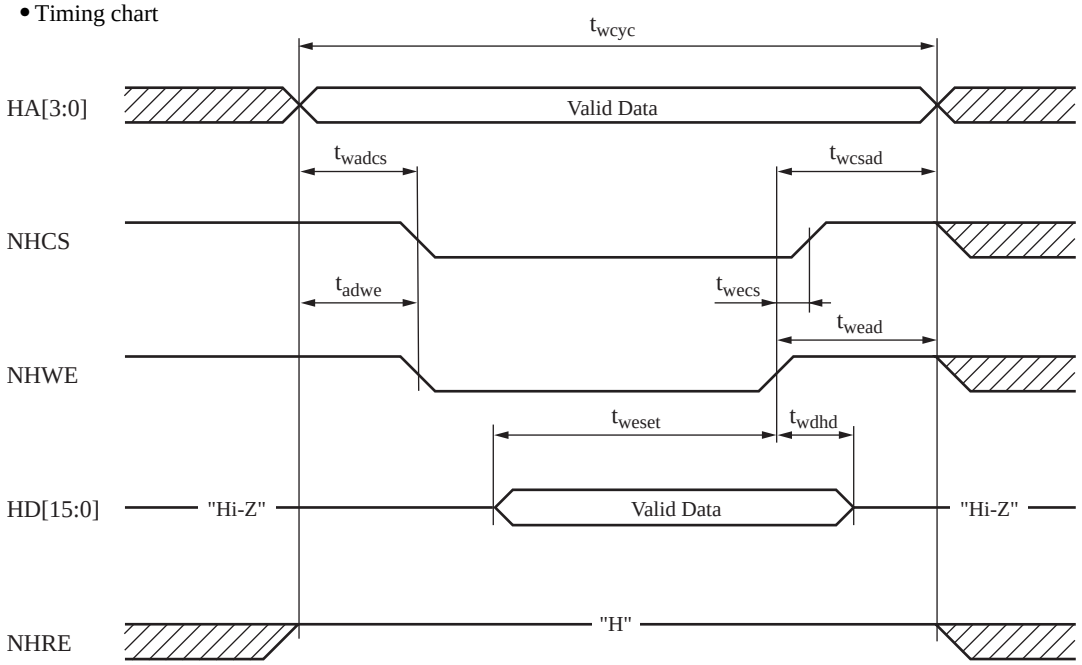
■ Interfaces (continued)

1. Host interface (continued)

1) Direct addressing access (continued)

[Write]

- Timing chart



- AC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Write cycle time	t_{wcyc}	200	—	—	ns
HA[3:0] setup time from the NHCS falling edge	t_{wadcs}	0	—	—	ns
HA[3:0] setup time from the NHRE falling edge	t_{adwe}	0	—	—	ns
HD[15:0] valid data setup time from the NHWE rising edge	t_{weset}	20	—	—	ns
HA[3:0] hold time from the NHCS rising edge	t_{wcsad}	40	—	—	ns
HA[3:0] hold time from the NHWE rising edge	t_{wead}	40	—	—	ns
NHCS rising edge time from NHWE rising edge	t_{wecs}	0	—	—	ns
HD[15:0] valid data hold time from the NHWE rising edge	t_{wdhd}	1	—	—	ns

■ Interfaces (continued)

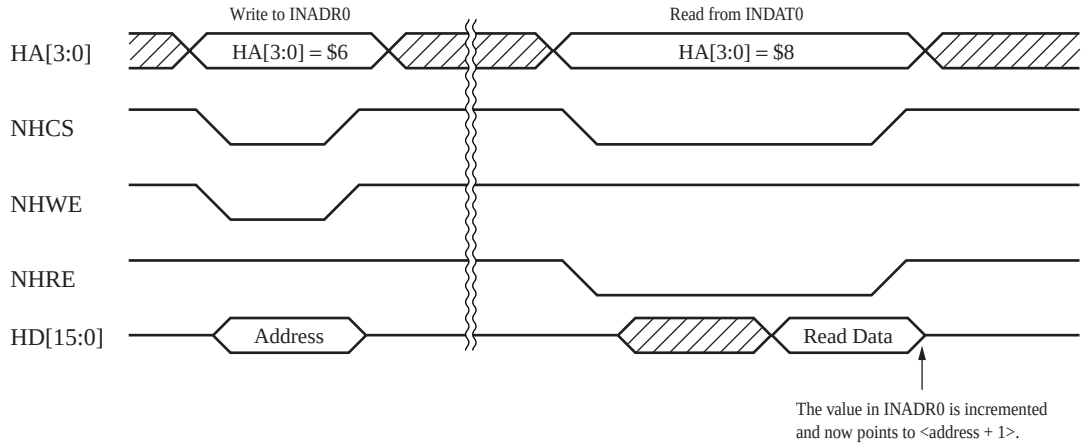
1. Host interface (continued)

2) Indirect addressing access

[Read]

(1) The indirect address value is written to INADR0 (HA[3:0] = $6). This sets the indirect address.

(2) Data is read from INDAT0 (HA[3:0] = $8). At this time the data at the address set in INADR0 is read out over this device's internal bus, although it appears to be read out from INDAT0. This completes the read operation. At the same time, the value stored in INADR0 is automatically incremented (auto increment).

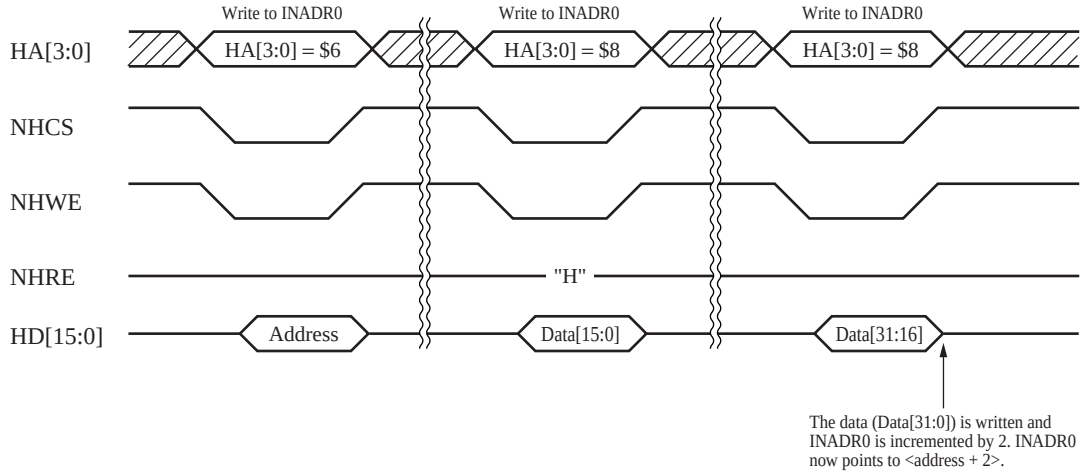


[Write]

(1) The indirect address value is written to INADR0 (HA[3:0] = $6). This sets the indirect address. (Since writes are performed in 32-bit units, the set indirect address must be an even value.)

(2) Data is written to INDAT0 (HA[3:0] = $8). This latches the lower 16 bits of the data.

(3) Another data is written to INDAT0 (HA[3:0] = $8). This, in conjunction with the 16 bits of data acquired in step (2) above, forms a 32-bit data unit, which is then written over the internal data bus. At the same time, the value stored in INADR0 is automatically incremented by 2 (auto increment).



■ Interfaces (continued)

2. DMA transfer interface (DIF)

The DMA transfer interface (DIF) transfers data using DMA between the external host and this device's DMA data transfer buffer memory (WRDM). Since WRDM has a size of 1 024 32-bit words, the maximum valid data count is 2 048.

(This function is valid when the CHIPCTL0 direct addressing access register dmasel bit is 0.)

The WRDM can be accessed in two ways: by read or write instructions from the SRISC and by DMA data transfers (read or write) from the external host.

Since there are two techniques, which technique gains access is arbitrated by the DIF internal arbitration circuit.

Access requests to the arbitration circuit are issued from the SRISC by instruction execution, and from the external host by writing a 1 to the DIFACC (HA[3:0] = $A) req register (a direct addressing register). If requests are issued to the arbitration circuit at the same time, access permission is granted according to the priority determined by the value of the difreg ($0020) indirect addressing access register.

Note that there are two DMA transfer modes: "single bus cycle DMA transfer mode", in which access is synchronized with the DMA clock signal (DMACLK), and "two bus cycle DMA transfer mode", in which transfers are not dependent on a clock signal.

3. Code output interface

The code output interface is provided to transfer data to a communication system or to the storage system media and outputs a multiplexed AV bit stream to external circuits.

There are two major classes of output formats provided by the code output interface: "standalone mode (8-bit parallel)", which outputs the bit stream using a dedicated set of pins, and "DMA transfer mode (16-bit parallel) which outputs using an external host bus shared with the host interface.

The setting of the CHIPCTL0 dma sel register (a direct addressing register) selects which of these two output formats is used. If this bit is set to 0, standalone mode is used, and if set to 1, DMA transfer mode is used.

Additionally, there are three clock modes in standalone mode. These consist of two modes that use a code output clock (RCLKI) input to this device, "inverted clock input standalone mode", and "noninverted clock input standalone mode as well as a mode that uses a code output clock (RCLKO) output from this device, "ARIB parallel interface standard mode (TS output)".

Also note that there are two DMA transfer modes which differ in the number of bus cycles required to transfer data, "single bus cycle DMA transfer mode" and "two bus cycle DMA transfer mode".

The table below summarizes these modes, and lists the clock frequencies, pins, and other items used in each mode. Note that in every one of these modes, the maximum amount of valid output data per single handshake operation is 2 048 bytes, and that the maximum average output bit rate is 15 Mbps.

Mode		Pin names used	Clock frequencies	Output data format
Standalone mode	Inverted/noninverted clock input	CDO[7:0], CDREADY, CDACK, RCLKI, (IPIC, VOB)[3]	RCLKI 16 MHz maximum	MSB first
	ARIB parallel interface standard	CDO[7:0], CDREADY, RCLKI, IPIC, (VOB)[3]	RCLKO 6.75 MHz, 3.375 MHz	MSB first
DMA transfer mode	Single bus cycle	HD[15:0], NHDREQ, NHDACK, DMACLK	DMACLK 33 MHz maximum	Big Endian/ Little Endian
	Two bus cycle	HD[15:0], NHCS, HA[3:0], NHRE, NHWE, NHDREQ	Clock signal not required	Big Endian/ Little Endian

■ Interfaces (continued)

4. Video data input interface

• Interface pin descriptions

Pin Name	I/O	Description
VIN[7:0]	I	Video data input Video data must be input in synchronization with the video data input clock (VCLK). The format of the input video data must be ITU-R BT.656 (level D1, 4:2:2).
VCLK	I	Video data input clock input

The video data input to this product assumes that the input signal has been time base corrected (TBC) in the stage prior to this product.

This product also assumes that the PCM data input and the video data input are locked in the stage prior to this product.

5. PCM data input (audio data input) interface

The PCM data input interface is provided for input of the audio data (PCM coded data) to the audio encoding block.

This product performs encoding for audio data that is sampled at a sampling frequency of 48 kHz.

It uses either Dolby Digital or linear PCM as the encoding technique.

There are limitations on the PCM data input quantization word length depending on the encoding technique used.

For Dolby Digital processing, this product supports 16, 18, 20, and 24-bit quantizations. For linear PCM processing it only supports 16-bit quantization.

This product supports 2-channel (left/right) audio, and data is 1-bit serial data transmitted MSB first.

This product supports the I2S, left justified, and right justified formats as input formats.

The PCM data input interface can be switched between two modes: master mode and slave mode.

In master mode, a PCM master clock signal (256 or 384 fs) is input to this product's PCKI pin and used to create the output PCM master clock output signal, the bit clock signal, and the left/right channel discrimination clock signal for the external A/D converter. These signals are output from the PCKO, BCKIO, and LRCKIO pins, respectively.

In slave mode, the PCKI, BCKIO, and LRCKIO pins are used to input a PCM master clock signal (256 or 384 fs), bit clock signal, and a left/right channel discrimination clock signal, respectively. (In this mode, the PCKO pin must be left open (N.C.).)

All the PCM data input interface parameter settings are set from multiplexing block SRISC microcode.

• Interface pin descriptions

Pin Name	I/O	Description
BCKIO	I/O	Bit clock output
LRCKIO	I/O	Left/right channel discrimination clock output
ADIN	I	PCM data (audio data) input
PCKI	I	PCM master clock input
PCKO	O	PCM master clock output

■ Interfaces (continued)

6. SDRAM interface

This product's SDRAM interface supports JEDEC standard single data rate SDRAM with a CAS latency of 3, a cycle time of 8 ns or faster, and an access time of 6 ns or faster.

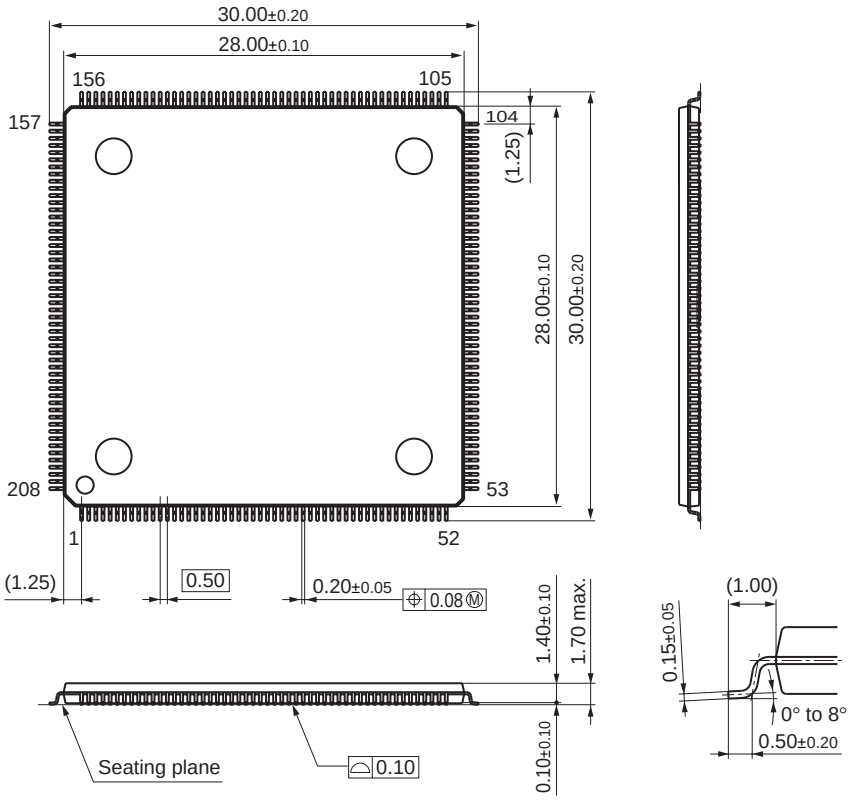
Data is transferred in 32-bit units, and either one 64M 32-bit data path SDRAM chip or two 64M 16-bit data path SDRAM chips may be used.

- Pin Descriptions

Pin Name	I/O	Description
MCLK	O	External memory clock output
MCLKIN	I	Clock input for data transfers between external memory and this product
NMCS	O	External memory chip select output
NMRAS	O	External memory RAS output
NMCAS	O	External memory CAS output
NMWE	O	External memory write enable output
MDQM	O	External memory data output buffer control
MA[13 : 0]	O	External memory address output
MDQ[31 : 0]	I/O	External memory data I/O (These pins have built-in pull-up resistors.)
MCKE	O	External memory CKE output

■ Package Dimensions (Unit: mm)

- LQFP208-P-2828 (Lead-free package)



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