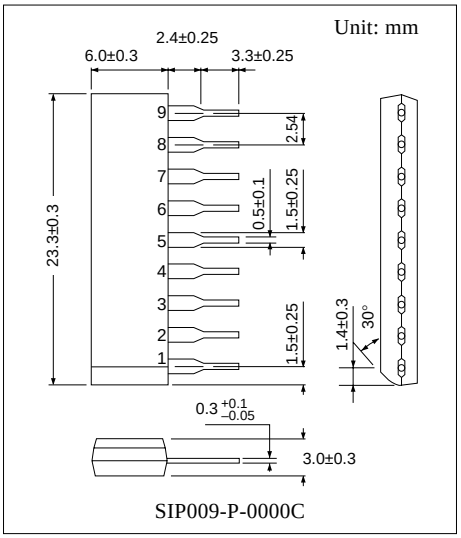
AN8029

Self-excited RCC pseudo-resonance type AC-DC switching power supply control IC



■ Overview

The AN8029 is an IC developed for controlling the self-excited switching power supply employing the RCC pseudo-resonance type control method.
It is compact, equipped only with the necessary minimum functions.

The maximum on-period and the minimum off-period can be set separately by using the external capacitor and resistor respectively.

It is suitable for the power supply of AV equipment.

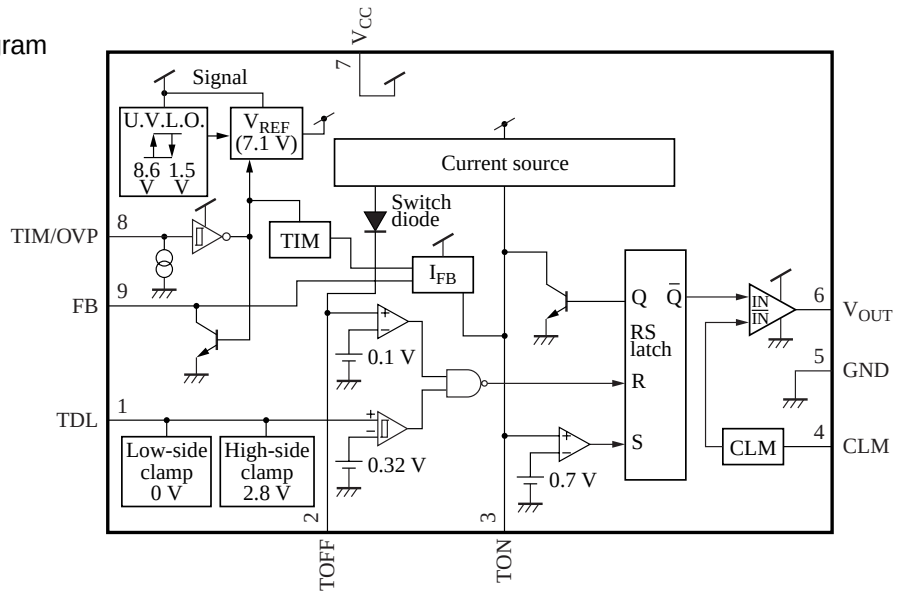
■ Features

- Operating supply voltage range:
  Stop voltage (8.6 V typical) to 34 V
- Output block employs the totem pole system.
- Power MOSFET can be directly driven.
  (output peak current: ±1 A maximum)
- Small pre-start operating current (95 µA typical) allows using a small size start resistor.
- Built-in pulse-by-pulse overcurrent protection function
- Incorporating the protection circuit against malfunction at low voltage (start/stop: 14.9 V/8.6 V)
- Built-in overvoltage protection function (externally resettable)
- Built-in timer latch function
- Equipped with frequency (VF) control function.
- 9-pin single inline package expands the freedom of board design

■ Applications

- Televisions, facsimiles, printers, scanners, video equipment

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Description
1	TDL	Transformer reset detection
2	TOFF	Pin for connecting C and R to set minimum off-period
3	TON	Pin for connecting C to set minimum on-period
4	CLM	Input pin for overcurrent protection detection
5	GND	Grounding pin
6	V_{OUT}	Output pin
7	V_{CC}	Power supply voltage pin
8	TIM/OVP	Pin for use both overvoltage protection circuit and timer latch
9	FB	Photocoupler connection pin for error voltage feedback

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	35	V
Peak output current	I_{6PEAK}	±1	A
Power dissipation	P_D	874	mW
Operating ambient temperature *	T_{opr}	−30 to +85	°C
Storage temperature *	T_{stg}	−55 to +150	°C

Note) ∗: Expect for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	From stop voltage to 34	V

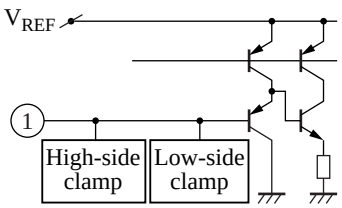
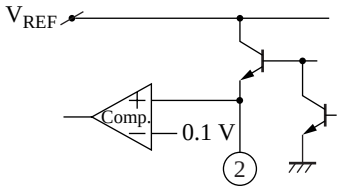
■ Electrical Characteristics at V_{CC} = 18 V, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
U.V.L.O. start supply voltage	V_{7START}		13.4	14.9	16.4	V
U.V.L.O. operation stop supply voltage	V_{7STOP}		7.7	8.6	9.5	V
U.V.L.O. start to stop supply voltage	ΔV_7		5.7	6.3	6.9	V
OVP operation threshold voltage	V_{8OVP}		6.1	7.3	8.5	V
OVP release voltage	V_{7OVP}		7.4	8.2	9	V
OVP operating circuit current 1	I_{7OVP1}	V_{CC} = 9.1 V, V_{OVP} = 8.5 V	0.56	0.79	1.02	mA
OVP operating circuit current 2	I_{7OVP2}	V_{CC} = 20 V, V_{OVP} = 8.5 V	5.9	7.7	9.5	mA
TDL threshold voltage	V_{1TDL}		0.22	0.32	0.42	V
TDL upper limit clamp voltage	$V_{1TDL/H}$	I_{TDL} = 3mA	2	2.8	3.6	V
TDL lower limit clamp voltage	$V_{1TDL/L}$	I_{TDL} = −3mA	− 0.3	0	0.3	V
CLM threshold voltage	V_{4CLM}		180	200	220	mV

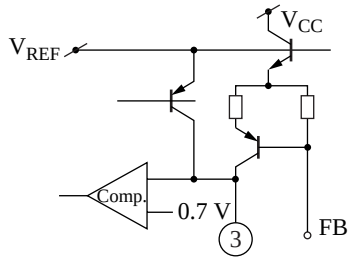
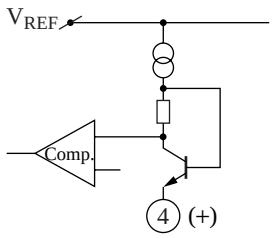
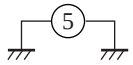
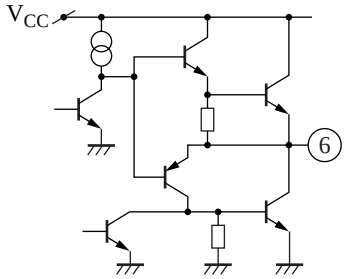
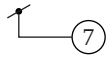
■ Electrical Characteristics at V_{CC} = 18 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TON maximum on-period current	I_{3TON}	FB terminal = open TON terminal = GND	−135	−110	−85	μA
TON upper limit voltage	$V_{3TON/H}$	FB terminal = open	0.55	0.7	0.85	V
TON lower limit voltage	$V_{3TON/L}$	FB terminal = open	− 0.1	0.05	0.2	V
TOFF upper limit voltage	$V_{2TOFF/H}$		0.7	0.9	1.1	V
TOFF lower limit voltage	$V_{2TOFF/L}$		− 0.1	0.05	0.2	V
Output oscillation frequency	f_{OSC}	C_{ON} = 2 200 pF, R_{OFF} = 1.5 kΩ C_{OFF} = 1 000 pF	55	65	75	kHz
Output current feedback current gain	G_{IFB}	I_{FB} = −1 mA	5.05	6.8	8.55	—
Pre-start low-level output voltage	$V_{6STB/L}$	V_{CC} = 10 V, I_{OUT} = 10 mA	—	1	1.25	V
Low-level output voltage 1	$V_{6L(1)}$	I_{OUT} = 10 mA	—	0.9	2	V
Low-level output voltage 2	$V_{6L(2)}$	I_{OUT} = 100 mA	—	1.1	2.2	V
High-level output voltage 1	$V_{6H(1)}$	I_{OUT} = −10 mA	15.7	16.5	—	V
High-level output voltage 2	$V_{6H(2)}$	I_{OUT} = −100 mA	15.5	16.3	—	V
Pre-start circuit current	I_{7STB}	V_{CC} = 12V	55	95	135	μA
Circuit current 1	$I_{7OPR(1)}$	V_{CC} = 18 V TON terminal = GND FB terminal = open	8.55	11.5	14.3	mA
Circuit current 2	$I_{7OPR(2)}$	V_{CC} = 34 V TON terminal = GND FB terminal = open	9.6	12.5	15.4	mA
TDL flowing-out current	I_{1TDL}	V_{TDL} = 0.5 V	−5	0	—	μA

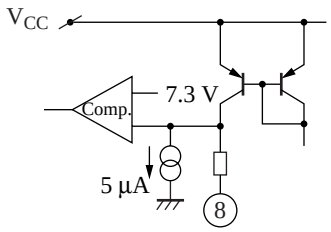
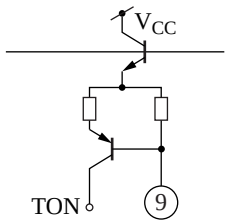
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	I/O
1		TDL: Transformer reset detection terminal. When the transformer reset is detected and low is inputted into the terminal, the output of the IC (V_{OUT}) becomes high. However, low-level signal under the minimum off-period determined by the T_{OFF} is ignored.	I
2		TOFF: Terminal for connecting the resistor and capacitor for determining the minimum off-period (low) of the IC output (V_{OUT}). An equation for approximate calculation of the minimum off-period (T_{OFF}) is as follows: $T_{OFF} = 2.2 \times C \times R$ C: External capacitance R: External resistance	—

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
3		TON: Terminal for connecting the capacitor for determining the maximum on-period (high) of the IC output (V_{OUT}). An equation for approximate calculation of the maximum on-period (T_{ON}) is as follows: $T_{ON} = 6\,500 \times C$ C: External capacitance	—
4		CLM: Input terminal for detection of the pulse-by-pulse overcurrent protection. Normally, it is recommended that a filter be attached externally.	I
5		GND: Grounding terminal	—
6		V_{OUT}: Output terminal for directly driving the power MOSFET. It uses the totem pole type output. The maximum rating of the output current : Peak: ±1 A DC: ±150 mA	O
7		V_{CC}: Terminal for applying power supply voltage. It monitors the supply voltage and has the operation threshold of start/stop/OVP reset.	—

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
8		TIM/OVP: Terminal for use both OVP (overvoltage protection circuit) and timer latch. [OVP] When overvoltage signal of the power supply is detected and high is inputted to the terminal, it turns off the internal circuit. At the same time, it holds that condition (latch). To reset the OVP latch, the V_{CC} should be decreased to a voltage lower than the release voltage. [Timer latch] It detects the output voltage fall due to the overcurrent condition of the power supply output through the current level inputted to IFB. When the I_{IFB} decreases under the current of certain value, the charge current flows in the capacitor which is connected to this terminal. Then, when the capacitor is charged up to the threshold voltage of the OVP, the OVP works so that the IC could keep the operation stop condition.	I
9		FB: Terminal for connecting the photocoupler for error voltage feedback of the power supply output. It is possible to cancel about 180 mA of the dark current of photocoupler.	I

■ Application Notes

[1] Operation descriptions

1. Start/stop circuit block

• Start mechanism

When AC voltage is applied and the supply voltage reaches the start voltage through the current from start resistance, the IC starts operation. Then the power MOSFET driving starts. Thereby, bias is generated in the transformer and the supply voltage is given from the bias coil to the IC. (point a in figure 1)

During the period from the time when the start voltage is reached and the voltage is generated in the bias coil to the time when the IC is provided with a sufficient supply voltage, the supply voltage of the IC is supplied by the capacitor (C8) connected to V_{CC} .

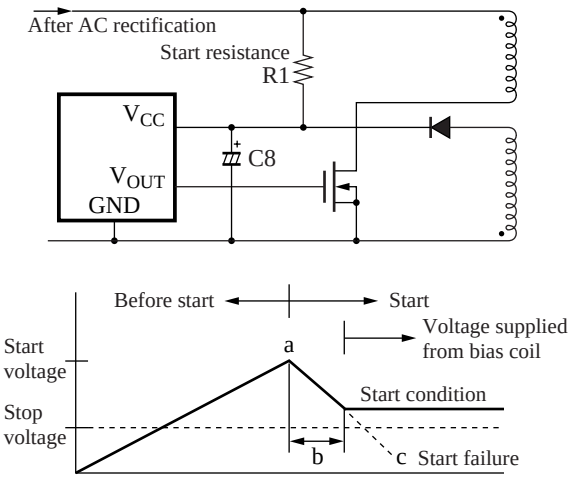


Figure 1

■ Application Notes (continued)

[1] Operation descriptions (continued)

1. Start/stop circuit block (continued)

- Start mechanism (continued)

Since the supply voltage continuously decreases during the above period (area b in figure 1), the power supply is not able to start (state c in figure 1), if the stop voltage of the IC is reached before the sufficient supply voltage is supplied from the bias coil.

- Function

The start/stop circuit block is provided with the function to monitor the V_{CC} voltage, and to start the operation of IC when V_{CC} voltage reaches the start voltage (14.9 V typical), and to stop when it decreases under the stop voltage (8.6 V typical). A large voltage difference is set between start and stop (6.3 V typical) so that it is easier to select the start resistor and the capacitor to be connected to V_{CC}.

Note) To start up the IC operation, the startup current which is a pre-start current plus a circuit drive current is necessary. Set the resistance value so as to supply a startup current of 350 μA.

2. Oscillation circuit

The oscillation circuit generates the pulse signal for turning on/off the power MOSFET by using charge/discharge of the C2, R2 and C3 connected to TOFF (pin 2), TON (pin 3) respectively.

The concept of constant voltage control at the time of making up the switching power supply is fixing the off-period of the power MOSFET and achieving the control by changing the on-period. This on-period control is performed by directly changing the output pulse width of the oscillation circuit.

During the on-period of the power MOSFET, the C2 is charged to the constant voltage (approximately 0.9 V).

On the other hand, the C3 is charged from almost 0 V by the charge current from the TON terminal. When the voltage across the both ends of the C3 reaches approximately 0.7 V (T_a = 75°C), the oscillation circuit output is reversed and the power MOSFET is turned off. At the same time, the C3 is rapidly discharged by the discharge circuit inside the IC and its voltage across the both ends becomes almost 0 V. The charge current from the TON terminal is changed by the feedback signal to the FB terminal (pin 9). (Described later.)

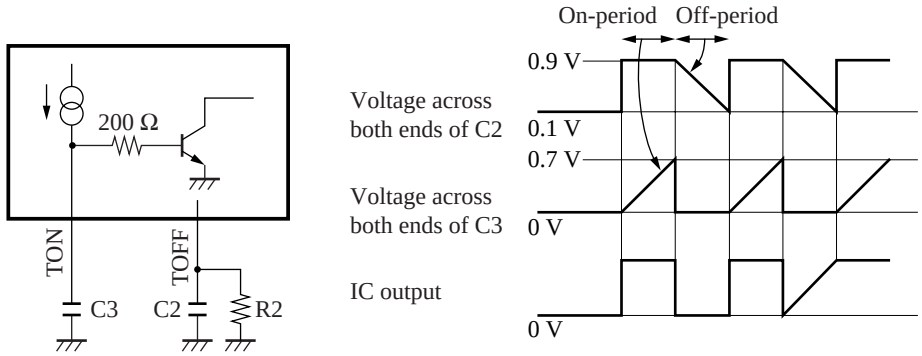


Figure 2. Oscillation circuit operation

An equation for approximate calculation of the maximum on-period $T_{ON(max)}$ of the power MOSFET is as follows:

$$T_{ON(max)} = 6\,500 \times C3$$

When the power MOSFET is off, the TOFF terminal becomes a high impedance state and the C2 starts discharging by the R2. When the voltage across the both ends of C2 decreases to approximately 0.1 V, the oscillation circuit output is reversed again to turn on the power MOSFET. At the same time, the C2 is rapidly charged to approximately 0.9 V. An equation for approximate calculation of the minimum off-period $T_{OFF(min)}$ is as follows:

$$T_{OFF(min)} = 2.2 \times C2 \times R2$$

However, when the voltage-time fed back to the TDL terminal (pin 1) is longer than the T_{OFF} period determined by the C2 and R2, the off-period in the pseudo-resonance circuit operation described below is determined by the former.

By repeating the above operation, the power MOSFET is turned on and off continuously. Figure 2 shows the oscillation waveform at the time when the TDL terminal is pulled down to the GND.

■ Application Notes (continued)

[1] Operation descriptions (continued)

3. Power supply output control system (FB : Feedback)

The constant voltage control of the power supply output is achieved by fixing the off-period of the power MOSFET and changing the on-period. The control of on-period is performed by changing the charge current from the TON terminal to the C3 through the following process: The photocoupler connected to the FB terminal (pin 9) absorbs, from the FB terminal, the feedback current corresponding to the output signal of the output voltage detection circuit provided in the secondary side output. A current approximately 7 times of the current flowing out of the FB terminal flows out of the TON terminal as the charge current for the C3. (Refer to figure 3.)

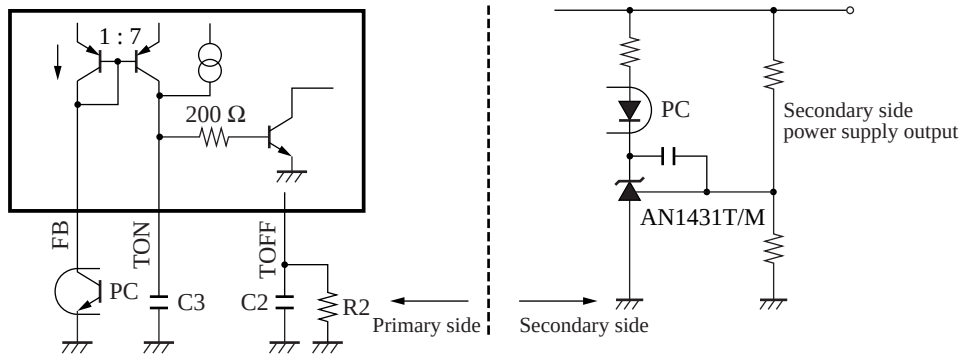


Figure 3. Power supply output control system

The higher the AC input voltage of the current becomes, or the smaller the load current becomes, the larger the current flowing out of the FB terminal becomes. When the current flowing out of the FB terminal becomes larger, the charging to C3 becomes faster and the on-period becomes shorter.

In addition, the system has cancellation capability of about 180 μA for the dark current of the photocoupler. (Refer to figure 4.)

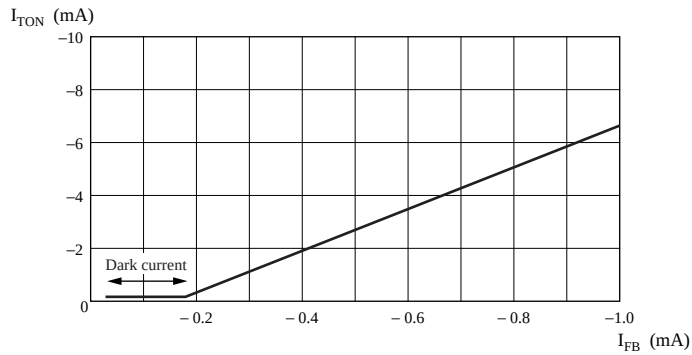


Figure 4. Feedback current versus charge current characteristics

4. Pseudo-resonance operation (Power MOSFET turn-on delay circuit)

For the AN8029, the pseudo-resonance operation becomes possible by making connection as shown in figure 5. The C7 is a resonance capacitor, and the R9 and C9 constitute the delay circuit for regulating the turn-on of power MOSFET. When the power MOSFET is turned off, the voltage generated in the drive coil is inputted to the TDL (time delay) terminal (pin 1) through the R9 and C9. While high-level signal (higher than threshold voltage 0.32 V) is inputted, the power MOSFET remains off. Also, the TDL terminal has the high/low side clamping capability. The upper limit of clamping voltage is 2.8 V typical (when sink current: 3 mA) and the lower limit of clamping voltage is approximately 0 V (typical) (when source current: 3 mA). The off-period of the power MOSFET is determined by the following periods whichever longer: The time until the TDL terminal input voltage becomes a voltage lower than the threshold voltage as the transformer started the resonance operation and the drive coil voltage drops, and the minimum off-period $T_{OFF(min)}$ of the internal oscillation circuit. (Refer to description on the oscillation circuit.)

■ Application Notes (continued)

[1] Operation descriptions (continued)

4. Pseudo-resonance operation (Power MOSFET turn-on delay circuit) (continued)

As for the turn-on of power MOSFET, determine the delay time by selecting the constant of the R9 and C9 so that it turns on at 1/2 cycle of the resonance frequency.

In a simplified method, select so that the voltage waveform turns on at zero voltage. (Refer to figure 6)

The approximate value of resonance frequency can be obtained by the following equations:

$$f_{SYNC} = \frac{1}{2\pi\sqrt{L \cdot C}} \quad [Hz]$$

C: resonance capacitance
L: inductance of transformer's primary coil

Therefore, the turn-on delay time $t_{pd(ON)}$ for turning on the power MOSFET at 1/2 cycle of resonance frequency is as follows:

$$t_{pd(ON)} = \pi\sqrt{L \cdot C} \quad [s]$$

5. Notes on R9 and C9 selection

If too low resistance is selected for the R9, the current flowing into the TDL terminal after the start of power supply exceeds the maximum rating value and there is a possibility of causing malfunction (destruction in the worst case). It is recommended that about 8 kΩ to 10 kΩ be selected for the R9 though it depends on the supply voltage from the bias coil.

Therefore, adjust $t_{pd(ON)}$ with C9 after converting from the inductance of transformer being used and the resonance capacitance.

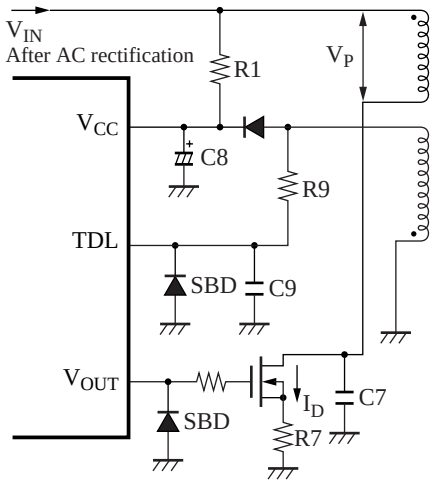


Figure 5

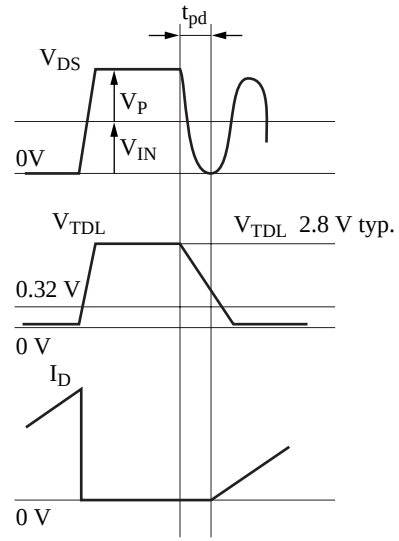


Figure 6

6. Overcurrent protection circuit

The overcurrent of the power supply output is proportional to the value of current flowing in the main switch in the primary side (the power MOSFET). Taking advantage of the above fact, the overcurrent of the power supply output is restricted by regulating the upper limit of the pulse current flowing in the main switch to protects the parts easily damaged by the overcurrent.

The current flowing in the main switch is detected by monitoring the voltage of both ends of the low resistor which is connected between the source of power MOSFET and the power supply GND. When the power MOSFET is turned on and the threshold voltage of CLM (Current Limit) is detected, the circuit turns off the output and turns off the power MOSFET to control so as not to allow further current flow. The threshold voltage of CLM is approximately 0.2 V (typical) under T_a = 25°C with respect to GND. This control is repeated for each cycle. Once the overcurrent is detected, the off condition is kept during that cycle and it can not be turned on until the next cycle. The overcurrent detection method described in the above is called "pulse-by-pulse overcurrent detection".

■ Application Notes (continued)

[1] Operation descriptions (continued)

6. Overcurrent protection circuit (continued)

The R6 and C6 in figure 7 construct the filter circuit for removing the noise generated by the parasitic capacitance equivalently accompanied when turning on the power MOSFET. For overcurrent detection resistance R7, the carbon resistor should be used but not the wire winding resistor, because the high-frequency current flows in it.

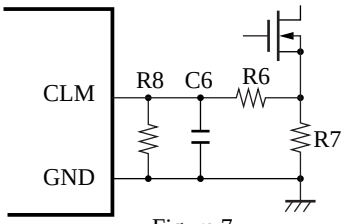


Figure 7

• Notes on the detection level precision

This overcurrent detection level reflects on the operating current level of the power supply overcurrent protection. Therefore, if this detection level fluctuates with temperature or variability, the operating current level of the overcurrent protection of power supply itself also fluctuates. Since such level fluctuation means the necessity for an increase in the withstanding capability of used parts and in the worst case it means the cause of destruction, the accuracy of detection level is increased as much as possible for the AN8029 (approximately ±4%).

7. Overvoltage protection circuit (OVP)

OVP is an abbreviation of over voltage protection. It refers to a self-diagnosis function, which stops the power supply to protect the load when the power supply output generates abnormal voltage higher than the normal output voltage due to failure of the control system or an abnormal voltage applied from the outside. (Refer to figure 8.)

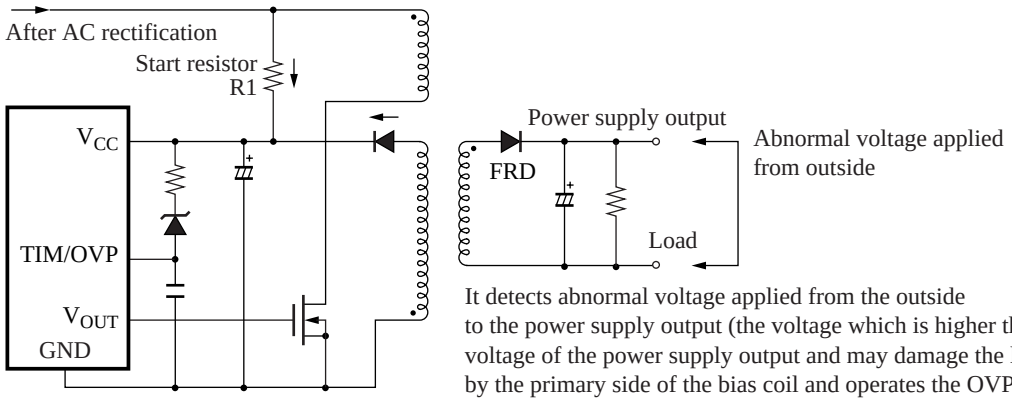


Figure 8

Basically, it is set to monitor the voltage of supply voltage V_{CC} terminal of the IC. Normally, the V_{CC} voltage is supplied from the transformer drive coil. Since this voltage is proportional to the secondary side output voltage, it still operates even when the secondary side output is in overvoltage.

1) When the voltage input to the OVP terminal exceeds the threshold voltage (7.3 V typical) as the result of power supply output abnormality, the protective circuit shuts down the internal reference voltage of the IC to stop all of the controls and keeps this stop condition.
2) The OVP reset is done by decreasing the supply voltage (V_{CC} < 8.2 V typical: OVP release supply voltage).
   (1) When the supply voltage becomes lower than the stop voltage,
   (2) When the supply voltage becomes lower than the OVP release voltage,

   The discharge circuit is incorporated so that the electric charge which is charged in the capacitor connected to the OVP terminal can be discharged momentarily for the next re-start.

$$V_{th(OUT)} = \frac{\text{secondary side output voltage under normal operation } V_{OUT}}{V_{CC} \text{ terminal voltage under normal operation}} \times V_7$$

$V_7 = V_{th(OVP)} + V_Z$

$V_{th(OUT)}$: Secondary side output overvoltage threshold value
$V_{th(OVP)}$: OVP operation threshold value
V_Z : Zener voltage (externally attached to OVP terminal)

■ Application Notes (continued)

[1] Operation descriptions (continued)

7. Overvoltage protection circuit (OVP) (continued)

• Operating supply current characteristics

While the OVP is operating, the decrease of the supply current causes the rise of the supply voltage V_{CC} , and in the worst case, the guaranteed breakdown voltage of the IC (35 V) can be exceeded. In order to prevent the rise of supply voltage, the IC is provided with such characteristics as that the supply current rises in the constant resistance mode. This characteristics ensure that the OVP can not be released unless the AC input is cut, if the supply voltage V_{CC} under OVP operating has been stabilized over the OVP release supply voltage (which depends on start resistor selection). (Refer to figure 9.)

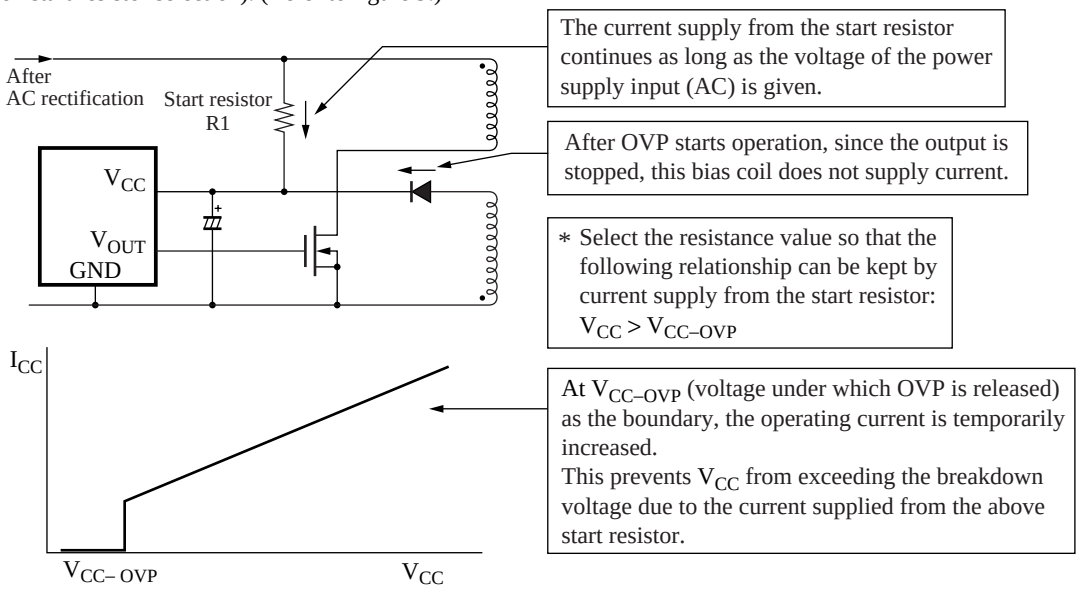


Figure 9

8. Timer latch

When the short-circuit or overload of the power supply output continues for a certain period, the pulse-by-pulse overcurrent protection is not sufficient for protection of the transformer, fast recovery diode (FRD), Schottky diode in the secondary side, and the power MOSFET. For this reason, the timer latch function is employed, which stops the power supply by hitting the OVP when the overcurrent condition continues for a certain period.

The short-circuit or overload of the power supply output is monitored as the decrease of the power supply output (at this time the pulse-by-pulse overcurrent protector is in the operating condition). The decrease of the power supply output is detected as the decrease of current amount at the current feedback terminal of IFB control. When the decrease amount of this current exceeds a certain value, the comparator inside the IC reverses, and the constant current flows to the TIM/OVP terminal.

The external capacitor is connected to the TIM/OVP terminal. Electric charges are accumulated in this capacitor, rising the OVP terminal voltage. When the OVP operating threshold voltage (7.3 V typical) is reached, the OVP starts operation to stop the IC, and keeps this stop condition. (Refer to figure 10.)

• Timer period

The period from the time when an error of the power supply output is detected to the time when the OVP starts operation (hereinafter referred to as "timer period") should be longer than the rise time of the power supply. Since at operation start the IC is in the same condition as the overload or output short-circuit condition, if the timer period is shorter, the power supply works latch and can not start.

Therefore, the IC is designed so that the timer period can be set arbitrarily to by the value of the external capacitor connected to the TIM/OVP terminal. However, particular care should be taken, because too large value of this capacitor may cause the breakdown of the power supply.

■ Application Notes (continued)

[1] Operation descriptions (continued)

8. Timer latch (continued)

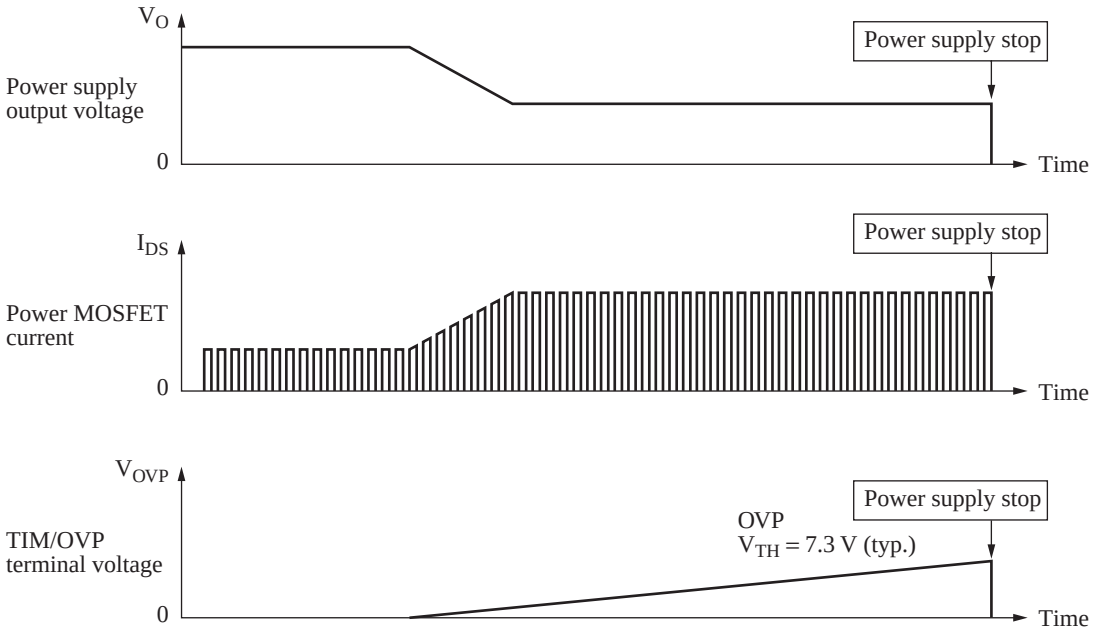


Figure 10. Timer latch basic operation

9. Output block

In order to drive the power MOSFET which is a capacitive load at high speed, this IC is adopting the totem pole (push-pull) type output circuit which performs the sink and source of the current with the NPN transistor as shown in figure 10.

The maximum sink/source current is ± 0.1 A (DC) and the current at peak is ±1.0 A (Peak). The circuit is provided with the sink capability even if the supply voltage V_{CC} is under the stop voltage so that it turns off the power MOSFET without fail.

The peak current capability is mainly required and a particularly too large current is not required constantly. Because the power MOSFET becomes a capacitive load for the output, a large peak current is required for driving it at a high speed. However, after the charge and discharge, a particularly large current is not required to keep such condition. In the case of this IC, the peak current capability of ±1 A is ensured by taking a capacitance value of the power MOSFET used into account.

The parasitic LC of the power MOSFET may produce ringing to decrease the output pin under the GND potential. When the voltage decrease of the output pin becomes larger than the voltage drop of diode and its voltage becomes negative, the parasitic diode consisting of the substrate and collector of the output NPN turns on. This phenomenon can cause the malfunction of device. In such a case, the Schottky barrier diode should be connected between the output and GND.

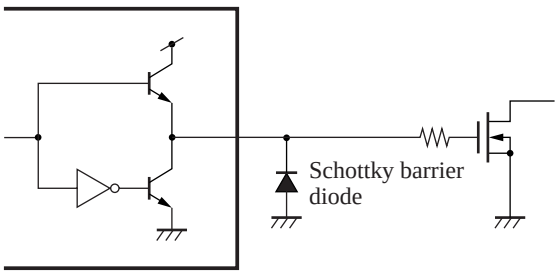


Figure 11

■ Application Notes (continued)

[2] Design reference data

- How to start the soft start function by external parts

The power supply rises under overload condition due to the capacitor connected to the power supply output. In this condition, since the voltage of the power supply output is low, the normal constant voltage control attempts to rise the power supply output at the maximum duty. The control uses the pulse-by-pulse overcurrent protection (CLM) , attempting to limit the current. However, the pulse can not be brought down to zero due to delay of filter, etc. As a result, a large current flows into the main switch (the power MOSFET) or the diode in the secondary side, and in the worst case these parts are damaged. For this reason, the soft start function is used to suppress the rush current at start of the power supply.

As shown in figure 12, the R3 and C4 are connected between the FB terminal (pin 9) and the GND terminal (pin 5) to use the soft start function. When the supply voltage of the IC reaches the start voltage and the start circuit begins operation, the open bias is outputted to the FB terminal.

By this voltage, the charge current flows in the C4 to become flowing-out current of the FB terminal (I_{FB}) and output control begins under the condition in which T_{ON} period is short. The I_{FB} decreases with elapse of time, since it changes proportionally to the charge current of the C4. The CLM circuit operates, depending on the sum of the R7 end-to-end voltage by the current which flows in the power MOSFET at power-on and the R6 end-to-end voltage by the charge current of the C4.

Therefore, since the current which flows in the power MOSFET at power-on gradually increases, the rush current can be suppressed.

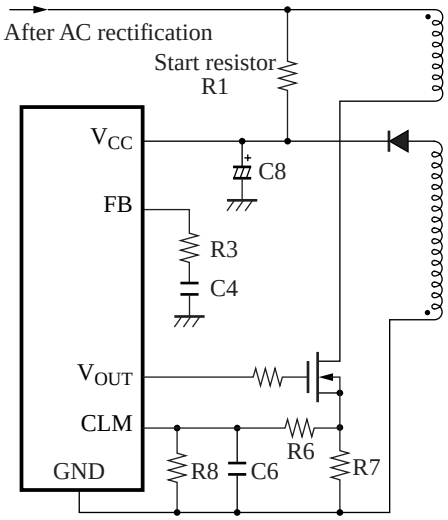


Figure 12

■ Application Circuit Example