NBSG16VS

2.5V/3.3V SiGe Differential Receiver/Driver with Variable Output Swing

The NBSG16VS is a differential receiver/driver targeted for high frequency applications that require variable output swing. The device is functionally equivalent to the EP16VS device with much higher bandwidth and lower EMI capabilities. This device may be used for applications driving VCSEL lasers.

Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVTTL, LVCMOS, CML, or LVDS. The output amplitude is varied by applying a voltage to the V_{CTRL} input pin. Outputs are variable swing ECL from 100 mV to 750 mV amplitude, optimized for operation from V_{CC} - V_{EE} = 3.0 V to 3.465 V.

The V_{BB} and V_{MM} pins are internally generated voltage supplies available to this device only. The V_{BB} is used as a reference voltage for single-ended NECL or PECL inputs and the V_{MM} pin is used as a reference voltage for LVCMOS inputs. For single-ended input operation, the unused complementary differential input is connected to V_{BB} or V_{MM} as a switching reference voltage. V_{BB} or V_{MM} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{MM} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} and V_{MM} outputs should be left open.

- Maximum Input Clock Frequency up to 12 GHz Typical
- Maximum Input Data Rate up to 12 Gb/s Typical
- 40 ps Typical Rise and Fall Times (V_{CTRL} = V_{CC} - 1 V)
- 120 ps Typical Propagation Delay (V_{CTRL} = V_{CC} - 1 V)
- Variable Swing PECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Variable Swing NECL Output with NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = -2.375 V to -3.465 V
- Output Level (100 mV to 750 mV Peak-to-Peak Output; V_{CC} - V_{EE} = 3.0 V to 3.465 V), Differential Output Only
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V EP Devices
- V_{BB} and V_{MM} Reference Voltage Output

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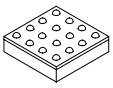
MARKING DIAGRAM*



FCBGA-16
BA SUFFIX
CASE 489

QFN-16
MN SUFFIX
CASE 485G

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NBSG16VSBA	4x4 mm FCBGA-16	100 Units/Tray
NBSG16VSBAR2	4x4 mm FCBGA-16	500/Tape & Reel
NBSG16VSMN	3x3 mm QFN-16	123 Units/Rail
NBSG16VSMNR2	3x3 mm QFN-16	3000/Tape & Reel

Board	Description
NBSG16VSBAEVB	NBSG16VSBA Evaluation Board

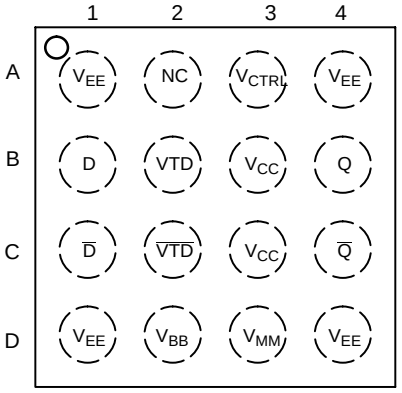


Figure 1. BGA-16 Pinout (Top View)

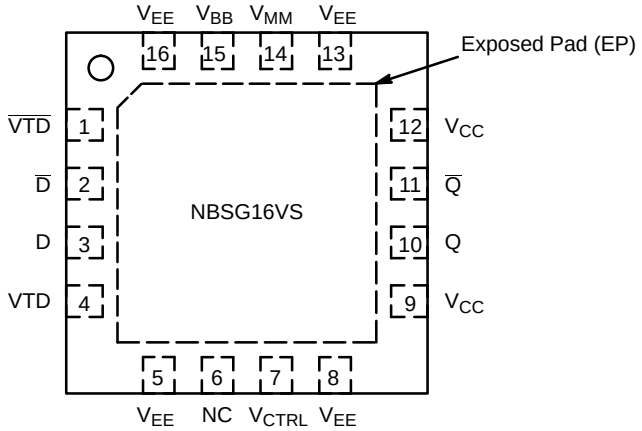


Figure 2. QFN-16 Pinout (Top View)

Table 1. Pin Description

Pin		Name	I/O	Description
BGA	QFN			
C2	1	$\overline{VTD}$	-	Internal 50 Ω Termination Pin. See Table 2.
C1	2	$\overline{D}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
B1	3	D	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Input. Internal 75 kΩ to V_{EE}.
B2	4	VTD	-	Internal 50 Ω Termination Pin. See Table 2.
A1,D1,A4, D4	5,8,13,16	V_{EE}	-	Negative Supply Voltage
A2	6	NC	-	No Connect
A3	7	V_{CTRL}		Output Amplitude Swing Control. Bypass Pin to V_{CC} through 0.1 μF Capacitor.
B3,C3	9,12	V_{CC}	-	Positive Supply Voltage
B4	10	Q	RSECL Output	Noninverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V
C4	11	$\overline{Q}$	RSECL Output	Inverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V
D3	14	V_{MM}	-	LVCMOS Reference Voltage Output. (V_{CC} - V_{EE})/2
D2	15	V_{BB}	-	ECL Reference Voltage Output
N/A	-	EP	-	Exposed Pad. (Note 2)

1. The NC pin is electrically connected to the die and must be left open.
2. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation. The thermally exposed pad on package bottom (see case drawing) must be attached to a heat-sinking conduit.
3. In the differential configuration when the input termination pins (VTD, $\overline{VTD}$) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.

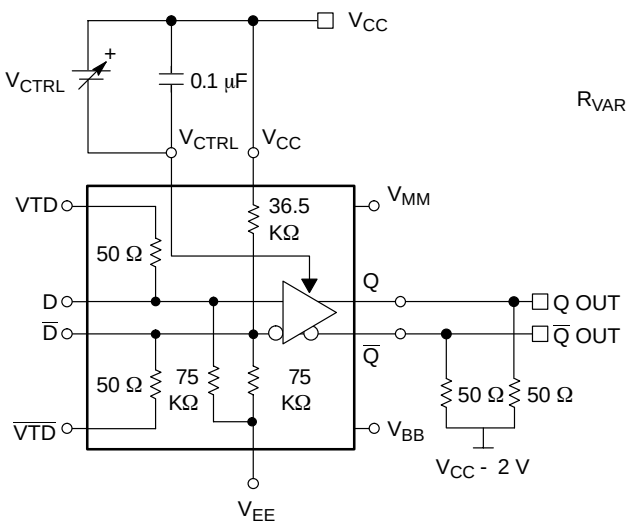


Figure 3. Logic Diagram/ Voltage Source Implementation

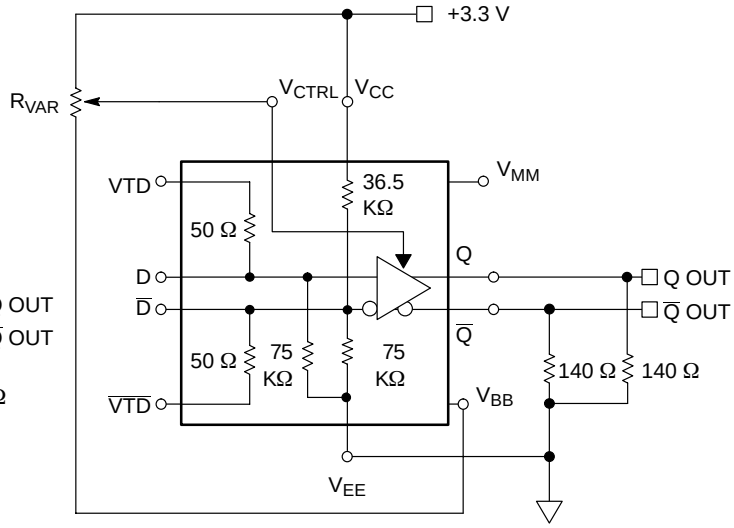


Figure 4. Alternative Voltage Source Implementation

Table 2. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD and $\overline{VTD}$ to V_{CC}
LVDS	Connect VTD and $\overline{VTD}$ Together
AC-COUPLED	Bias VTD and $\overline{VTD}$ Inputs within Common Mode Range (V_{IHCMR})
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL	An external voltage should be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTL.
LVCMOS	V_{MM} should be connected to the unused complementary differential input.

Table 3. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor (D, $\overline{D}$)		75 kΩ
Internal Input Pullup Resistor ($\overline{D}$)		36.5 kΩ
ESD Protection	Human Body Model Machine Model	> 2 kV > 100 V
Moisture Sensitivity (Note 1)	FCBGA-16 QFN-16	Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		192
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		-3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 -3.6	V V
V_{INPP}	Differential Input Voltage |D - $\overline{D}$|	V_{CC} - $V_{EE} \ge$ 2.8 V V_{CC} - V_{EE} < 2.8 V		2.8 $\|V_{CC} - V_{EE}\|$	V V
I_{OUT}	Output Current	Continuous Surge		25 50	mA mA
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{BB}	V_{BB} Sink/Source			1	mA
I_{MM}	V_{MM} Sink/Source			1	mA
TA	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 LFPM 500 LFPM 0 LFPM 500 LFPM	16 FCBGA 16 FCBGA 16 QFN 16 QFN	108 86 41.6 35.2	°C/W °C/W °C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 3) 2S2P (Note 4)	16 FCBGA 16 QFN	5.0 4.0	°C/W °C/W
T_{sol}	Wave Solder	< 15 sec.		225	°C

2. Maximum Ratings are those values beyond which device damage may occur.
3. JEDEC standard 51-6 multilayer board - 2S2P (2 signal, 2 power).
4. JEDEC standards multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS, INPUT WITH VARIABLE PECL OUTPUT V_{CC} = 2.5 V; V_{EE} = 0 V (Note 5)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	18	25	32	18	25	32	18	25	32	mA
V_{OH}	Output HIGH Voltage (Note 6)	1315	1440	1565	1305	1430	1555	1305	1430	1555	mV
V_{OL}	Output LOW Voltage (Note 6) (Max Swing) (V_{CTRL} = V_{CC} - 600 mV)	645 1090	765 1210	885 1330	605 1035	725 1155	845 1275	600 1010	720 1130	840 1250	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Notes 8 and 9)	V_{THR} + 75	V_{CC} - 1000*	V_{CC}	V_{THR} + 75	V_{CC} - 1000*	V_{CC}	V_{THR} + 75	V_{CC} - 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Notes 8 and 10)	V_{IH} - 2500	V_{CC} - 1400*	V_{THR} - 75	V_{IH} - 2500	V_{CC} - 1400*	V_{THR} - 75	V_{IH} - 2500	V_{CC} - 1400*	V_{THR} - 75	mV
V_{BB}	PECL Output Voltage Reference	1080	1140	1200	1080	1140	1200	1080	1140	1200	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7) (Differential Configuration)	1.2		2.5	1.2		2.5	1.2		2.5	V
V_{MM}	CMOS Output Voltage Reference (V_{CC} - V_{EE})/2	1100	1250	1400	1100	1250	1400	1100	1250	1400	mV
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

Table 6. DC CHARACTERISTICS, INPUT WITH VARIABLE PECL OUTPUT V_{CC} = 3.3 V; V_{EE} = 0 V (Note 11)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	20	27	34	20	27	34	20	27	34	mA
V_{OH}	Output HIGH Voltage (Note 6)	2095	2220	2345	2085	2210	2335	2075	2200	2325	mV
V_{OL}	Output LOW Voltage (Note 6) (Max Swing) (V_{CTRL} = V_{CC} - 600 mV)	1275 1750	1395 1870	1515 1990	1285 1730	1405 1850	1525 1970	1295 1715	1415 1835	1535 1955	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Notes 8 and 9)	V_{THR} + 75	V_{CC} - 1000*	V_{CC}	V_{THR} + 75	V_{CC} - 1000*	V_{CC}	V_{THR} + 75	V_{CC} - 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Notes 8 and 10)	V_{IH} - 2500	V_{CC} - 1400*	V_{THR} - 75	V_{IH} - 2500	V_{CC} - 1400*	V_{THR} - 75	V_{IH} - 2500	V_{CC} - 1400*	V_{THR} - 75	mV
V_{BB}	PECL Output Voltage Reference	1880	1940	2000	1880	1940	2000	1880	1940	2000	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7) (Differential Configuration)	1.2		3.3	1.2		3.3	1.2		3.3	V
V_{MM}	CMOS Output Voltage Reference (V_{CC} - V_{EE})/2	1500	1650	1800	1500	1650	1800	1500	1650	1800	mV
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above tables after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to -0.965 V.
6. All loading with 50 Ω to V_{CC}-2.0 volts. V_{OH}/V_{OL} measured at V_{IH}/V_{IL}.
7. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
8. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM}. $V_{THR(MIN)}$ = V_{IHCMR} + 75 mV. $V_{THR(MAX)}$ = V_{IHCMR} - 75 mV.
9. V_{IH} cannot exceed V_{CC}.
10. V_{IL} always ≥ V_{EE}.
11. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to -0.165 V.

*Typicals used for testing purposes.

Table 7. DC CHARACTERISTICS, NECL INPUT WITH VARIABLE NECL OUTPUT

V_{CC} = 0 V; V_{EE} = -3.465 V to -2.375 V (Note 12)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	20	27	34	20	27	34	20	27	34	mA
VOH	Output HIGH Voltage (Note 13) -3.465 V ≤ V_{EE} ≤ -3.0 V -3.0 V < V_{EE} ≤ -2.375 V	 -1205 -1185	 -1080 -1060	 -955 -935	 -1215 -1195	 -1090 -1070	 -965 -945	 -1225 -1195	 -1100 -1070	 -975 -945	mV
V_{OL}	Output LOW Voltage (Note 13) -3.465 V ≤ V_{EE} ≤ -3.0 V (Max Swing) (V_{CTRL} = V_{CC} - 600 mV) -3.0 V < V_{EE} ≤ -2.375 V (Max Swing) (V_{CTRL} = V_{CC} - 600 mV)	 -2000 -1560 -1855 -1410	 -1910 -1440 -1620 -1215	 -1820 -1320 -1290 -1000	 -1990 -1580 -1895 -1460	 -1900 -1460 -1705 -1290	 -1810 -1340 -1425 -1100	 -1980 -1595 -1900 -1490	 -1890 -1475 -1730 -1330	 -1800 -1355 -1470 -1150	mV mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Notes 15 and 16)	V_{THR} + 75	V_{CC} - 1000*	V_{CC}	V_{THR} + 75	V_{CC} - 1000*	V_{CC}	V_{THR} + 75	V_{CC} - 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Notes 15 and 17)	V_{IH} - 2500	V_{CC} - 1400*	V_{THR} - 75	V_{IH} - 2500	V_{CC} - 1400*	V_{THR} - 75	V_{IH} - 2500	V_{CC} - 1400*	V_{THR} - 75	mV
V_{BB}	NECL Output Voltage Reference	-1420	-1360	-1300	-1420	-1360	-1300	-1420	-1360	-1300	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 14) (Differential Configuration)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
V_{MM}	CMOS Output Voltage Reference (Note 18)	V_{MMT} - 150	V_{MMT}	V_{MMT} + 150	V_{MMT} - 150	V_{MMT}	V_{MMT} + 150	V_{MMT} - 150	V_{MMT}	V_{MMT} + 150	mV
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

12. Input and output parameters vary 1:1 with V_{CC}.
13. All loading with 50 Ω to V_{CC} -2.0 volts. V_{OH}/V_{OL} measured at V_{IH}/V_{IL}.
14. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
15. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM}. $V_{THR(MIN)}$ = V_{IHCMR} + 75 mV. $V_{THR(MAX)}$ = V_{IHCMR} - 75 mV.
16. V_{IH} cannot exceed V_{CC}.
17. V_{IL} always ≥ V_{EE}.
18. V_{MM} typical = $|V_{CC}-V_{EE}| / 2 + V_{EE} = V_{MMT}$.

*Typicals used for testing purposes.

Table 8. AC CHARACTERISTICS for FCBGA-16 V_{CC} = 0 V; V_{EE} = -3.465 V to -3.0 V or V_{CC} = 3.0 V to 3.465 V; V_{EE} = 0 V

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 8) (Note 19)	10.7 (Note 22)	12		10.7 (Note 22)	12		10.7 (Note 22)	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential (V_{CTRL} = V_{CC} - 2 V) D → Q, $\overline{Q}$ (V_{CTRL} = V_{CC} - 1 V) D → Q, $\overline{Q}$	100 100	125 120	145 140	100 100	125 120	145 140	100 100	125 120	145 140	ps
t_{SKEW}	Duty Cycle Skew (Note 20)		3	10		3	10		3	10	ps
t_{JITTER}	RMS Random Clock Jitter f_{in} < 10 GHz Peak-to-Peak Data Dependent Jitter f_{in} < 10 Gb/s		0.8 TBD	2		0.8 TBD	2		0.8 TBD	2	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 21)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times (20% - 80%) @ 1 GHz (V_{CTRL} = V_{CC} - 2 V) Q, $\overline{Q}$ (V_{CTRL} = V_{CC} - 1 V) Q, $\overline{Q}$	30 30	45 40	55 50	30 30	45 40	55 50	30 30	45 40	55 50	ps

19. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V. Input edge rates 40 ps (20% - 80%).
20. t_{SKEW} = $|t_{PLH}-t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 10.
21. $V_{INPP(MAX)}$ cannot exceed V_{CC} - V_{EE} (applicable only when V_{CC} - V_{EE} < 2600 mV).
22. Conditions include input amplitude of 500 mV and V_{CTRL} = V_{CC} - 2 V. Minimum output amplitude guarantee of 100 mV (see Output P-P Spec in Figure 8).

Table 9. AC CHARACTERISTICS for FCBGA-16 V_{CC} = 0 V; -3.0 V < V_{EE} ≤ -2.375 V or 2.375 V ≤ V_{CC} < 3.0 V; V_{EE} = 0 V

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 9) (Note 23)	10.7 (Note 26)	12		10.7 (Note 26)	12		10.7 (Note 26)	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential (V_{CTRL} = V_{CC} - 2 V) D → Q, $\overline{Q}$ (V_{CTRL} = V_{CC} - 1 V) D → Q, $\overline{Q}$	100 100	125 120	145 140	100 100	125 120	145 140	100 100	125 120	145 140	ps
t_{SKEW}	Duty Cycle Skew (Note 24)		3	10		3	10		3	10	ps
t_{JITTER}	RMS Random Clock Jitter f_{in} < 10 GHz Peak-to-Peak Data Dependent Jitter f_{in} < 10 Gb/s		0.9 TBD	3		0.9 TBD	3		0.9 TBD	3	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 25)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times (20% - 80%) @ 1 GHz (V_{CTRL} = V_{CC} - 2 V) Q, $\overline{Q}$ (V_{CTRL} = V_{CC} - 1 V) Q, $\overline{Q}$	25 22	50 45	70 60	25 22	50 45	70 60	25 22	50 45	70 60	ps

23. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V. Input edge rates 40 ps (20% - 80%).
24. t_{SKEW} = $|t_{PLH}-t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 10.
25. $V_{INPP(MAX)}$ cannot exceed V_{CC} - V_{EE} (applicable only when V_{CC} - V_{EE} < 2600 mV).
26. Conditions include input amplitude of 500 mV and V_{CTRL} = V_{CC} - 2 V. Minimum output amplitude guarantee of 100 mV (see Output P-P Spec in Figure 9).

Table 10. AC CHARACTERISTICS for QFN-16 V_{CC} = 0 V; V_{EE} = -3.465 V to -3.0 V or V_{CC} = 3.0 V to 3.465 V; V_{EE} = 0 V

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 8) (Note 27)	10 (Note 30)	12		10 (Note 30)	12		10 (Note 30)	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	(V_{CTRL} = V_{CC} - 2 V) D → Q, $\overline{Q}$	100	140	180	100	140	180	100	140	180	
	(V_{CTRL} = V_{CC} - 1 V) D → Q, $\overline{Q}$	100	135	180	100	135	180	80	135	220	
t_{SKEW}	Duty Cycle Skew (Note 28)		3	20		3	15		3	10	ps
t_{JITTER}	RMS Random Clock Jitter										ps
	f_{in} < 10 GHz		0.5	2		0.5	2		0.5	2	
	Peak-to-Peak Data Dependent Jitter										
	f_{in} < 10 Gb/s		TBD			TBD			TBD		
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 29)	75		2600	75		2600	75		2600	mV
t_r	Output Rise/Fall Times (20% - 80%)										ps
t_f	@ 1 GHz										
	(V_{CTRL} = V_{CC} - 2 V) Q, $\overline{Q}$	30	45	55	30	45	55	30	45	55	
	(V_{CTRL} = V_{CC} - 1 V) Q, $\overline{Q}$	30	40	50	30	40	50	30	40	50	

27. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V. Input edge rates 40 ps (20% - 80%).
28. t_{SKEW} = $|t_{PLH}-t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 10.
29. $V_{INPP(MAX)}$ cannot exceed V_{CC} - V_{EE} (applicable only when V_{CC} - V_{EE} < 2600 mV).
30. Conditions include input amplitude of 500 mV and V_{CTRL} = V_{CC} - 2 V. Minimum output amplitude guarantee of 100 mV (see Output P-P Spec in Figure 8).

Table 11. AC CHARACTERISTICS for QFN-16 V_{CC} = 0 V; -3.0 V < V_{EE} ≤ -2.375 V or 2.375 V ≤ V_{CC} < 3.0 V; V_{EE} = 0 V

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 9) (Note 31)	10 (Note 34)	12		10 (Note 34)	12		10 (Note 34)	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	(V_{CTRL} = V_{CC} - 2 V) D → Q, $\overline{Q}$	100	140	180	100	140	180	80	140	180	
	(V_{CTRL} = V_{CC} - 1 V) D → Q, $\overline{Q}$	100	135	180	100	135	180	100	135	220	
t_{SKEW}	Duty Cycle Skew (Note 32)		3	20		3	15		3	10	ps
t_{JITTER}	RMS Random Clock Jitter										ps
	f_{in} < 10 GHz		0.5	3		0.5	3		0.5	3	
	Peak-to-Peak Data Dependent Jitter										
	f_{in} < 10 Gb/s		TBD			TBD			TBD		
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 33)	75		2600	75		2600	75		2600	mV
t_r	Output Rise/Fall Times (20% - 80%)										ps
t_f	@ 1 GHz										
	(V_{CTRL} = V_{CC} - 2 V) Q, $\overline{Q}$	25	50	70	25	50	70	25	50	70	
	(V_{CTRL} = V_{CC} - 1 V) Q, $\overline{Q}$	22	45	60	22	45	60	22	45	60	

31. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V. Input edge rates 40 ps (20% - 80%).
32. t_{SKEW} = $|t_{PLH}-t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 10.
33. $V_{INPP(MAX)}$ cannot exceed V_{CC} - V_{EE} (applicable only when V_{CC} - V_{EE} < 2600 mV).
34. Conditions include input amplitude of 500 mV and V_{CTRL} = V_{CC} - 2 V. Minimum output amplitude guarantee of 100 mV (see Output P-P Spec in Figure 9).

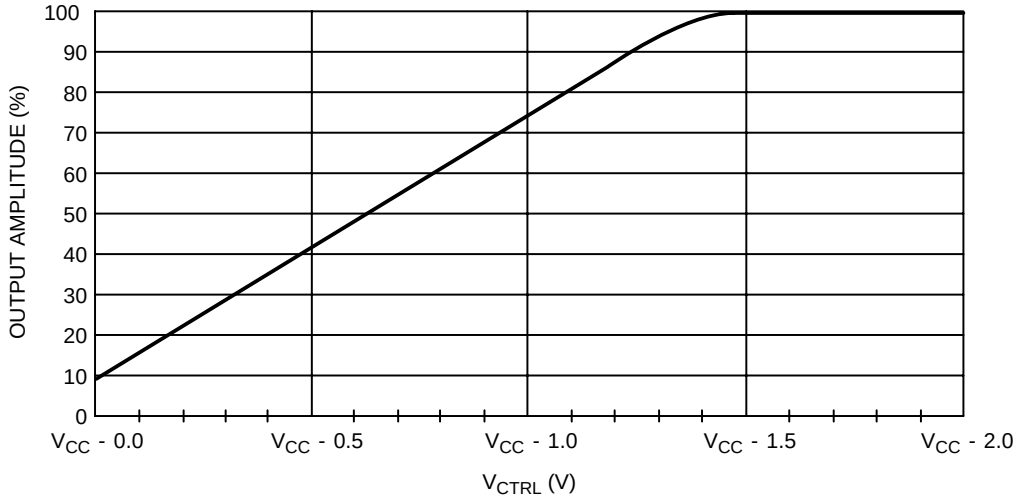


Figure 5. Output Amplitude % vs. V_{CTRL} (pin #A3)

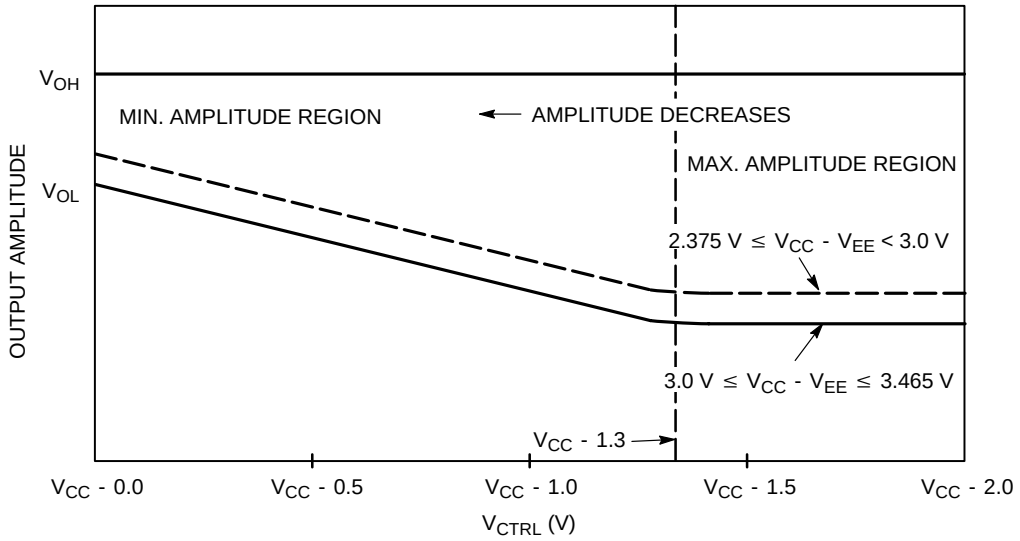


Figure 6. Output Amplitude vs. V_{CTRL} (pin #A3)

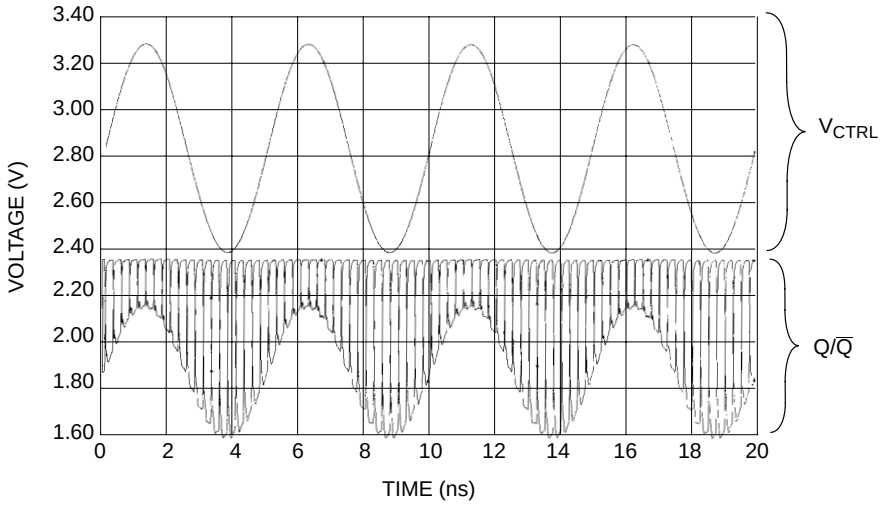


Figure 7. Output Response Under Amplitude Modulation of V_{CTRL} (Conditions Include V_{CC} - V_{EE} = 3.3 V at 25°C, f_{IN} (V_{CTRL}) = 200 MHz, and f_{IN} (D, $\overline{D}$) = 2 GHz)

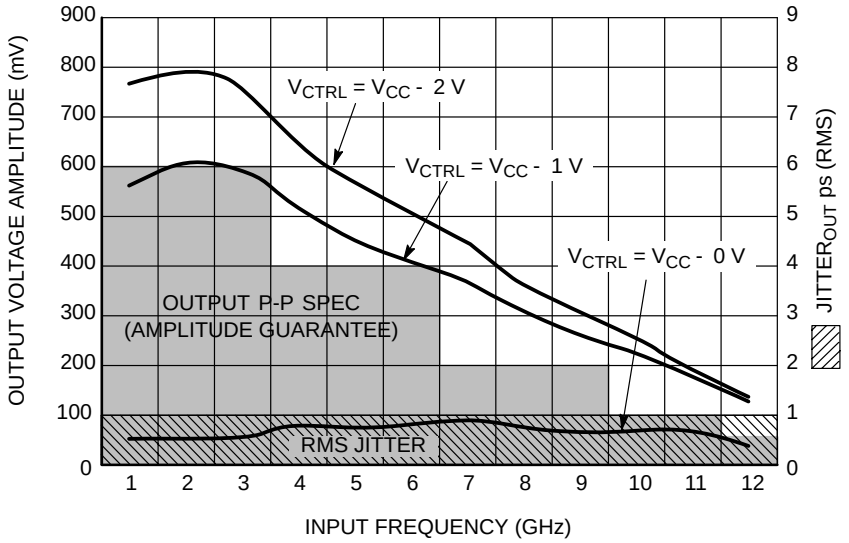


Figure 8. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

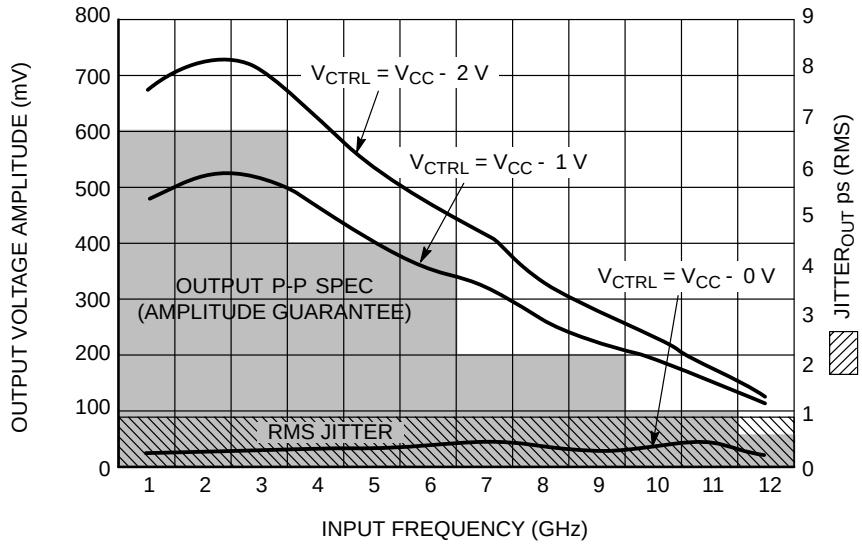


Figure 9. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

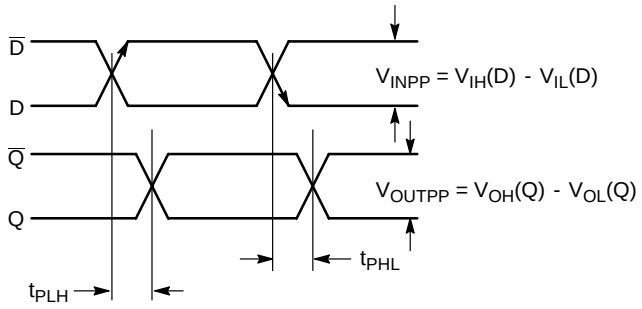


Figure 10. AC Reference Measurement

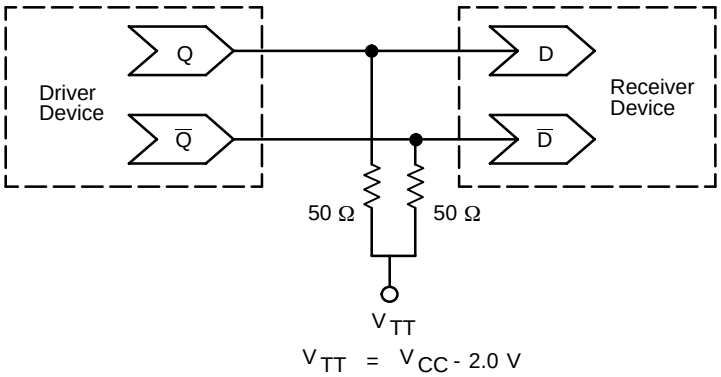
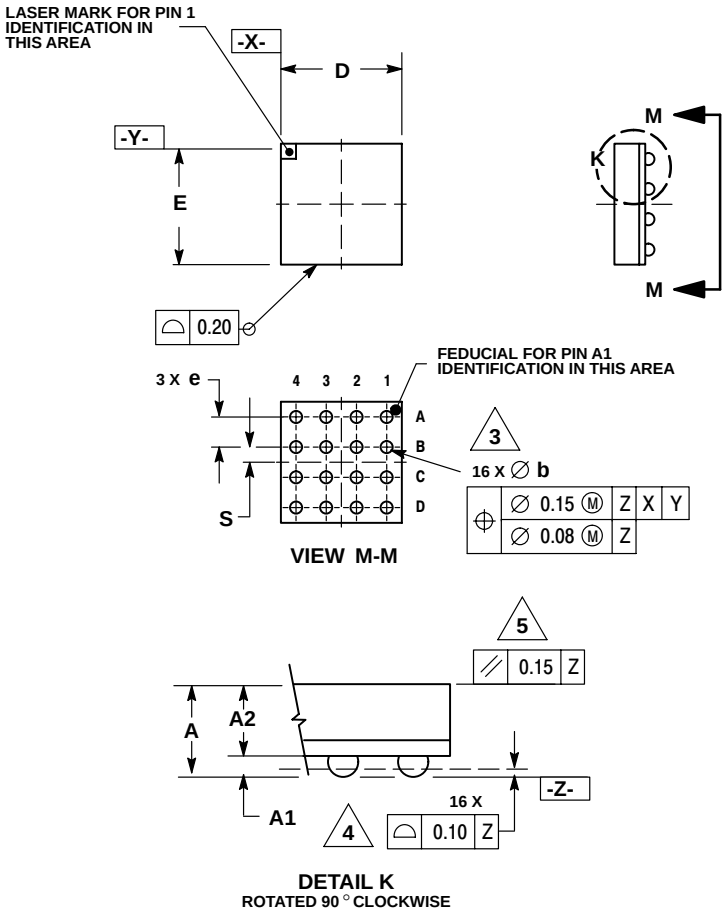


Figure 11. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 - Termination of ECL Logic Devices)

PACKAGE DIMENSIONS

FCBGA-16
BA SUFFIX
PLASTIC 4X4 (mm) BGA FLIP CHIP PACKAGE
CASE 489-01
ISSUE O

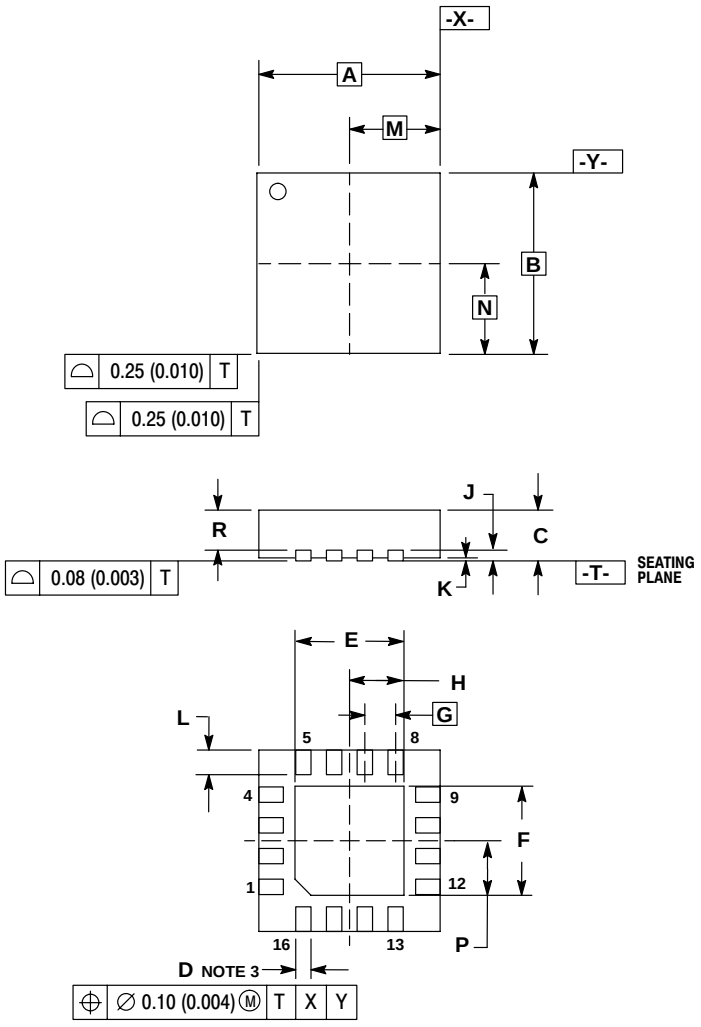


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40 MAX	
A1	0.25	0.35
A2	1.20 REF	
b	0.30	0.50
D	4.00 BSC	
E	4.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

PACKAGE DIMENSIONS

16 PIN QFN
MN SUFFIX
CASE 485G-01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.28	0.009	0.011
E	1.75	1.85	0.069	0.073
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	0.875	0.925	0.034	0.036
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.875	0.925	0.034	0.036
R	0.60	0.80	0.024	0.031

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