NB100LVEP91

2.5V / 3.3V Any Level Positive Input to -2.5V / -3.3V / -5V NECL Output Translator

The NB100LVEP91 is a triple any level positive input to NECL output translator. The device accepts LVPECL, LVTTL, LVCMOS, HSTL, CML or LVDS signals, and translates them to differential NECL output signals (-2.5 V / -3.3 V / -5 V).

To accomplish the level translation the LVEP91 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via 0.01 μF capacitors.

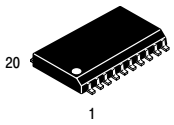
Under open input conditions, the $\overline{D}$ input will be biased at $V_{CC}/2$ and the D input will be pulled to GND. These conditions will force the Q outputs to a low, ensuring stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- Typical Maximum Frequency > 2.0 GHz
- 430 ps Typical Propagation Delay
- Operating Range: V_{CC} = 2.375 V to 3.8 V; V_{EE} = -2.375 V to -5.5 V; GND = 0 V
- Q Output will Default LOW with Inputs Open or at GND

ON Semiconductor®

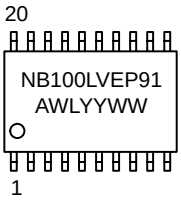
http://onsemi.com

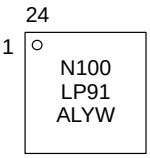


SO-20
DW SUFFIX
CASE 751D

24 PIN QFN
MN SUFFIX
CASE 485L

MARKING DIAGRAM*





A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NB100LVEP91DW	SO-20	38 Units/Rail
NB100LVEP91DWR2	SO-20	1000/Tape & Reel
NB100LVEP91MN	QFN-24	93 Units/Rail
NB100LVEP91MNR2	QFN-24	3000/Tape & Reel

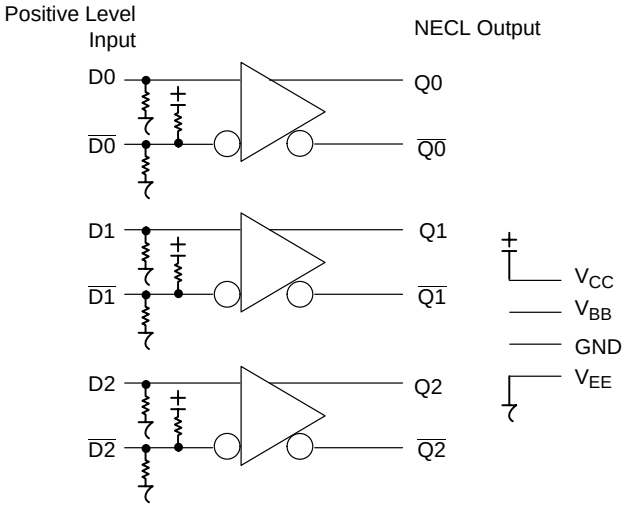
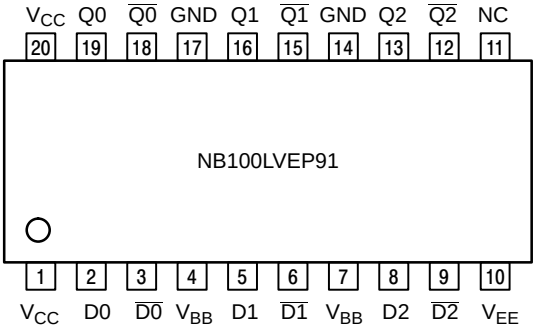


Figure 1. Logic Diagram

PIN DESCRIPTION

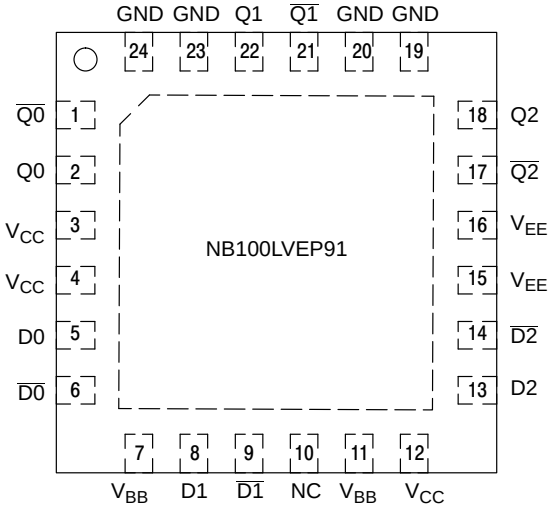
PIN	FUNCTION
Dn*, $\overline{Dn}$**	Any Level Inputs
Qn, $\overline{Qn}$	ECL Outputs
V_{BB}	PECL Reference Voltage Output
V_{CC}	Positive Supply (2.5 V, 3.3 V)
V_{EE}	Negative Supply (-2.5 V, -3.3 V, -5 V)
GND	Ground
NC	No Connect

*Pins will default differentially LOW when left open.
**Pins will default to V_{CC}/2 when left open.



Warning: All V_{CC}, V_{EE}, and GND pins must be externally connected to Power Supply to guarantee proper operation.

Figure 2. SOIC-20 Lead Pinout (Top View)



Warning: All V_{CC}, V_{EE}, and GND pins must be externally connected to Power Supply to guarantee proper operation. The thermally conductive exposed pad on package bottom (see case drawing) must be attached to a heat-sinking conduit.

Figure 3. QFN-24 Lead Pinout (Top View)

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 150 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		446 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Power Supply	GND = 0 V		3.8 to 0	V
V_{EE}	NECL Power Supply	GND = 0 V		-5.5 to 0	V
V_I	PECL Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	3.8 to 0	V
V_{OP}	Operating Voltage	GND = 0 V	V_{CC} - V_{EE}	9.3 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	PECL V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) JESD 51-3 (1S-Single Layer Test Board)	0 lFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient) JESD 51- 6 (2S2P Multilayer Test Board) with Filled Thermal Vias	0 LFPM	24 QFN	47.3	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

LVPECL INPUT DC CHARACTERISTICS V_{CC} = 2.5 V, V_{EE} = -2.375 to -5.5 V, GND = 0 V (Note 3)

		-40 °C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	Power Supply Current	10	14	20	10	14	20	10	14	20	mA
V_{IH}	Input HIGH Voltage	1335		V_{CC}	1335		V_{CC}	1275		V_{CC}	mV
V_{IL}	Input LOW Voltage	GND		875	GND		875	GND		875	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)	0		2.5	0		2.5	0		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

3. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary +1.3 V / -0.125 V.
4. V_{IHCMR} min varies 1:1 with GND. V_{IHCMR} max varies 1:1 with V_{CC}.

LVPECL INPUT DC CHARACTERISTICS V_{CC} = 3.3 V; V_{EE} = -2.375 V to -5.5 V; GND = 0 V (Note 5)

		-40 °C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	V_{CC} Power Supply Current	10	16	24	10	16	24	10	16	24	mA
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		V_{CC}	2135		V_{CC}	2135		V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended)	GND		1675	GND		1675	GND		1675	mV
V_{BB}	Output Voltage Reference (Note 6)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)	0		3.3	0		3.3	0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

5. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary +0.5 / -0.925 V.
6. V_{IHCMR} min varies 1:1 with GND. V_{IHCMR} max varies 1:1 with V_{CC}.

NECL OUTPUT DC CHARACTERISTICS V_{CC} = 2.375 V to 3.8 V; V_{EE} = -2.375 V to -5.5 V; GND = 0 V (Note 7)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	V_{EE} Power Supply Current	40	50	60	38	50	68	38	50	68	mA
V_{OH}	Output HIGH Voltage (Note 8)	-1145	-1020	-895	-1145	1020	-895	-1030	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 8)	-1945	-1725	-1600	-1945	-1725	-1600	-1945	-1725	-1600	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

7. Output parameters vary 1:1 with GND.
8. All loading with 50 Ω resistor to GND-2 volts.

AC CHARACTERISTICS V_{CC} = 2.375 V to 3.8 V; V_{EE} = -2.375 V to -5.5 V; GND = 0 V

Symbol	Characteristic		-40 °C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{opp}	Output Voltage Amplitude (Figure 4)	f_{in} < 1.0 GHz f_{in} < 1.5 GHz	575 525	800 750		600 525	800 750		550 400	800 750		mV
t_{PLH} t_{PHL0}	Propagation Delay D to Q	Differential Single-Ended	375 300	500 450	600 650	375 300	500 450	600 675	400 300	550 500	650 750	ps
t_{SKEW}	Pulse Skew (Note 9) Output-to-Output (Note 10) Part-to-Part (Diff) (Note 10)			15 25 50	75 95 125		15 30 50	75 105 125		15 30 70	80 105 150	ps
t_{JITTER}	RMS Random Clock Jitter (Note 11) Peak-to-Peak Data Dependant Jitter (Note 12)	f_{in} = 2.0 GHz f_{in} = 2.0 Gbps		0.5 20	2.0		0.5 20	2.0		0.5 20	2.0	ps
V_{PP}	Input Voltage Swing (Note 13)		200	800	1200	200	800	1200	200	800	1200	mV
t_r, t_f	Output Rise/Fall Times Q (20% - 80%)		75	150	250	75	150	250	75	150	275	ps

9. Pulse Skew = $|t_{PLH} - t_{PHL}|$
10. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
11. RMS Jitter with 50% Duty Cycle Input Clock Signal.
12. Peak-to-Peak Jitter with input NRZ PRBS 2^{31-1} at 2.0 Gbps.
13. Input voltage swing is a single-ended measurement operating in differential mode. The device has a DC gain of ≈ 50.

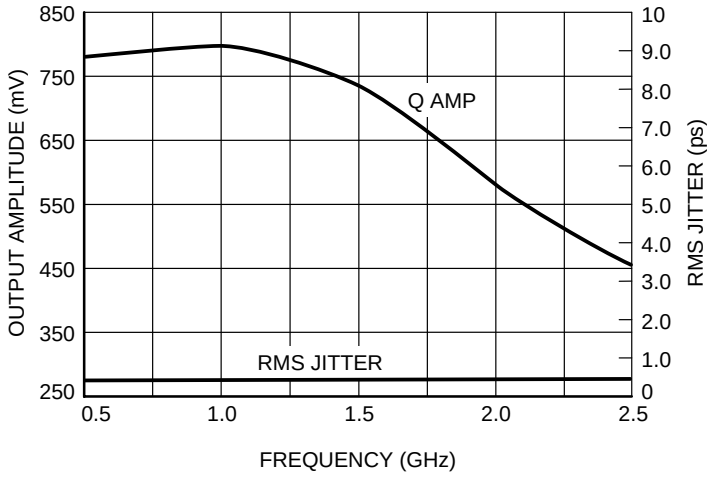


Figure 4.

Application Information

All NB100LVEP91 inputs can accept LVPECL, LVTTL, LVCMOS, HSTL, CML, or LVDS signal levels. The limitations for differential input signal (LVDS, HSTL, LVPECL, or CML) are the minimum input swing of 150 mV and the maximum input swing of 3.0 V. Within these conditions, the input voltage can range from V_{CC} to GND. Examples interfaces are illustrated below in a 50 Ω environment (Z = 50 Ω)

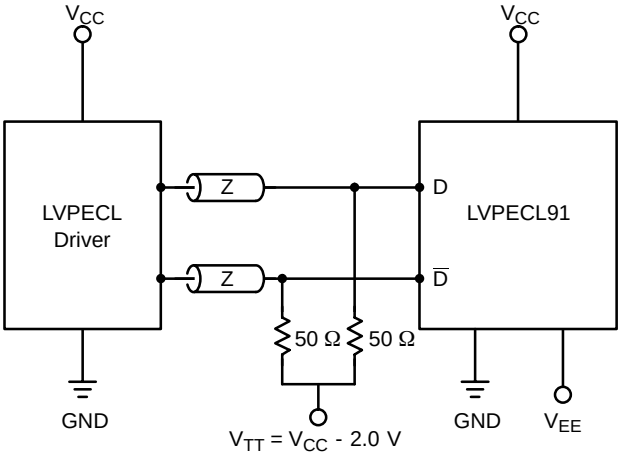


Figure 5. Standard LVPECL Interface

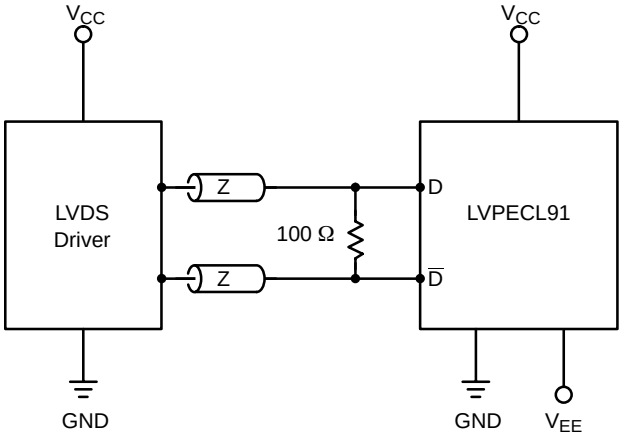


Figure 6. Standard LVDS Interface

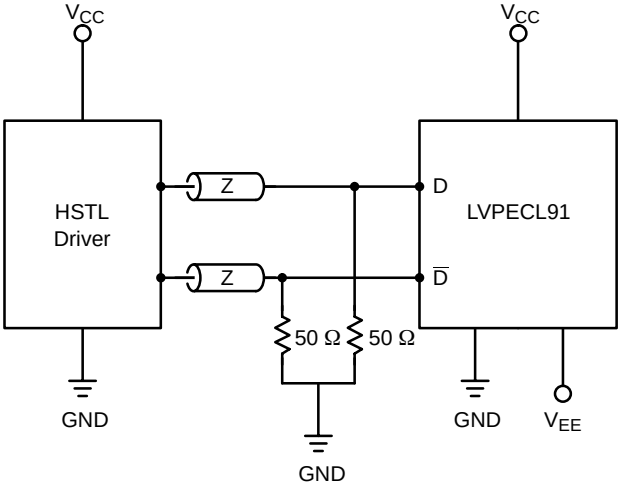


Figure 7. Standard HSTL Interface

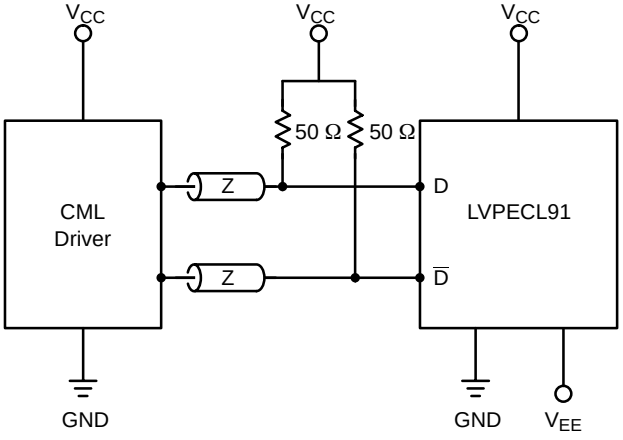


Figure 8. Standard 50 Ω Load CML Interface

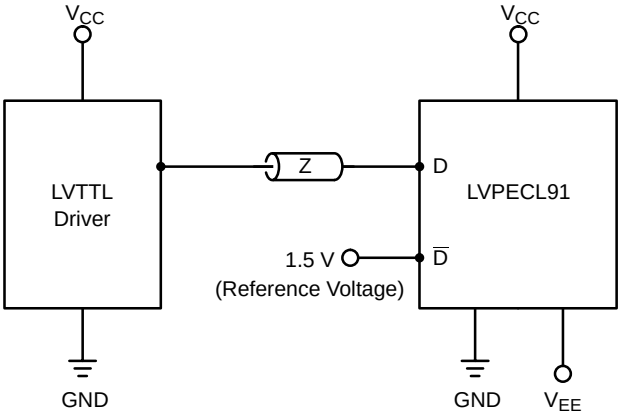


Figure 9. Standard LVTTTL Interface

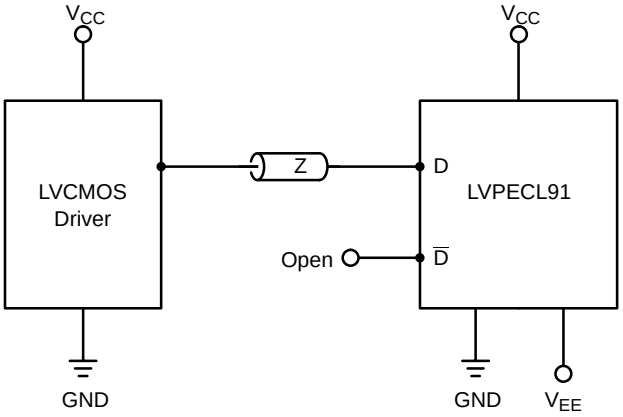


Figure 10. Standard LVCMOS Interface ($\overline{D}$ will default to V_{CC}/2 when left open. A reference voltage of V_{CC}/2 should be applied to D input, if $\overline{D}$ is interfaced to CMOS signals.)

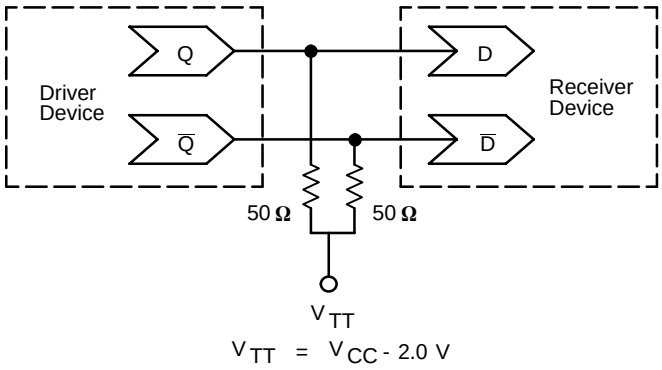


Figure 11. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 - Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 - ECLinPS Circuit Performance at Non-Standard V_{IH} Levels

AN1405 - ECL Clock Distribution Techniques

AN1503 - ECLinPS I/O SPICE Modeling Kit

AN1504 - Metastability and the ECLinPS Family

AN1560 - Low Voltage ECLinPS SPICE Modeling Kit

AN1650 - Using Wire-OR Ties in ECLinPS Designs

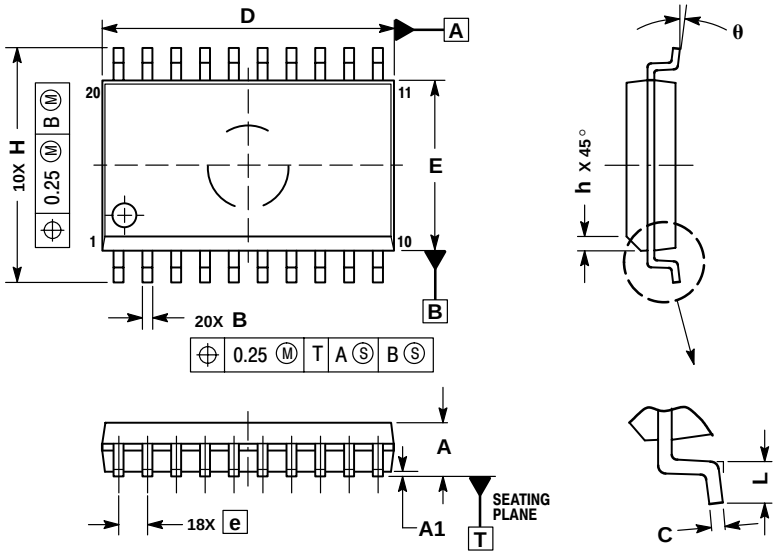
AN1672 - The ECL Translator Guide

AND8002 - Marking and Date Codes

AND8020 - Termination of ECL Logic Devices

PACKAGE DIMENSIONS

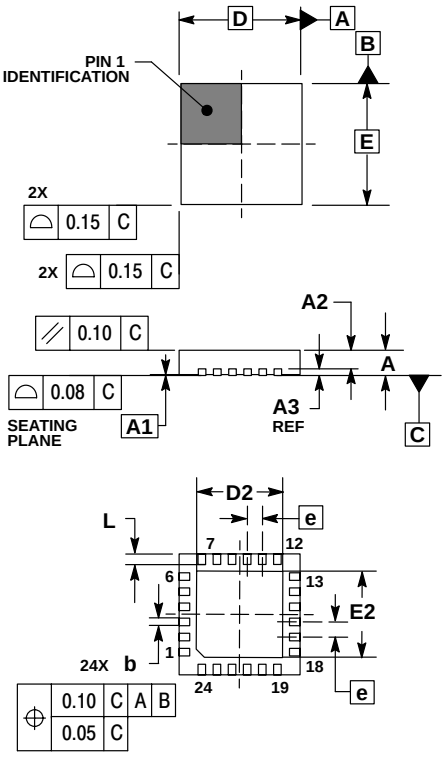
SO-20
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

QFN 24
MN SUFFIX
24 PIN QFN, 4x4
CASE 485L-01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.23	0.28
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.35	0.45

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.