

# Quad TTL/NMOS to PECL\* Translator

The MC10H351 is a quad translator for interfacing data between a saturated logic section and the PECL section of digital systems when only a +5.0 Vdc power supply is available. The MC10H351 has TTL/NMOS compatible inputs and PECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state ( $\approx +3.2$  V) and all inverting outputs to the PECL high logic state ( $\approx +4.1$  V).

The MC10H351 can also be used with the MC10H350 to transmit and receive TTL/NMOS information differentially via balanced twisted pair lines.

- Single +5.0 Power Supply
- All V<sub>CC</sub> Pins Isolated On Chip
- Differentially Drive Balanced Lines
- t<sub>pd</sub> = 1.3 nsec Typical

## MAXIMUM RATINGS

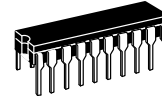
Characteristic	Symbol	Rating	Unit
Power Supply	V <sub>CC</sub>	0 to +7.0	Vdc
Input Voltage (V <sub>CC</sub> = 5.0 V)	V <sub>I</sub>	0 to V <sub>CC</sub>	Vdc
Output Current— Continuous — Surge	I <sub>out</sub>	50 100	mA
Operating Temperature Range	T <sub>A</sub>	0 to +75	°C
Storage Temperature Range— Plastic — Ceramic	T <sub>stg</sub>	-55 to +150 -55 to +165	°C

## ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = V<sub>CC1</sub> = V<sub>CC2</sub> = 5.0 V ± 5.0%)

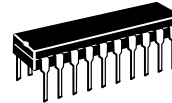
Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	ECL	—	50	—	45	—	50	mA
	TTL	—	20	—	15	—	20	mA
Reverse Current Pins 7, 8, 12, 14 Pin 9	I <sub>R</sub>	—	25	—	20	—	25	μA
	I <sub>INH</sub>	—	100	—	80	—	100	
Forward Current Pins 7, 8, 12, 14 Pin 9	I <sub>F</sub>	—	-0.8	—	-0.6	—	-0.8	mA
	I <sub>INL</sub>	—	-3.2	—	-2.4	—	-3.2	
Input Breakdown Voltage	V <sub>(BR)in</sub>	5.5	—	5.5	—	5.5	—	Vdc
Input Clamp Voltage (I <sub>in</sub> = -18 mA)	V <sub>I</sub>	—	-1.5	—	-1.5	—	-1.5	Vdc
High Output Voltage (1)	V <sub>OH</sub>	3.98	4.16	4.02	4.19	4.08	4.27	Vdc
Low Output Voltage (1)	V <sub>OL</sub>	3.05	3.37	3.05	3.37	3.05	3.37	Vdc
High Input Voltage	V <sub>IH</sub>	2.0	—	2.0	—	2.0	—	Vdc
Low Input Voltage	V <sub>IL</sub>	—	0.8	—	0.8	—	0.8	Vdc

(1) With V<sub>CC</sub> at 5.0 V. V<sub>OH</sub>/V<sub>OL</sub> change 1:1 with V<sub>CC</sub>.  
\*Positive Emitter Coupled Logic

## MC10H351



**L SUFFIX**  
CERAMIC PACKAGE  
CASE 732-03

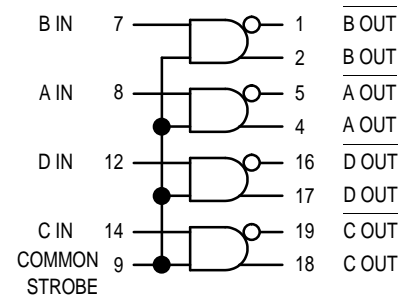


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 738-03



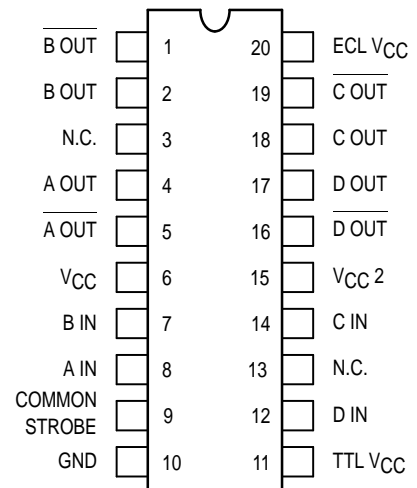
**FN SUFFIX**  
PLCC  
CASE 775-02

## LOGIC DIAGRAM



V<sub>CC</sub> (+5.0 VDC) = PINS 6, 11, 15, 20  
GND = PIN 10

## DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.  
For PLCC pin assignment, see the Pin Conversion Tables on page 6-36 of the Motorola MECL Data Book (DL122/D).



**AC PARAMETERS**

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Propagation Delay (1)	$t_{pd}$	0.4	2.2	0.4	2.2	0.4	2.1	ns
Rise Time (20% to 80%)	$t_r$	0.4	1.9	0.4	2.0	0.4	2.1	ns
Fall Time (80% to 20%)	$t_f$	0.4	1.9	0.4	2.0	0.4	2.1	ns
Maximum Operating Frequency	$f_{max}$	150	—	150	—	150	—	MHz

(1) Propagation delay is measured on this circuit from +1.5 volts on the input waveform to the 50% point on the output waveform.

**NOTE:**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to  $V_{CC} - 2.0$  Vdc.

OUTLINE DIMENSIONS

FN SUFFIX  
 PLASTIC PLCC PACKAGE  
 CASE 775-02  
 ISSUE C

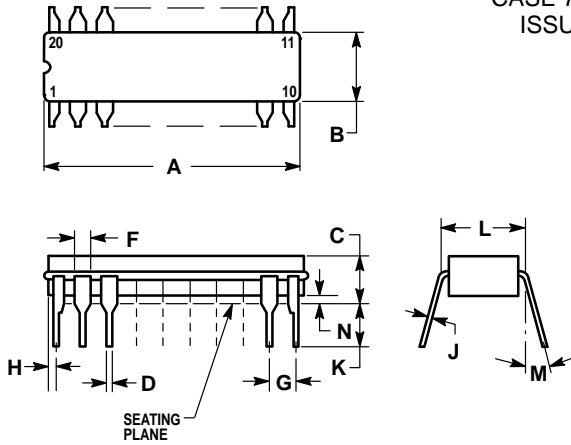


- NOTES:
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
  - DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
  - DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
  - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.
  - THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
  - DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

OUTLINE DIMENSIONS

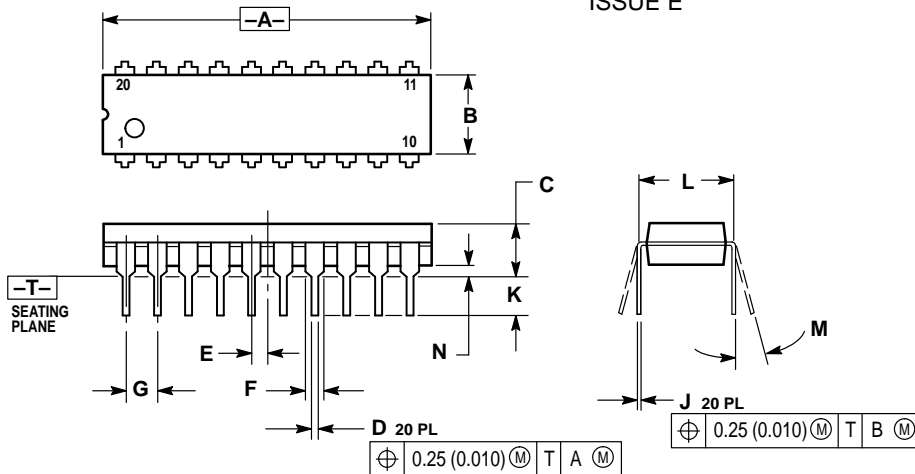
**L SUFFIX**  
**CERAMIC DIP PACKAGE**  
 CASE 732-03  
 ISSUE E



- NOTES:
- LEADS WITHIN 0.010 DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
  - DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - DIMENSIONS A AND B INCLUDE MENISCUS.

DIM	INCHES	
	MIN	MAX
A	0.940	0.990
B	0.260	0.295
C	0.150	0.200
D	0.015	0.022
F	0.055	0.065
G	0.100 BSC	
H	0.020	0.050
J	0.008	0.012
K	0.125	0.160
L	0.300 BSC	
M	0° 15°	
N	0.010	0.040

**P SUFFIX**  
**PLASTIC DIP PACKAGE**  
 CASE 738-03  
 ISSUE E



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.
  - DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  - DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0° 15°		0° 15°	
N	0.020	0.040	0.51	1.01

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