# MC10E416, MC100E416

# 5V ECL Quint Differential Line Receiver

The MC10E416/100E416 is a 5-bit differential line receiving device. The 2.0 GHz of bandwidth provided by the high frequency outputs makes the device ideal for buffering of very high speed oscillators.

The design incorporates two stages of gain, internal to the device, making it an excellent choice for use in high bandwidth amplifier applications.

The differential inputs have internal clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5 V below $V_{CC}$.

The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

The 100 Series contains temperature compensation.

- Differential D and Q; $V_{BB}$ available
- 600 ps Max. Propagation Delay
- High Frequency Outputs
- 2 Stages of Gain
- PECL Mode Operating Range: $V_{CC}$= 4.2 V to 5.7 V with $V_{EE}$= 0 V
- NECL Mode Operating Range: $V_{CC}$= 0 V with $V_{EE}$= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 201 devices

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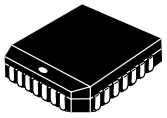
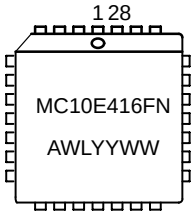
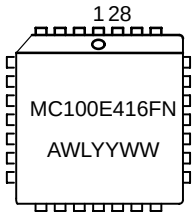


**PLCC–28**
**FN SUFFIX**
**CASE 776**

**MARKING DIAGRAMS**



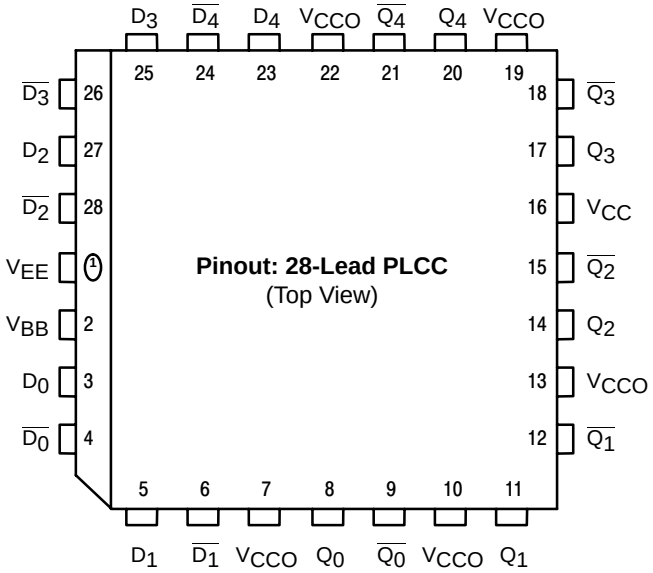




A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MC10E416FN | PLCC–28 | 37 Units/Rail |
| MC10E416FNR2 | PLCC–28 | 500 Units/Reel |
| MC100E416FN | PLCC–28 | 37 Units/Rail |
| MC100E416FNR2 | PLCC–28 | 500 Units/Reel |

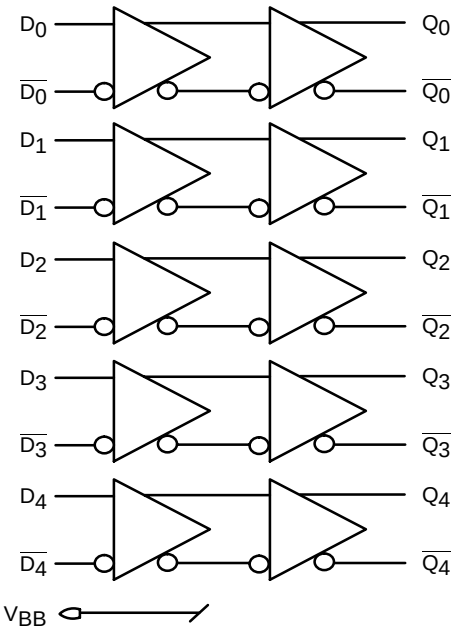
## LOGIC DIAGRAM AND PINOUT ASSIGNMENT




* All $V_{CC}$ and $V_{CCO}$ pins are tied together on the die.

Warning: All $V_{CC}$, $V_{CCO}$, and $V_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation.

## LOGIC DIAGRAM




## PIN DESCRIPTION

| PIN | FUNCTION |
|---|---|
| D[0:4], $\overline{D}$[0:4] | ECL Differential Data Inputs |
| Q[0:4], $\overline{Q}$[0:4] | ECL Differential Data Outputs |
| $V_{BB}$ | Reference Voltage Output |
| $V_{CC}$, $V_{CCO}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |

**MAXIMUM RATINGS** (Note 1)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 8 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | –8 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6<br>–6 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ± 0.5 | mA |
| TA | Operating Temperature Range | | | 0 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | –65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction to Ambient) | 0 LFPM<br>500 LFPM | 28 PLCC<br>28 PLCC | 63.5<br>43.5 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction to Case) | std bd | 28 PLCC | 22 to 26 | °C/W |
| $V_{EE}$ | PECL Operating Range<br>NECL Operating Range | | | 4.2 to 5.7<br>–5.7 to –4.2 | V<br>V |
| $T_{sol}$ | Wave Solder | <2 to 3 sec @ 248°C | | 265 | °C |

1. Maximum Ratings are those values beyond which device damage may occur.

**10E SERIES PECL DC CHARACTERISTICS** $V_{CCx}$= 5.0 V; $V_{EE}$= 0.0 V (Note 1)

| | | 0°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
| $I_{EE}$ | Power Supply Current | | 135 | 162 | | 135 | 162 | | 135 | 162 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 3980 | 4070 | 4160 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 3050 | 3210 | 3370 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single Ended) | 3830 | 3995 | 4160 | 3870 | 4030 | 4190 | 3940 | 4110 | 4280 | mV |
| $V_{IL}$ | Input LOW Voltage (Single Ended) | 3050 | 3285 | 3520 | 3050 | 3285 | 3520 | 3050 | 3302 | 3555 | mV |
| $V_{BB}$ | Output Voltage Reference | 3.62 | | 3.73 | 3.65 | | 3.75 | 3.69 | | 3.81 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3) | 2.7 | | 5.0 | 2.7 | | 5.0 | 2.7 | | 5.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.3 | 0.2 | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}$–2 volts.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, max varies 1:1 with $V_{CC}$.

**10E SERIES NECL DC CHARACTERISTICS** $V_{CCx}$= 0.0 V; $V_{EE}$= –5.0 V (Note 1)

| | | 0°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
| $I_{EE}$ | Power Supply Current | | 135 | 162 | | 135 | 162 | | 135 | 162 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | –1020 | –930 | –840 | –980 | –895 | –810 | –910 | –815 | –720 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | –1950 | –1790 | –1630 | –1950 | –1790 | –1630 | –1950 | –1773 | –1595 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single Ended) | –1170 | –1005 | –840 | –1130 | –970 | –810 | –1060 | –890 | –720 | mV |
| $V_{IL}$ | Input LOW Voltage (Single Ended) | –1950 | –1715 | –1480 | –1950 | –1715 | –1480 | –1950 | –1698 | –1445 | mV |
| $V_{BB}$ | Output Voltage Reference | –1.38 | | –1.27 | –1.35 | | –1.25 | –1.31 | | –1.19 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3) | –2.3 | | 0.0 | –2.3 | | 0.0 | –2.3 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.065 | | 0.3 | 0.2 | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}$–2 volts.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, max varies 1:1 with $V_{CC}$.

**100E SERIES PECL DC CHARACTERISTICS** $V_{CCx}$= 5.0 V; $V_{EE}$= 0.0 V (Note 1)

| | | 0°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Power Supply Current | | 135 | 162 | | 135 | 162 | | 155 | 186 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 3190 | 3295 | 3380 | 3190 | 3255 | 3380 | 3190 | 3260 | 3380 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single Ended) | 3835 | 4050 | 4120 | 3835 | 4120 | 4120 | 3835 | 4120 | 4120 | mV |
| $V_{IL}$ | Input LOW Voltage (Single Ended) | 3190 | 3300 | 3525 | 3190 | 3525 | 3525 | 3190 | 3525 | 3525 | mV |
| $V_{BB}$ | Output Voltage Reference | 3.62 | | 3.74 | 3.62 | | 3.74 | 3.62 | | 3.74 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3) | 2.7 | | 5.0 | 2.7 | | 5.0 | 2.7 | | 5.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}$–2 volts.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, max varies 1:1 with $V_{CC}$.

**100E SERIES NECL DC CHARACTERISTICS** $V_{CCx}$= 0.0 V; $V_{EE}$= –5.0 V (Note 1)

| | | 0°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Power Supply Current | | 135 | 162 | | 135 | 162 | | 155 | 186 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | –1025 | –950 | –880 | –1025 | –950 | –880 | –1025 | –950 | –880 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | –1810 | –1705 | –1620 | –1810 | –1745 | –1620 | –1810 | –1740 | –1620 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single Ended) | –1165 | –950 | –880 | –1165 | –880 | –880 | –1165 | –880 | –880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single Ended) | –1810 | –1700 | –1475 | –1810 | –1475 | –1475 | –1810 | –1475 | –1475 | mV |
| $V_{BB}$ | Output Voltage Reference | –1.38 | | –1.26 | –1.38 | | –1.26 | –1.38 | | –1.26 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3) | –2.3 | | 0.0 | –2.3 | | 0.0 | –2.3 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}$–2 volts.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, max varies 1:1 with $V_{CC}$.

**AC CHARACTERISTICS** $V_{CCx}$= 5.0 V; $V_{EE}$= 0.0 V or $V_{CCx}$= 0.0 V; $V_{EE}$= –5.0 V (Note 1)

| | | 0°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $f_{MAX}$ | Maximum Toggle Frequency | | TBD | | | > 2.0 | | | TBD | | GHz |
| $t_{PLH}$ | Propagation Delay to Output | | | | | | | | | | ps |
| $t_{PHL}$ | d(Diff) | 250 | 350 | 500 | 250 | 350 | 500 | 250 | 350 | 500 | |
| | D(SE) | 200 | 350 | 550 | 200 | 350 | 550 | 200 | 350 | 550 | |
| $t_{SKEW}$ | Within-Device Skew (Note 1.) | | 50 | | | 50 | | | 50 | | ps |
| $t_{SKEW}$ | Duty Cycle Skew | | | | | | | | | | |
| $t_{JITTER}$ | Cycle–to–Cycle Jitter | | TBD | | | TBD | | | TBD | | ps |
| | $t_{PLH}$-$t_{PHL}$ (Note 2.) | | ±10 | | | ±10 | | | ±10 | | ps |
| $V_{PP}$(AC) | Minimum Input Swing (Note 3.) | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| $t_r$ | Rise/Fall Time | | | | | | | | | | |
| $t_f$ | (20 - 80%) | 100 | 200 | 350 | 100 | 200 | 350 | 100 | 200 | 350 | ps |

1. 10 Series: $V_{EE}$ can vary +0.46 V / –0.06 V.
   100 Series: $V_{EE}$ can vary +0.46 V / –0.8 V.
1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Duty cycle skew defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
3. Minimum input swing for which AC parameters are guaranteed.

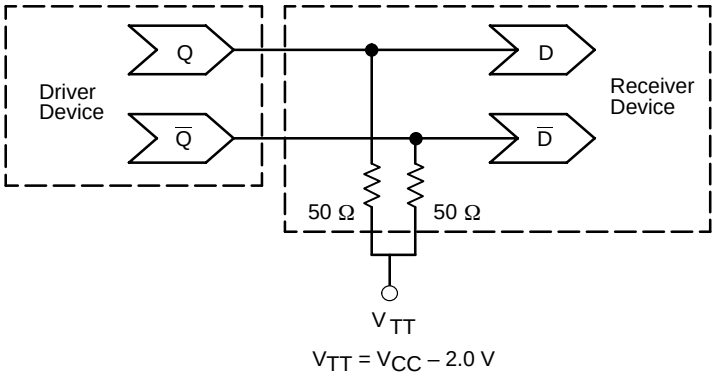


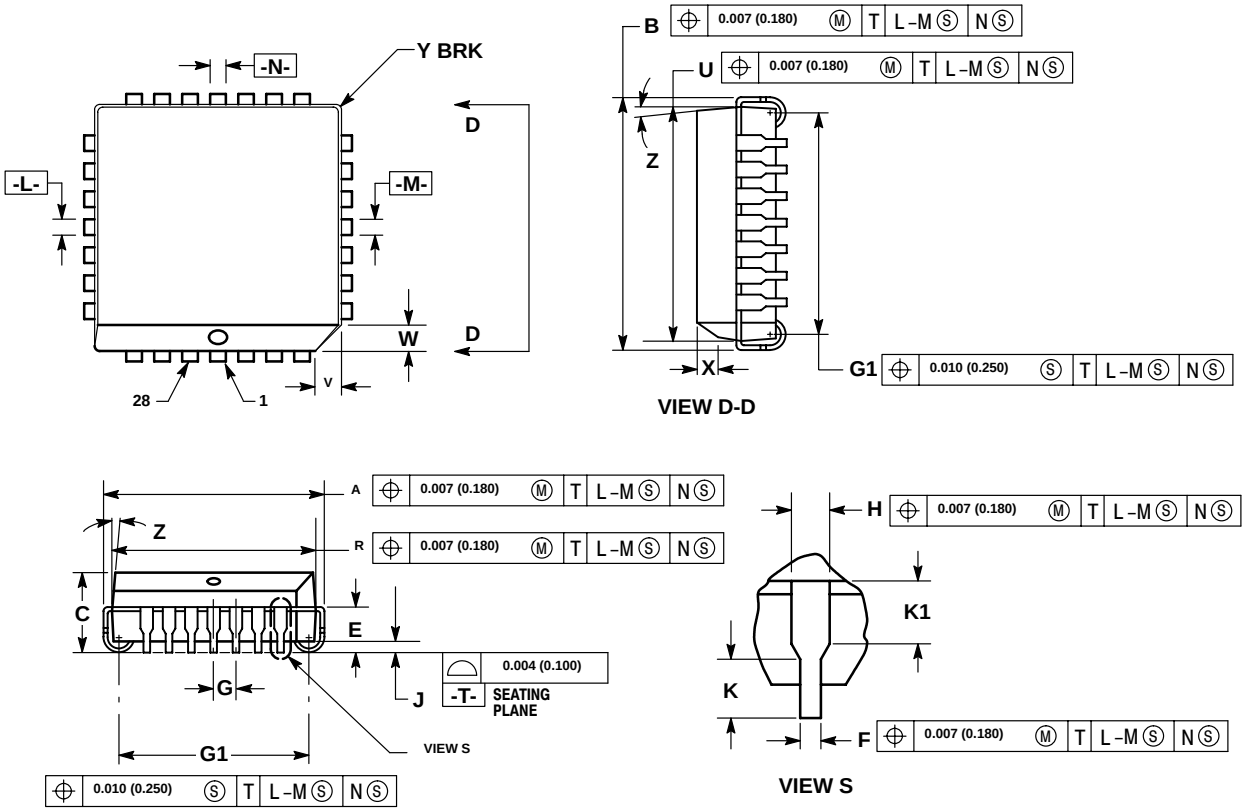

**Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)**

## Resource Reference of Application Notes

| | | |
|---|---|---|
| **AN1404** | – | ECLinPS Circuit Performance at Non–Standard $V_{IH}$ Levels |
| **AN1405** | – | ECL Clock Distribution Techniques |
| **AN1406** | – | Designing with PECL (ECL at +5.0 V) |
| **AN1503** | – | ECLinPS I/O SPICE Modeling Kit |
| **AN1504** | – | Metastability and the ECLinPS Family |
| **AN1568** | – | Interfacing Between LVDS and ECL |
| **AN1596** | – | ECLinPS Lite Translator ELT Family SPICE I/O Model Kit |
| **AN1650** | – | Using Wire–OR Ties in ECLinPS Designs |
| **AN1672** | – | The ECL Translator Guide |
| **AND8001** | – | Odd Number Counters Design |
| **AND8002** | – | Marking and Date Codes |
| **AND8020** | – | Termination of ECL Logic Devices |

## PACKAGE DIMENSIONS

**PLCC–28**
**FN SUFFIX**
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE E




NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | — | 0.51 | — |
| K | 0.025 | — | 0.64 | — |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | — | 0.020 | — | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | — | 1.02 | — |

# Notes

## PUBLICATION ORDERING INFORMATION

**Literature Fulfillment**:
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