

# MC10E154, MC100E154

## 5V ECL 5-Bit 2:1 Mux-Latch

The MC10E/100E154 contains five 2:1 multiplexers followed by transparent latches with differential outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent, and output data is controlled by the multiplexer select control, SEL. A logic HIGH on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

The 100 series contains temperature compensation.

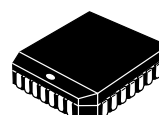
- 850 ps Max. LEN to Output
- 825 ps Max. D to Output
- Differential Outputs
- Asynchronous Master Reset
- Dual Latch-Enables
- PECL Mode Operating Range:  $V_{CC} = 4.2\text{ V}$  to  $5.7\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -4.2\text{ V}$  to  $-5.7\text{ V}$
- Internal Input Pulldown Resistors
- ESD Protection:  $> 2\text{ KV HBM}$ ,  $> 200\text{ V MM}$
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
- For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 237 devices



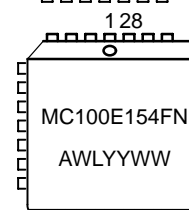
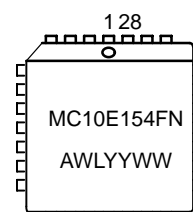
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### MARKING DIAGRAMS



**PLCC-28  
FN SUFFIX  
CASE 776**



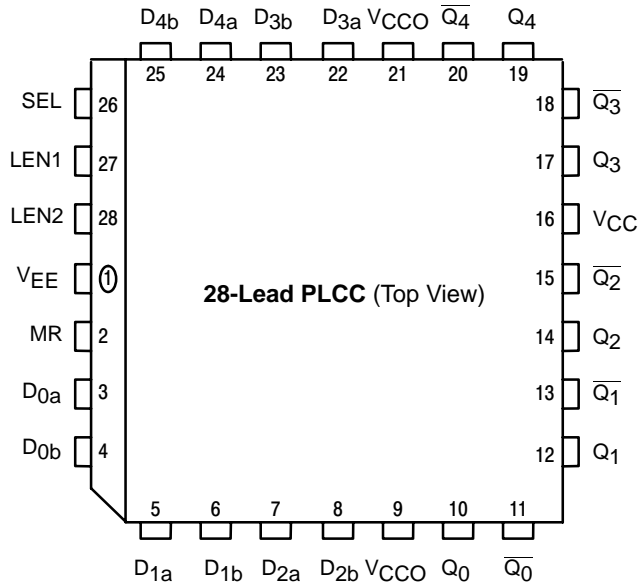
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC10E154FN	PLCC-28	37 Units/Rail
MC10E154FNR2	PLCC-28	500 Units/Reel
MC100E154FN	PLCC-28	37 Units/Rail
MC100E154FNR2	PLCC-28	500 Units/Reel

# MC10E154, MC100E154

## LOGIC DIAGRAM AND PINOUT ASSIGNMENT



\* All VCC and VCCO pins are tied together on the die.

Warning: All VCC, VCCO, and VEE pins must be externally connected to Power Supply to guarantee proper operation.

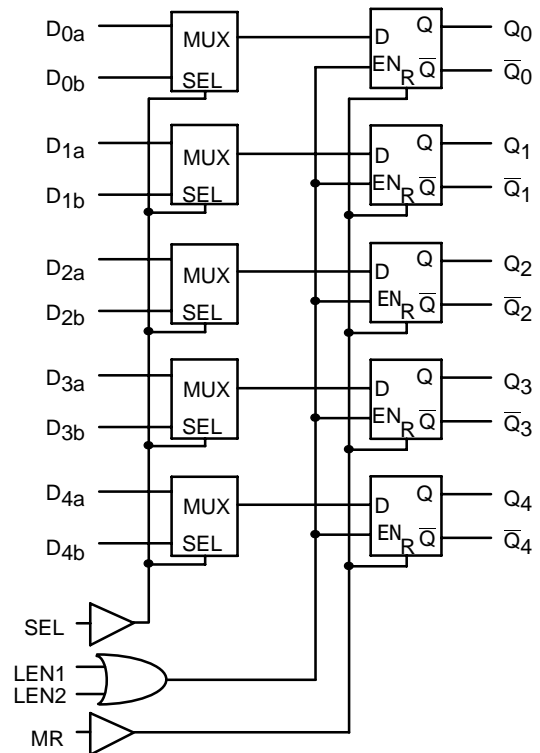
### PIN DESCRIPTION

PIN	FUNCTION
D0a – D4a	ECL Input Data a
D0b – D4b	ECL Input Data b
SEL	ECL Data Select Input
LEN1, LEN2	ECL Latch Enables
MR	ECL Master Reset
Q0– Q4, $\overline{Q_0} - \overline{Q_4}$	ECL Differential Outputs
VCC, VCCO	Positive Supply
VEE	Negative Supply

### TRUTH TABLE

SEL	Data
H	a
L	b

### LOGIC DIAGRAM



# MC10E154, MC100E154

## MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		8	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		−8	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 −6	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
T <sub>A</sub>	Operating Temperature Range			0 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			−65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V <sub>EE</sub>	PECL Operating Range NECL Operating Range			4.2 to 5.7 −5.7 to −4.2	V V
T <sub>sol</sub>	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

## 10E SERIES PECL DC CHARACTERISTICS V<sub>CCx</sub> = 5.0 V; V<sub>EE</sub> = 0.0 V (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		76	91		76	91		76	91	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V <sub>IH</sub>	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V <sub>IL</sub>	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.46 V / −0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V<sub>CC</sub>−2 volts.

## 10E SERIES NECL DC CHARACTERISTICS V<sub>CCx</sub> = 0.0 V; V<sub>EE</sub> = −5.0 V (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		76	91		76	91		76	91	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)	−1020	−930	−840	−980	−895	−810	−910	−815	−720	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)	−1950	−1790	−1630	−1950	−1790	−1630	−1950	−1773	−1595	mV
V <sub>IH</sub>	Input HIGH Voltage	−1170	−1005	−840	−1130	−970	−810	−1060	−890	−720	mV
V <sub>IL</sub>	Input LOW Voltage	−1950	−1715	−1480	−1950	−1715	−1480	−1950	−1698	−1445	mV
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.46 V / −0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V<sub>CC</sub>−2 volts.

# MC10E154, MC100E154

## 100E SERIES PECL DC CHARACTERISTICS $V_{CCx}=5.0\text{ V}$ ; $V_{EE}=0.0\text{ V}$ (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		76	91		76	91		87	105	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
$V_{OL}$	Output LOW Voltage (Note 2)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
$V_{IH}$	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
$V_{IL}$	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.46 V / -0.8 V.

2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}$ -2 volts.

## 100E SERIES NECL DC CHARACTERISTICS $V_{CCx}=0.0\text{ V}$ ; $V_{EE}=-5.0\text{ V}$ (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		76	91		76	91		87	105	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
$V_{IH}$	Input HIGH Voltage	-1165	-950	-880	-1165	-880	-880	-1165	-880	-880	mV
$V_{IL}$	Input LOW Voltage	-1810	-1700	-1475	-1810	-1475	-1475	-1810	-1475	-1475	mV
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.46 V / -0.8 V.

2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}$ -2 volts.

## AC CHARACTERISTICS $V_{CCx}=5.0\text{ V}$ ; $V_{EE}=0.0\text{ V}$ or $V_{CCx}=0.0\text{ V}$ ; $V_{EE}=-5.0\text{ V}$ (Note 1.)

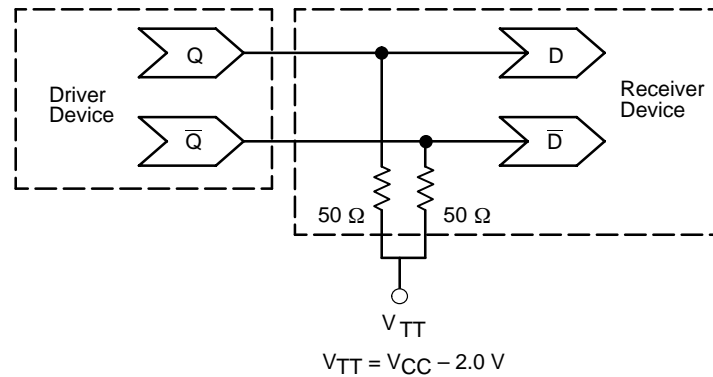
Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output D SEL LEN MR	325 475 350 450	500 650 500 600	700 925 750 800	325 475 350 450	500 650 500 600	700 925 750 800	325 475 350 450	500 650 500 600	700 925 750 800	ps
$t_s$	Setup Time D SEL	300 500	100 250		300 500	100 250		300 500	100 250		ps
$t_h$	Hold Time D SEL	300 200	-100 -250		300 200	-100 -250		300 200	-100 -250		ps
$t_{RR}$	Reset Recovery Time	800	600		800	600		800	600		ps
$t_{PW}$	Minimum Pulse Width MR	400			400			400			ps
$t_{SKEW}$	Within-Device Skew (Note 2.)		50			50			50		ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$t_r$ $t_f$	Rise/Fall Times (20 - 80%)	300	475	800	300	475	800	300	475	800	ps

1. 10 Series:  $V_{EE}$  can vary +0.46 V / -0.06 V.

100 Series:  $V_{EE}$  can vary +0.46 V / -0.8 V.

2. Within-device skew is defined as identical transitions on similar paths through a device.

## MC10E154, MC100E154



**Figure 1. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

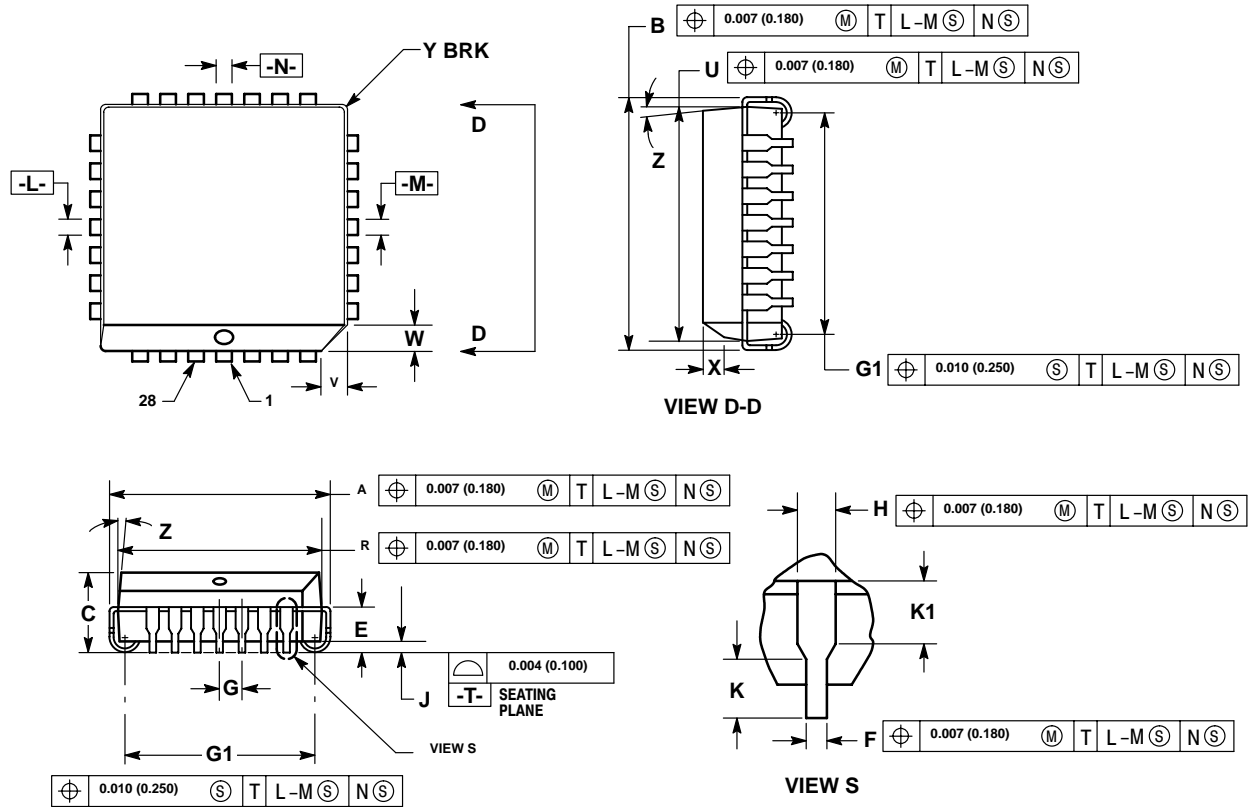
### Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

# MC10E154, MC100E154


## PACKAGE DIMENSIONS

PLCC-28  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 776-02  
ISSUE E



## **Notes**

# MC10E154, MC100E154

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