MC100LVE164

3.3V ECL 16:1 Multiplexer

The MC100LVE164 is a 16:1 multiplexer with a differential output. The select inputs (SEL0, 1, 2, 3) control which one of the sixteen data inputs (A0 – A15) is propragated to the output. The device is functionally equivalent to the MC100E164 except it operates from a 3.3 V supply. The device is packaged in the 32–lead LQFP. The LQFP has a 7x7 mm body with a 0.8 mm lead pitch.

Special attention to the design layout results in a typical skew between the 16 inputs of only 50 ps.

- 850 ps Data Input to Output
- Differential Output
- ESD Protection: >2 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 2
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 307 devices

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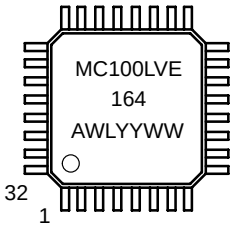
LQFP
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



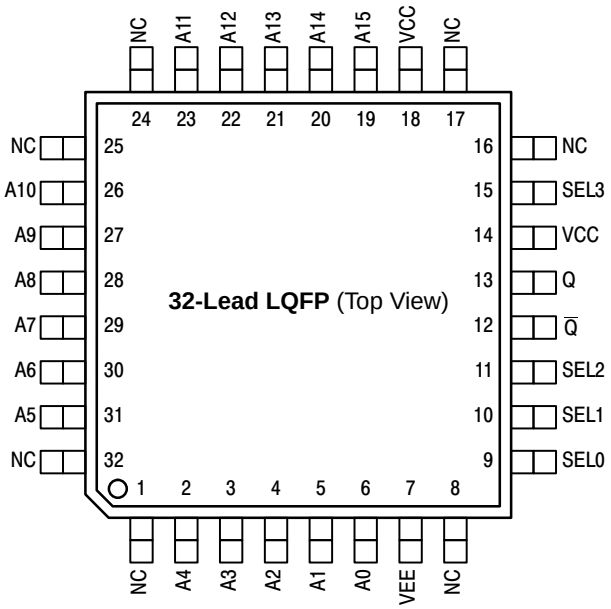
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

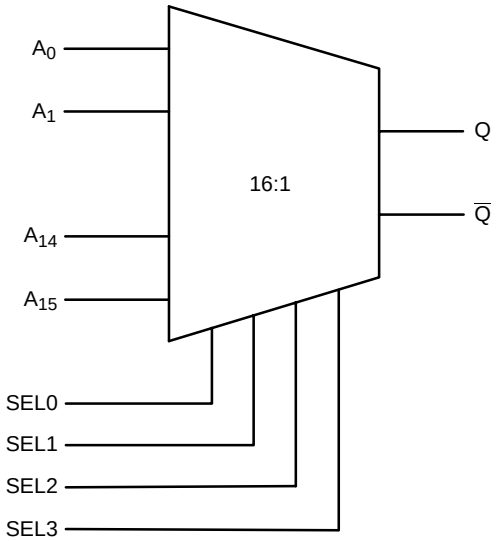
ORDERING INFORMATION

Device	Package	Shipping
MC100LVE164FA	LQFP	250 Units/Tray
MC100LVE164FAR2	LQFP	2000 Tape & Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



LOGIC DIAGRAM



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
$A_0 – A_{15}$	ECL Data Inputs
SEL[0:3]	ECL Select Inputs
Q, $\overline{Q}$	ECL Differential Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

SEL3	SEL2	SEL1	SEL0	Data
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	L	L	L	A8
H	L	L	H	A9
H	L	H	L	A10
H	L	H	H	A11
H	H	L	L	A12
H	H	L	H	A13
H	H	H	L	A14
H	H	H	H	A15

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	32 LQFP	12 to 17	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 2)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		34	45		34	45		37	45	mA
V_{OH}	Output HIGH Voltage (Note 3)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 3)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
3. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 4)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		34	45		34	45		37	45	mA
V_{OH}	Output HIGH Voltage (Note 5)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 5)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

4. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
5. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 6)

Symbol	Characteristic		–40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency			TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	A Input SEL0 SEL1 SEL2 SEL3	350 500 400 400 400	600 700 675 675 550	850 900 900 900 700	350 500 400 400 400	600 700 675 675 550	850 900 900 900 700	350 500 400 400 400	600 700 675 675 550	850 900 900 900 700	ps
t_{SKEW}	Within Device Skew (Note 7)			75			50			50		ps
t_{JITTER}	Cycle–to–Cycle Jitter			TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times (20% – 80%)		275	400	550	275	400	550	275	400	550	ps

6. V_{EE} can vary ±0.3 V.
7. Within Device skew is defined as the difference in the A to Q delay between the 16 different A inputs.

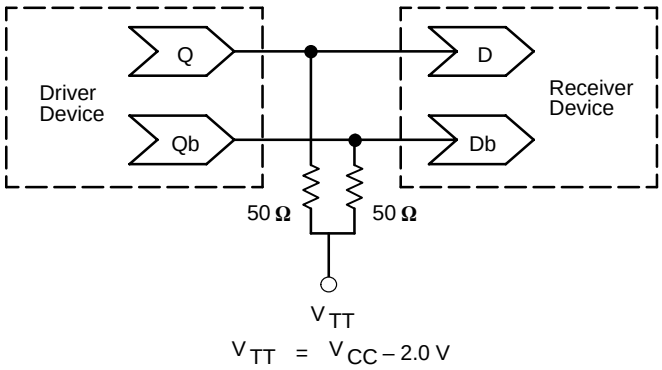


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

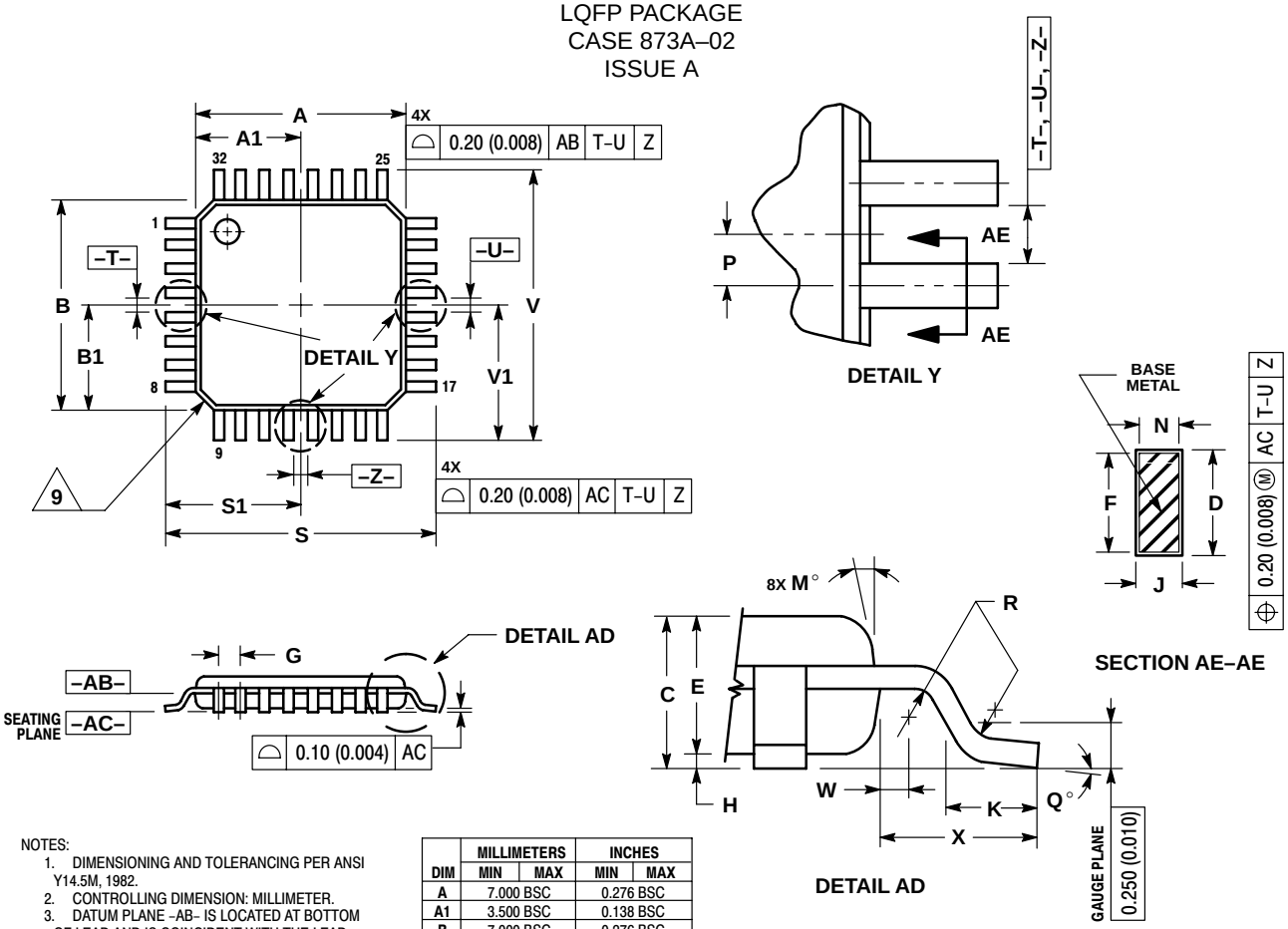
AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

PACKAGE DIMENSIONS

FA SUFFIX
LQFP PACKAGE
CASE 873A–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Notes

Notes

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