MC10ELT28, MC100ELT28

5V TTL to Differential PECL and Differential PECL to TTL Translator

The MC10ELT/100ELT28 is a differential PECL to TTL translator and a TTL to differential PECL translator in a single package. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the dual translation design of the ELT28 makes it ideal for applications which are sending and receiving signals across a backplane.

The 100 Series contains temperature compensation.

- 3.5 ns Typical PECL to TTL Propagation Delay
- 1.2 ns Typical TTL to PECL Propagation Delay
- PNP TTL Inputs for Minimal Loading
- 24 mA TTL Outputs
- Flow Through Pinouts
- ESD Protection: >2 KV HBM
- Operating Range V_{CC}= 4.75 V to 5.25 V with GND= 0 V
- Q_{TTL} Output Will Default High with Inputs Left Open or < 1.3 V
- Q_{ECL} Output Will Default High with Inputs Left Open
- Internal PECL Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in,
  Oxygen Index: 28 to 34
- Transistor Count = 71 devices

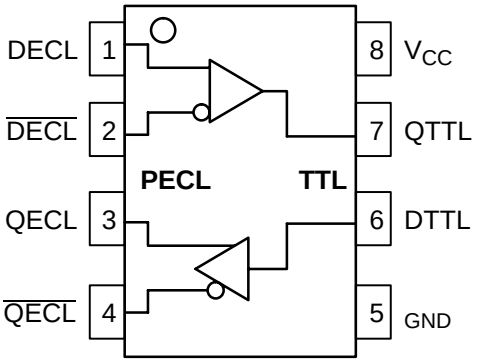

Figure 1. 8-Lead Pinout and Logic Diagram
(Top View)

PIN DESCRIPTION

PIN	FUNCTION
QTTL	TTL Output
DTTL	TTL Inputs
QECL, $\overline{QECL}$	PECL Differential Outputs
DECL, $\overline{DECL}$	PECL Differential Inputs
V_{CC}	Positive Supply
GND	Ground

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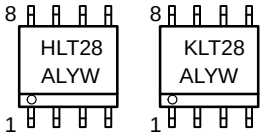
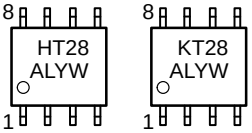
MARKING DIAGRAMS*

SO-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10ELT28D	SO-8	98 Units/Rail
MC10ELT28DR2	SO-8	2500 Tape & Reel
MC100ELT28D	SO-8	98 Units/Rail
MC100ELT28DR2	SO-8	2500 Tape & Reel
MC10ELT28DT	TSSOP-8	98 Units/Rail
MC10ELT28DTR2	TSSOP-8	2500 Tape & Reel
MC100ELT28DT	TSSOP-8	98 Units/Rail
MC100ELT28DTR2	TSSOP-8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		7	V
V_{IN}	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	0 to 6	V
I_{out}	PECL Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10ELT SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 2)

		-40 °C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (Note 3)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 3)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3050		3500	3050		3520	3050		3555	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)	2.2		5.0	2.2		5.0	2.2		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
3. PECL outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.
4. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

100ELT SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 5)

		-40 °C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (Note 6)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 6)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7)	2.2		5.0	2.2		5.0	2.2		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
6. PECL outputs are terminated through a 50 ohm resistor to V_{CC} - 2 volts.
7. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

TTL OUTPUT DC CHARACTERISTICS V_{CC} = 4.75V to 5.25V; T_A = -40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.0 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA			0.5	V
I_{CCH}	Power Supply Current			27	40	mA
I_{CCL}	Power Supply Current			29	42	mA
I_{OS}	Output Short Circuit Current		-150		-60	mA

TTL INPUT DC CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; T_A = -40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V			20	μA
I_{IHH}	Input HIGH Current	V_{IN} = 7.0 V			100	μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V			-0.6	mA
V_{IK}	Input Clamp Diode Voltage	I_{IN} = -18 mA			-1.2	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

AC CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V (Note 8.)

		-40 °C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			100			TBD		MHz
t_{PLH}	Propagation Delay @ 1.5 V DECL to QTTL DTTL to QECL	 2.0 0.6		 5.5 1.2	 2.0 0.9	 1.2	 5.5 1.5	 2.0 0.6		 5.5 1.35	ns
t_{PHL}	Propagation Delay @ 1.5 V DECL to QTTL DTTL to QECL	 2.0 0.4		 5.5 1.0	 2.0 0.5	 0.8	 5.5 1.1	 2.0 0.7		 5.5 1.3	ns
t_r, t_f	Rise/Fall Times (20% - 80%) QECL	0.15		1.5	0.15		1.5	0.15		1.5	ns
V_{PP}	PECL Input Swing (Note 9)	200		1000	200		1000	200		1000	mV
t_r/t_f	Output Rise Time (10-90%) Output Fall Time (10-90%)					1.6 1.1					ns ns

8. R_L = 500 Ω to GND and C_L = 20 pF to GND. Refer to Figure 2.
9. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed.

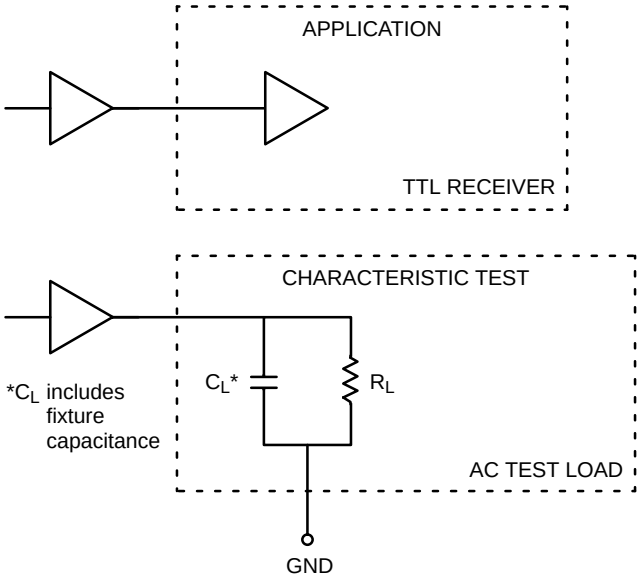


Figure 2. TTL Output Loading Used for Device Evaluation

Resource Reference of Application Notes

AN1404 - ECLinPS Circuit Performance at Non-Standard V_{IH} Levels

AN1405 - ECL Clock Distribution Techniques

AN1406 - Designing with PECL (ECL at +5.0 V)

AN1503 - ECLinPS I/O SPICE Modeling Kit

AN1504 - Metastability and the ECLinPS Family

AN1560 - Low Voltage ECLinPS SPICE Modeling Kit

AN1568 - Interfacing Between LVDS and ECL

AN1596 - ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 - Using Wire-OR Ties in ECLinPS Designs

AN1672 - The ECL Translator Guide

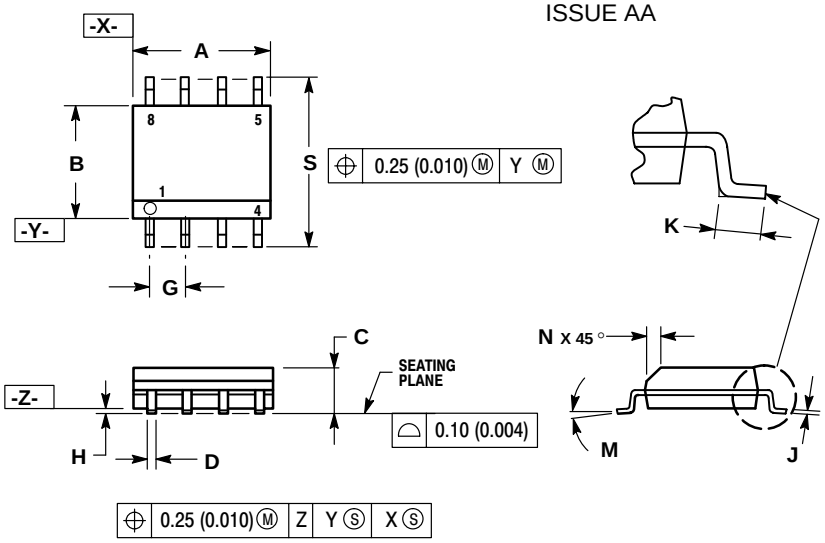
AND8001 - Odd Number Counters Design

AND8002 - Marking and Date Codes

AND8020 - Termination of ECL Logic Devices

PACKAGE DIMENSIONS

SO-8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-07
ISSUE AA

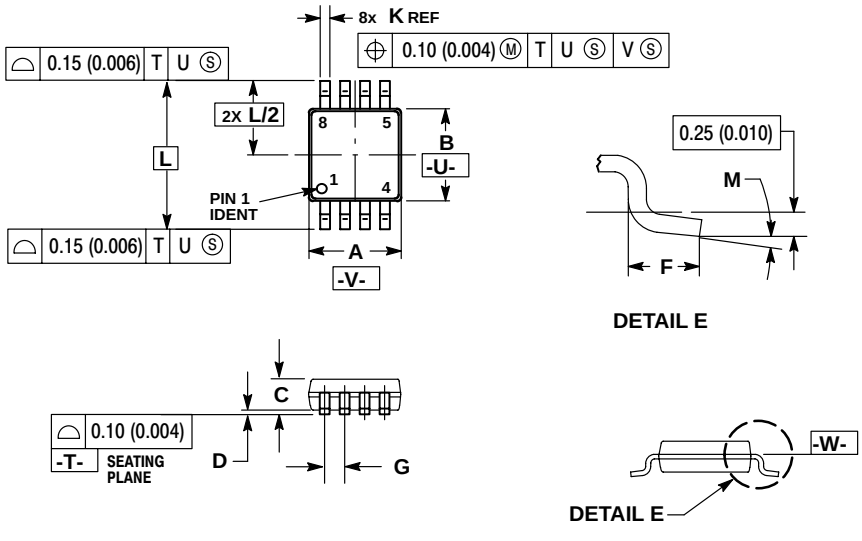


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDAARD IS 751−07

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R-02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

Notes

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