

# MC10ELT21, MC100ELT21

## 5V Differential PECL to TTL Translator

The MC10ELT/100ELT21 is a differential PECL to TTL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the single gate of the ELT21 makes it ideal for those applications where space, performance and low power are at a premium.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The 100 Series contains temperature compensation.

- 3.5 ns Typical Propagation Delay
- 24 mA TTL Output
- Flow Through Pinouts
- ESD Protection: >2 KV HBM
- Operating Range:  $V_{CC}$ = 4.75 V to 5.25 V with GND= 0 V
- Q Output Will Default LOW with Inputs Left Open or < 1.3 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1

For Additional Information, see Application Note AND8003/D

- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 81 devices

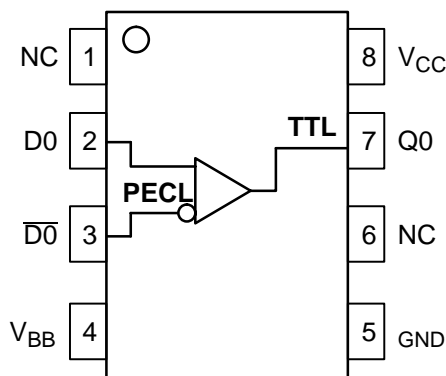


Figure 1. 8-Lead Pinout and Logic Diagram (Top View)

### PIN DESCRIPTION

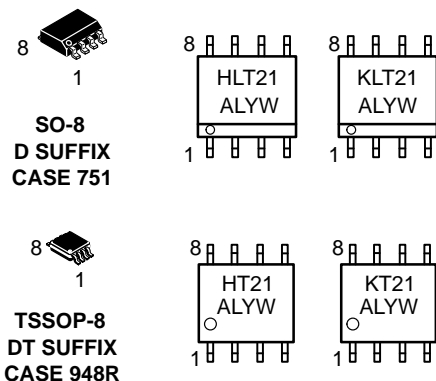
PIN	FUNCTION
Q0	TTL Output
D0, $\overline{D0}$	PECL Differential Inputs
$V_{BB}$	Reference Voltage Output
$V_{CC}$	Positive Supply
GND	Ground
NC	No Connect



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### MARKING DIAGRAMS\*



H = MC10                      L = Wafer Lot  
 K = MC100                    Y = Year  
 A = Assembly Location      W = Work Week

\*For additional information, see Application Note AND8002/D

### ORDERING INFORMATION

Device	Package	Shipping
MC10ELT21D	SO-8	98 Units/Rail
MC10ELT21DR2	SO-8	2500 Tape & Reel
MC100ELT21D	SO-8	98 Units/Rail
MC100ELT21DR2	SO-8	2500 Tape & Reel
MC10ELT21DT	TSSOP-8	98 Units/Rail
MC10ELT21DTR2	TSSOP-8	2500 Tape & Reel
MC100ELT21DT	TSSOP-8	98 Units/Rail
MC100ELT21DTR2	TSSOP-8	2500 Tape & Reel

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## MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	PECL Power Supply	GND = 0 V		7	V
V <sub>IN</sub>	PECL Input Voltage	GND = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	0 to 6	V
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	std bd	8 SOIC	41 to 44	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T <sub>sol</sub>	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

## 10ELT SERIES PECL INPUT DC CHARACTERISTICS V<sub>CC</sub>= 5.0 V; GND= 0.0 V (Note 2)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended)	3770		4110	3870		4190	3930		4265	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	3050		3500	3050		3520	3050		3555	mV
V <sub>BB</sub>	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	2.2		5.0	2.2		5.0	2.2		5.0	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input parameters vary 1:1 with V<sub>CC</sub>. V<sub>CC</sub> can vary ± 0.25 V.

3. V<sub>IHCMR</sub> min varies 1:1 with GND, V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>.

## 100ELT SERIES PECL INPUT DC CHARACTERISTICS V<sub>CC</sub>= 5.0 V; GND= 0.0 V (Note 4)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
V <sub>BB</sub>	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.745	V
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	2.2		5.0	2.2		5.0	2.2		5.0	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

4. Input parameters vary 1:1 with V<sub>CC</sub>. V<sub>CC</sub> can vary ± 0.25 V.

5. V<sub>IHCMR</sub> min varies 1:1 with GND, V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>.

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## TTL OUTPUT DC CHARACTERISTICS $V_{CC}= 4.75\text{ V to }5.25\text{ V}; T_A= -40^\circ\text{C to }85^\circ\text{C}$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.0\text{mA}$	2.4		(Note 6)	V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24\text{mA}$			0.5	V
$I_{CCH}$	Power Supply Current			20	29	mA
$I_{CCL}$	Power Supply Current			22	32	mA
$I_{OS}$	Output Short Circuit Current		-150		-60	mA

6. Max level is  $V_{CC}-0.7$  by design.

## AC CHARACTERISTICS $V_{CC}= 4.75\text{ V to }5.25\text{ V}; GND= 0.0\text{ V}$ (Note 7)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency		TBD			100			TBD		MHz
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$t_{PLH}$	Propagation Delay @ 1.5 V	2.0		5.5	2.0		5.5	2.0		5.5	ns
$t_{PHL}$	Propagation Delay @ 1.5 V	2.0		5.5	2.0		5.5	2.0		5.5	ns
$V_{PP}$	Input Swing (Note 8)	200		1000	200		1000	200		1000	mV
$t_r/t_f$	Output Rise/Fall Time (10-90%)					750					ps

7.  $R_L = 500\ \Omega$  to GND and  $C_L = 20\text{ pF}$  to GND. Refer to Figure 2.

8.  $V_{PP}(\text{min})$  is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of  $\approx 40$ .

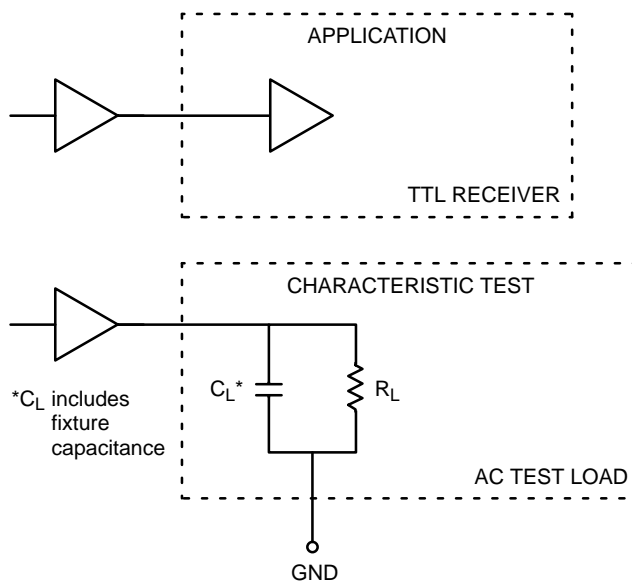


Figure 2. TTL Output Loading Used for Device Evaluation

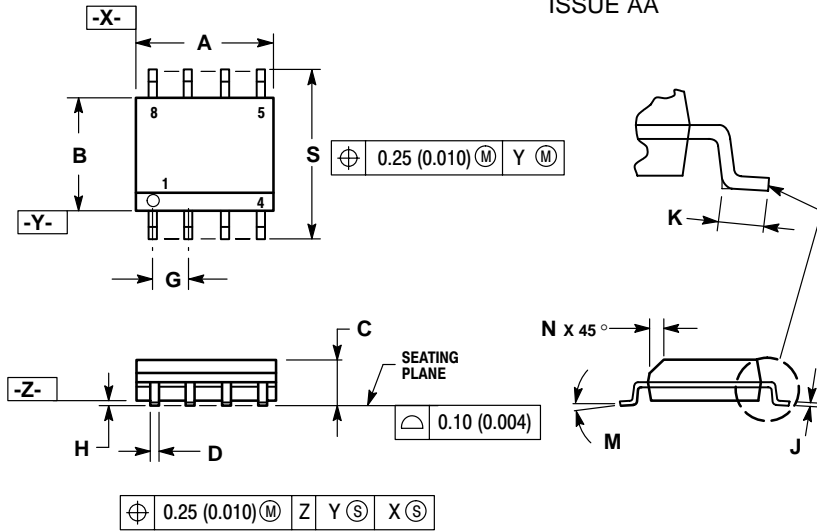
## Resource Reference of Application Notes

- AN1404** - ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** - ECL Clock Distribution Techniques
- AN1406** - Designing with PECL (ECL at +5.0 V)
- AN1503** - ECLinPS I/O SPICE Modeling Kit
- AN1504** - Metastability and the ECLinPS Family
- AN1560** - Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** - Interfacing Between LVDS and ECL
- AN1596** - ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** - Using Wire-OR Ties in ECLinPS Designs
- AN1672** - The ECL Translator Guide
- AND8001** - Odd Number Counters Design
- AND8002** - Marking and Date Codes
- AND8020** - Termination of ECL Logic Devices

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## PACKAGE DIMENSIONS

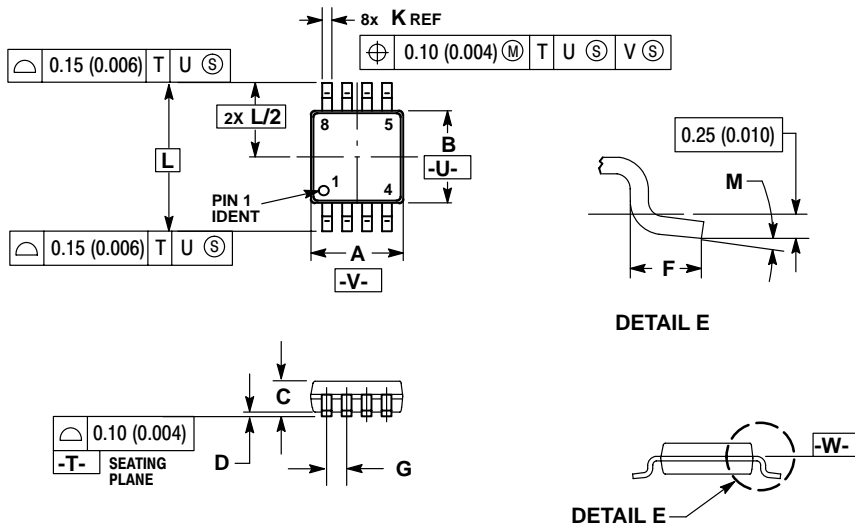
### SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE AA



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### TSSOP-8 DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948R-02 ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

## Notes

## Notes

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