

# MC10E116, MC100E116

## 5V ECL Quint Differential Line Receiver

The MC10E/100E116 is a quint differential line receiver with emitter-follower outputs. For applications which require bandwidths greater than that of the E116, the E416 device may be of interest.

Active current sources plus a deep collector feature of the MOSAIC III process provide the receivers with excellent common-mode noise rejection. Each receiver has a dedicated VCCO supply lead, providing optimum symmetry and stability.

If both inverting and non-inverting inputs are at an equal potential of  $> -2.5$  V, the receiver does *not* go to a defined state, but rather current-shares in normal differential amplifier fashion, producing output voltage levels midway between HIGH and LOW, or the device may even oscillate.

The V<sub>BB</sub> pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V<sub>BB</sub> as a switching reference voltage. V<sub>BB</sub> may also rebias AC coupled inputs. When used, decouple V<sub>BB</sub> and V<sub>CC</sub> via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V<sub>BB</sub> should be left open.

The 100 Series contains temperature compensation.

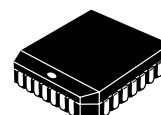
- 500 ps Max. Propagation Delay
  - V<sub>BB</sub> Supply Output
  - Dedicated V<sub>CCO</sub> Pin for Each Receiver
  - PECL Mode Operating Range: V<sub>CC</sub> = 4.2 V to 5.7 V with V<sub>EE</sub> = 0 V
  - NECL Mode Operating Range: V<sub>CC</sub> = 0 V with V<sub>EE</sub> = -4.2 V to -5.7 V
  - Output Qs will default low when inputs are  $< V_{CC} - 2.5$  V
  - Internal Input Pulldown Resistors
  - Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
  - ESD Protection:  $> 2$  KV HBM,  $> 200$  V MM
  - Moisture Sensitivity Level 1
- For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
  - Transistor Count = 98 devices



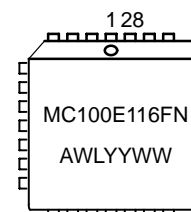
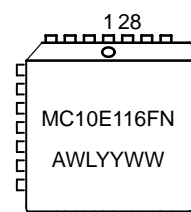
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### MARKING DIAGRAMS



**PLCC-28  
FN SUFFIX  
CASE 776**

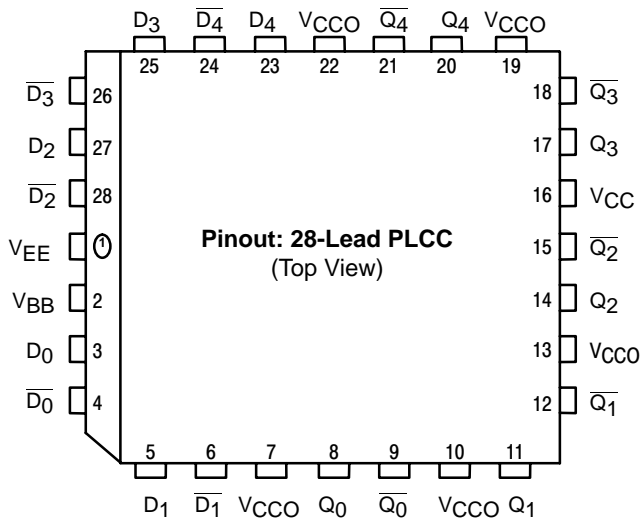


A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC10E116FN	PLCC-28	37 Units/Rail
MC10E116FNR2	PLCC-28	500 Units/Reel
MC100E116FN	PLCC-28	37 Units/Rail
MC100E116FNR2	PLCC-28	500 Units/Reel

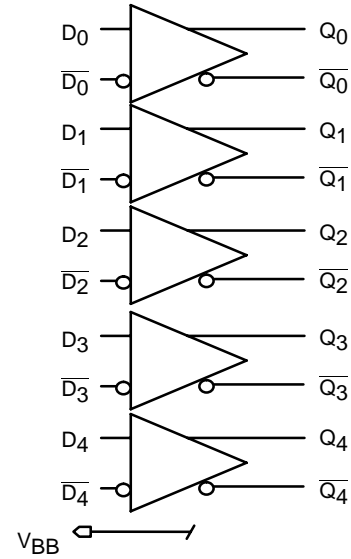
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\* All  $V_{CC}$  and  $V_{CCO}$  pins are tied together on the die.

Warning: All  $V_{CC}$ ,  $V_{CCO}$ , and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Pinout Assignment**



**Figure 2. Logic Diagram**

## PIN DESCRIPTION

PIN	FUNCTION
$D_0, \overline{D}_0 - D_4, \overline{D}_4$	ECL Differential Input Pairs
$Q_0, \overline{Q}_0 - Q_4, \overline{Q}_4$	ECL Differential Output Pairs
$V_{BB}$	Reference Voltage Output.
$V_{CC}, V_{CCO}$	Positive Supply
$V_{EE}$	Negative Supply

## MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8	V
$V_{EE}$	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-8	V
$V_I$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V V
$I_{out}$	Output Current	Continuous Surge		50 100	mA mA
$I_{BB}$	$V_{BB}$ Sink/Source			$\pm 0.5$	mA
$T_A$	Operating Temperature Range			0 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	$^{\circ}\text{C/W}$ $^{\circ}\text{C/W}$
$\theta_{JC}$	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	$^{\circ}\text{C/W}$
$V_{EE}$	PECL Operating Range NECL Operating Range			4.2 to 5.7 -5.7 to -4.2	V V
$T_{sol}$	Wave Solder	< 2 to 3 sec @ 248 $^{\circ}\text{C}$		265	$^{\circ}\text{C}$

1. Maximum Ratings are those values beyond which device damage may occur.

# MC10E116, MC100E116

## 10E SERIES PECL DC CHARACTERISTICS $V_{CCx} = 5.0\text{ V}$ ; $V_{EE} = 0.0\text{ V}$ (Note 1)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		29	35		29	35		29	35		29	35	mA
$V_{OH}$	Output HIGH Voltage (Note 2)				3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
$V_{OL}$	Output LOW Voltage (Note 2)				3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)				3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)				3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
$V_{BB}$	Output Voltage Reference	3.57		3.7	3.57		3.7	3.65		3.75	3.69		3.81	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3)				2.2		4.4	2.2		4.4	2.2		4.4	V
$I_{IH}$	Input HIGH Current			200			200			200			200	$\mu\text{A}$
$I_{IL}$	Input LOW Current				0.5	0.3		0.5	0.25		0.3	0.2		$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.46 V / -0.06 V.
2. Outputs are terminated through a 50  $\Omega$  resistor to  $V_{CC}$ -2 volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .

## 10E SERIES NECL DC CHARACTERISTICS $V_{CCx} = 0.0\text{ V}$ ; $V_{EE} = -5.0\text{ V}$ (Note 1)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		29	35		29	35		29	35		29	35	mA
$V_{OH}$	Output HIGH Voltage (Note 2)				-1020	-930	-840	-980	-895	-810	-910	-815	-720	mV
$V_{OL}$	Output LOW Voltage (Note 2)				-1950	-1790	-1630	-1950	-1790	-1630	-1950	-1773	-1595	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)				-1170	-1005	-840	-1130	-970	-810	-1060	-890	-720	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)				-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
$V_{BB}$	Output Voltage Reference	-1.43		-1.3	-1.13		-1.30	-1.35		-1.25	-1.31		-1.19	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3)				-2.8		-0.6	-2.8		-0.6	-2.8		-0.6	V
$I_{IH}$	Input HIGH Current			200			200			200			200	$\mu\text{A}$
$I_{IL}$	Input LOW Current				0.5	0.3		0.5	0.065		0.3	0.2		$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.46 V / -0.06 V.
2. Outputs are terminated through a 50  $\Omega$  resistor to  $V_{CC}$ -2 volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .

# MC10E116, MC100E116

## 100E SERIES PECL DC CHARACTERISTICS $V_{CCx} = 5.0\text{ V}$ ; $V_{EE} = 0.0\text{ V}$ (Note 1)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		29	35		29	35		29	35		29	40	mA
$V_{OH}$	Output HIGH Voltage (Note 2)				3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
$V_{OL}$	Output LOW Voltage (Note 2)				3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)				3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)				3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
$V_{BB}$	Output Voltage Reference	3.62		3.74	3.64		3.75	3.62		3.74	3.62		3.74	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3)				2.2		4.4	2.2		4.4	2.2		4.4	V
$I_{IH}$	Input HIGH Current			200			200			200			200	$\mu\text{A}$
$I_{IL}$	Input LOW Current				0.5	0.3		0.5	0.25		0.5	0.2		$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.46 V / -0.8 V.
2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}$ -2 volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .

## 100E SERIES NECL DC CHARACTERISTICS $V_{CCx} = 0.0\text{ V}$ ; $V_{EE} = -5.0\text{ V}$ (Note 1)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		29	35		29	35		29	35		29	40	mA
$V_{OH}$	Output HIGH Voltage (Note 2)				-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
$V_{OL}$	Output LOW Voltage (Note 2)				-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)				-1165	-950	-880	-1165	-880	-880	-1165	-880	-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)				-1810	-1700	-1475	-1810	-1475	-1475	-1810	-1475	-1475	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.26	-1.38		-1.25	-1.38		-1.26	-1.38		-1.26	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3)				-2.8		-0.6	-2.8		-0.6	-2.8		-0.6	V
$I_{IH}$	Input HIGH Current			200			200			200			200	$\mu\text{A}$
$I_{IL}$	Input LOW Current				0.5	0.3		0.5	0.25		0.5	0.2		$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

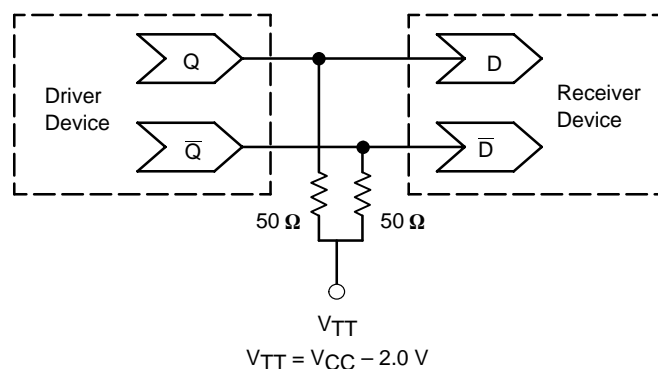
1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.46 V / -0.8 V.
2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}$ -2 volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .

# MC10E116, MC100E116

**AC CHARACTERISTICS**  $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output D (Differential) D (Single-Ended)	150 150	300 300	500 550	200 150	300 300	450 500	200 150	300 300	450 500	ps
$t_{skew}$	Within-Device Skew (Note 2)		50			50			50		ps
$t_{skew}$	Duty Cycle Skew (Note 3) $t_{PLH} - t_{PHL}$		$\pm 10$			$\pm 10$			$\pm 10$		ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$V_{PP}$	Input Voltage Swing (Differential) (Note 4)	150			150			150			mV
$t_r/t_f$	Rise/Fall Time 20–80%	250	375	625	275	375	575	275	375	575	ps

- 10 Series:  $V_{EE}$  can vary  $+0.46\text{ V} / -0.06\text{ V}$ .  
100 Series:  $V_{EE}$  can vary  $+0.46\text{ V} / -0.8\text{ V}$ .
- Within-device skew is defined as identical transitions on similar paths through a device.
- Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
- Minimum input swing for which AC parameters are guaranteed.



**Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

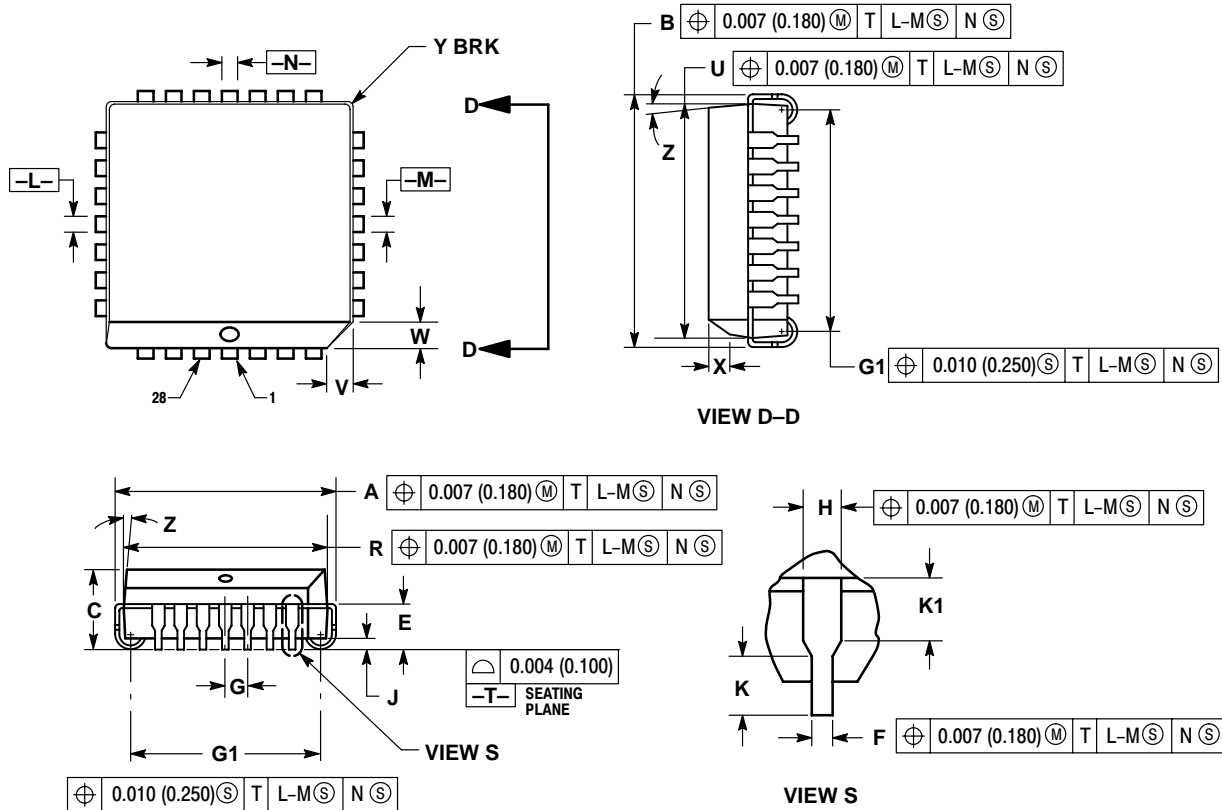
## Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at  $+5.0\text{ V}$ )
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

# MC10E116, MC100E116

## PACKAGE DIMENSIONS

PLCC-28  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 776-02  
ISSUE E




### NOTES:

1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2° 10°		2° 10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

## **Notes**

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