
MSM6568A

160-DOT COMMON DRIVER

GENERAL DESCRIPTION

The MSM6568A is a dot matrix LCD common driver which is fabricated in CMOS technology. The MSM6568A consists of two 80-bit bidirectional shift registers, two 80-bit level shifters, and two 80-bit 4-level drivers.

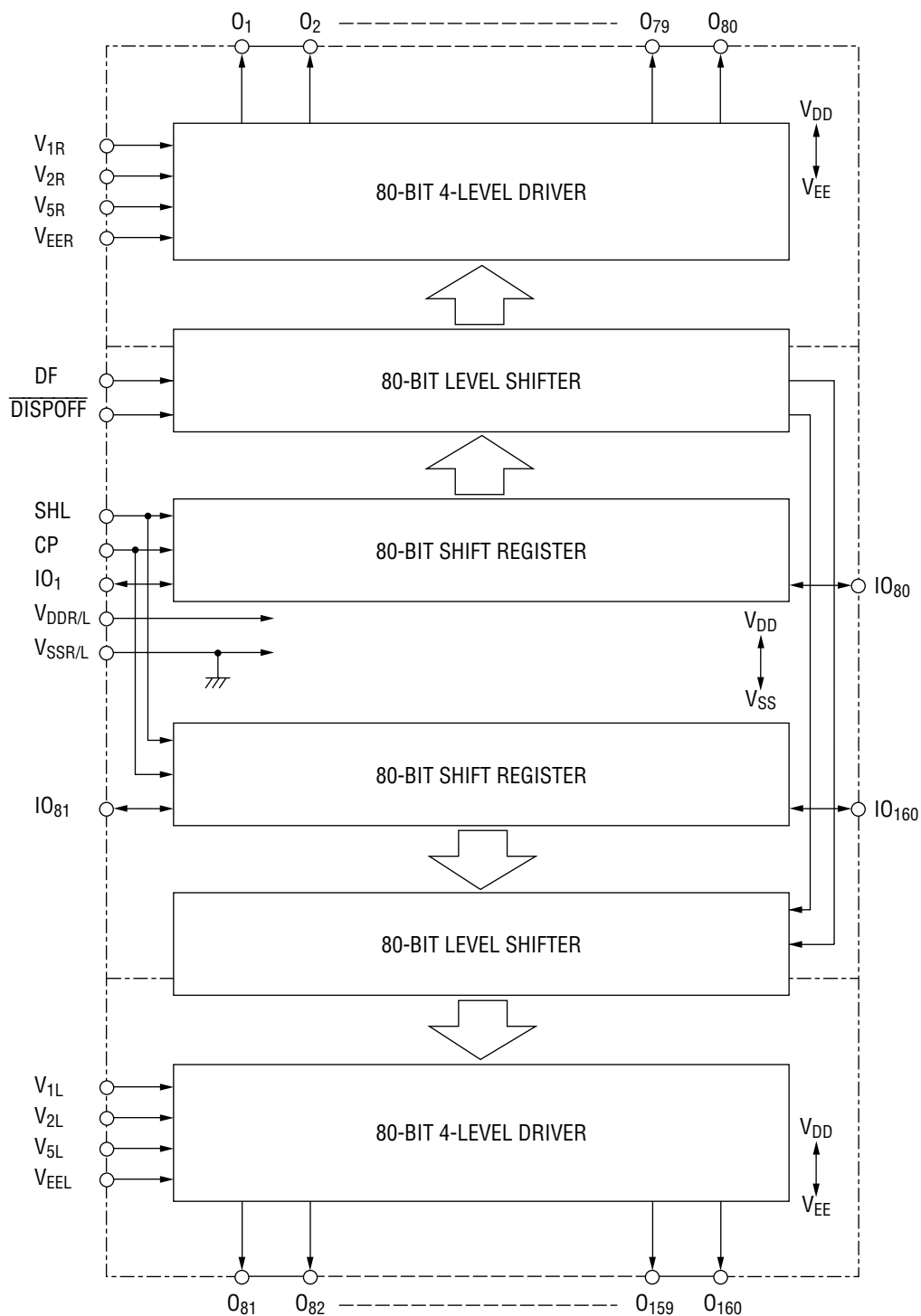
The MSM6568A is equipped with 160 output pins. By connecting two or more MSM6568A devices in cascade, the number of LCD outputs can be increased.

The MSM6568A can drive a variety of LCD panels because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from an external source.

FEATURES

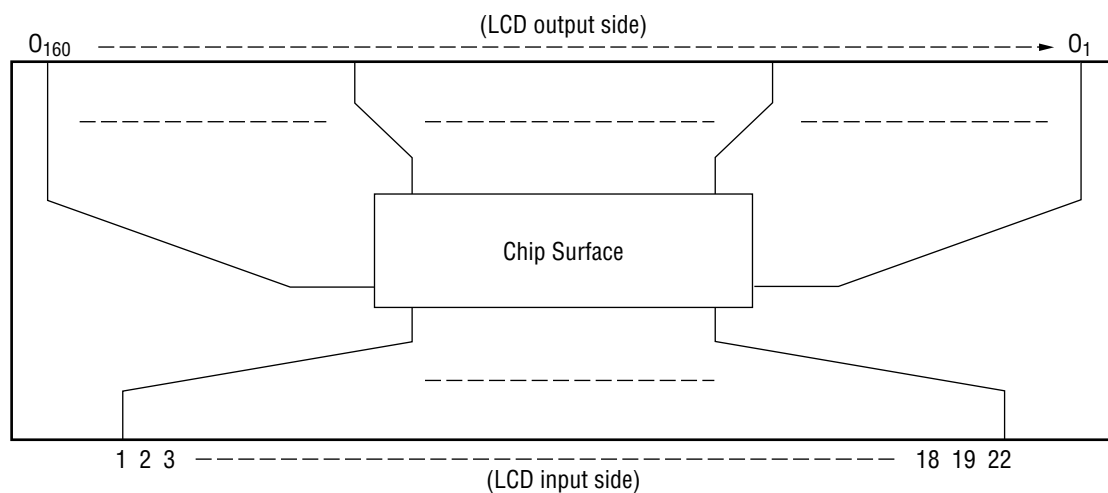
- Logic supply voltage : 2.7 to 5.5V
- LCD driving voltage : 14 to 28V
- Applicable LCD duty : 1/64 to 1/256
- External bias power supply available
- Package :
 - TCP mounting with 70mm wide film (Product name : MSM6568AV-Z)
 - Tin-plated

BLOCK DIAGRAM



($V_{DDR/L}$ stands for V_{DDR} and V_{DDL} , and $V_{SSR/L}$ for V_{SSR} and V_{SSL} .)

PIN CONFIGURATION (TOP VIEW)



| Pin | Symbol | Pin | Symbol |
|-----|-----------------------------|-----|-------------------|
| 1 | V _{1L} | 12 | IO ₁₆₀ |
| 2 | V _{2L} | 13 | IO ₈₁ |
| 3 | V _{5L} | 14 | IO ₈₀ |
| 4 | V _{EEL} | 15 | IO ₁ |
| 5 | NC | 16 | V _{SSR} |
| 6 | V _{DDL} | 17 | V _{DDR} |
| 7 | SHL | 18 | NC |
| 8 | V _{SSL} | 19 | V _{EER} |
| 9 | $\overline{\text{DISPOFF}}$ | 20 | V _{5R} |
| 10 | CP | 21 | V _{2R} |
| 11 | DF | 22 | V _{1R} |

NC : No connection

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|----------------------|-----------|---|----------------------|--------------------|
| Power Supply Voltage | V_{DD} | $T_a=25^{\circ}\text{C}$ | -0.3 to +6.5 | V |
| Bias Voltage | V_{LCD} | $T_a=25^{\circ}\text{C}, V_{DD} - V_{EE}$ | 0 to 30 | V |
| Input Voltage | V_I | $T_a=25^{\circ}\text{C}$ | -0.3 to $V_{DD}+0.3$ | V |
| Storage Temperature | T_{STG} | — | -30 to +85 | $^{\circ}\text{C}$ |

- * $V_1 > V_2 > V_5 > V_{EE}$
 $V_{EE} < V_5 \leq V_{EE} + 10\text{V}$
 $V_{DD} \geq V_1 > V_2 \geq V_{DD} - 10\text{V}$
 $V_{DD} = V_{DDR} = V_{DDL}, V_1 = V_{1R} = V_{1L}, V_2 = V_{2R} = V_{2L},$
 $V_5 = V_{5R} = V_{5L}, V_{EE} = V_{EER} = V_{EEL}$

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Range | Unit |
|-----------------------|-----------|-------------------|------------------|--------------------|
| Power Supply Voltage | V_{DD} | — | 2.7 to 5.5 | V |
| Bias Voltage | V_{LCD} | $V_{DD} - V_{EE}$ | No load | 14 to 28 |
| | | | LCD being driven | 18 to 28 |
| Operating Temperature | T_{op} | — | -20 to +75 | $^{\circ}\text{C}$ |

- * $V_1 > V_2 > V_5 > V_{EE}$
 $V_{EE} < V_5 \leq V_{EE} + 7\text{V}$
 $V_{DD} \geq V_1 > V_2 \geq V_{DD} - 7\text{V}$
 $V_{DD} = V_{DDR} = V_{DDL}, V_1 = V_{1R} = V_{1L}, V_2 = V_{2R} = V_{2L},$
 $V_5 = V_{5R} = V_{5L}, V_{EE} = V_{EER} = V_{EEL}$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=2.7 to 5.5V, T_a=-20 to +75°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--------------------|--------------------|---|----------------------|------|--------------------|------|
| "H" Input Voltage | V _{IH} *1 | — | 0.8V _{DD} | — | — | V |
| "L" Input Voltage | V _{IL} *1 | — | — | — | 0.2V _{DD} | V |
| "H" Input Current | I _{IH} *1 | V _I =V _{DD} , V _{DD} =5.5V | — | — | 1 | μA |
| "L" Input Current | I _{IL} *1 | V _I =0V, V _{DD} =5.5V | — | — | -1 | μA |
| "H" Output Voltage | V _{OH} *2 | I _O =-0.2mA, V _{DD} =2.7V | V _{DD} -0.4 | — | — | V |
| "L" Output Voltage | V _{OL} *2 | I _O =0.2mA, V _{DD} =2.7V | — | — | 0.4 | V |
| ON Resistance | R _{ON} *4 | V _{DD} -V _{EE} =25V *3 | — | — | 2.0 | kΩ |
| | | I _{VN-V_O} =0.25V | — | — | | |
| Supply Current | I _{SS} | CP=22kHz, V _{DD} =3.0V | — | — | 50 | μA |
| | I _{EE} | V _{DD} -V _{EE} =25V, no load*5 | — | — | 300 | |
| Input Capacitance | C _I | f=1MHz | — | 5 | — | pF |

*1 Applied to CP, IO₁, IO₈₀, IO₈₁, IO₁₆₀, SHL, DF, $\overline{\text{DISPOFF}}$ *2 Applied to IO₁, IO₈₀, IO₈₁, IO₁₆₀

*3 V_N=V_{DD} to V_{EE}, V₂=1/16 (V_{DD} - V_{EE}), V₅=15/16 (V_{DD} - V_{EE})
V_{DD}=V₁, V_{DD}=4.5V, V₁=V_{1L}=V_{1R}, V₂=V_{2L}=V_{2R}, V₅=V_{5L}=V_{5R}, V_{EE}=V_{EEL}=V_{EER},
V_{DD}=V_{DDL}=V_{DDR}

*4 Applied to O₁ to O₁₆₀

*5 Input a "H" level signal through the IO pins every 240 clock pulses when a supply current is measured.

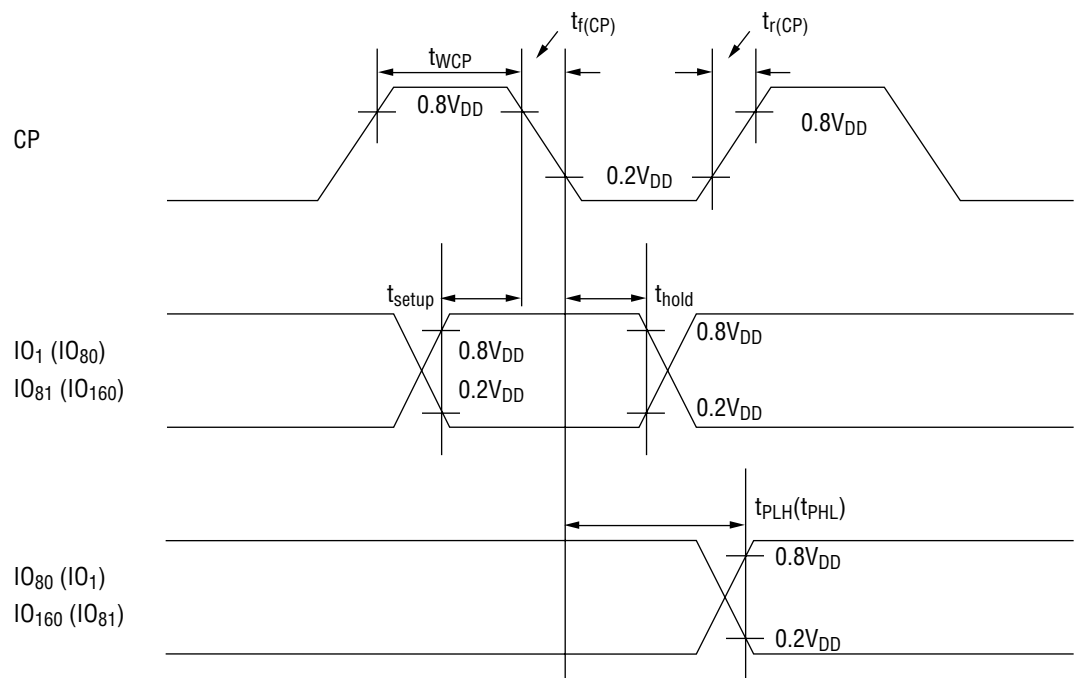
The DF frequency is 45Hz.

Switching Characteristics

(V_{DD}=2.7 to 5.5V, T_a=-20 to +75°C, C_L=15pF)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--|--|-----------|------|------|------|------|
| "H", "L" Propagation Delay Time | t _{PHL} | — | — | — | 3 | μs |
| | t _{PLH} | — | — | — | | |
| Maximum Clock Frequency | f _{CP} | — | 1 | — | — | MHz |
| Clock Pulse Width | t _{WCP} | — | 63 | — | — | ns |
| Data Setup Time IO _n →CP | t _{setup} *1 | — | 100 | — | — | ns |
| Data Hold Time CP→IO _n | t _{hold} *1 | — | 100 | — | — | ns |
| Rise Time / Fall Time of CP | t _r (CP) t _f (CP) | — | — | — | 20 | ns |

*1 IO_n=IO₁-IO₁₆₀



FUNCTIONAL DESCRIPTION

Pin Functional Description

- $IO_1, IO_{80}, IO_{81}, IO_{160}$
Data input/output pins for the two 80-bit bidirectional shift registers.
- SHL
Input pin to select the shift direction of the two 80-bit bidirectional registers.
Table 1 shows the relations between the SHL pin and the $IO_1, IO_{80}, IO_{81}, IO_{160}$ pins.
- CP
Clock pulse input pin for the two 80-bit bidirectional shift registers.
Scan data shifts at the falling edge of a clock pulse.
- DF
Signal input pin to synchronize with AC current for LCD driving waveforms.
Normally an inverted frame signal is input to this pin.
- $V_{DDL}, V_{DDR}, V_{SSL}, V_{SSR}$
Power supply pins.
Normal operating conditions are $V_{DDR}=V_{DDL}=2.7$ to $5.5V$, $V_{SSR}=V_{SSL}=0V$.
- DISPOFF
Input pin to control the O_1 to O_{160} outputs. During input of "L" level, V_1 levels are output from O_1 to O_{160} .
- $V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{5L}, V_{5R}, V_{EE}, V_{EER}$
Bias voltage input pins for LCD driving. Voltages must be input to all these pins.
- O_1 to O_{160}
4-level driver output pins corresponding to each bit of the shift registers.
The V_1, V_2, V_5 , or V_{EE} level is selected and output based on the combination of shift register data and a DF signal.
Table 2 shows the relations between the scan data and the LCD driving outputs.

Table 1

| SHL | Shift direction | $IO_1, IO_{81} / IO_{80}, IO_{160}$ | I/O | Input |
|-----|------------------------------|-------------------------------------|--------|---|
| L | $O_1 \rightarrow O_{80}$ | IO_1, IO_{81} | Input | IO_1 and IO_{81} are data input pins for the shift register. Data is input to these pins in synchronization with clocks and is output from IO_{80} and IO_{160} with delay by the number (80) of shift register bits in synchronization with clocks. |
| | $O_{81} \rightarrow O_{160}$ | IO_{80}, IO_{160} | Output | |
| H | $O_{80} \rightarrow O_1$ | IO_{80}, IO_{160} | Input | IO_{80} and IO_{160} are data input pins for the shift register. Data is input to these pins in synchronization with clocks and is output from IO_1 and IO_{81} with delay by the number (80) of shift register bits in synchronization with clocks. |
| | $O_{160} \rightarrow O_{81}$ | IO_1, IO_{81} | Output | |

Table 2

| Scan data | LCD driving output |
|-----------|----------------------------------|
| H | Select levels (V_1, V_{EE}) |
| L | Non-select levels (V_2, V_5) |

Truth Table

| DF | Shift register data | $\overline{\text{DISPOFF}}$ | Driver output level (O₁-O₁₆₀) |
|-----------|----------------------------|---|--|
| L | L | H | V ₂ |
| L | H | H | V _{EE} |
| H | L | H | V ₅ |
| H | H | H | V ₁ |
| X | X | L | V ₁ |

X : Don't Care