OCT7102

255 Channel ADPCM Encoder/Decoder

Reducing cost, power and size for high-density ADPCM compression.

The OCT7102 offers a very low cost, low power, and area efficient solution for high-density ADPCM compression. Using a specially designed processing core, the OCT7102 can compress and decompress up to 255 full duplex audio connections in a single device, requiring no external components for full operation. This equates to a DSP based performance of 2550 MIPS in 1 square inch. This capability can be used to offload more costly DSP based ADPCM compression in existing products or be combined with other Octasic devices for a seamless compression and packetization solution.

Compression and decompression can be done at rates of 16, 24, 32 and 40 kbps. PCM data can also be passed through the device transparently. In addition, a built-in 2100 Hz detector can be used to detect fax and/or modem connections, with or without phase reversal, on a per channel basis. The device can be configured to automatically change the compression rate of a channel when a tone is detected, and/or optionally interrupt software.

When used with Octasic packetization devices such as the OCT8304 (VoIP/AAL2 SAR) or the Mitel MT90502 (AAL2 SAR), the OCT7102 can also provide the following features using unique formats on the H.1x0 Bus:

- Automatic ADPCM CODEC resets for silence suppression per ITU I366.2 standard
- Automatic PCM/ADPCM rate changes on packet boundaries with no loss of audio quality
- Improved voice activity detection with silence suppression control
- Automatic DC offset filtering and SID power calculation

Applications

- DSP Offload
- Voice over ATM
- Voice over DSL
- Voice over Cable
- High-density Voice Gateways
- PBX Platforms
- Voice Messaging Systems

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Interfaces

There are two main interfaces to the device: an H.100/H.110 slave interface and a micro-processor port. The H.100/H.110 interface is a fully compliant slave device. It can use any of the 4096 timeslots for input or output. The timeslots are organized in 32 streams that have configurable frequency selections of 2.048, 4.096, or 8.192 MHz in groups of four streams. The OCT7102 detects the validity of the clocks on the bus in order to execute clock fallback in case of failure.

The microprocessor interface can be used in an Intel or Motorola mode, with 8 or 16 bits of data. An interrupt can also be generated on this interface.

Miscellaneous signals include: a JTAG test interface, a global reset pin and a master clock pin. Sixteen (16) GPIO pins are also available.

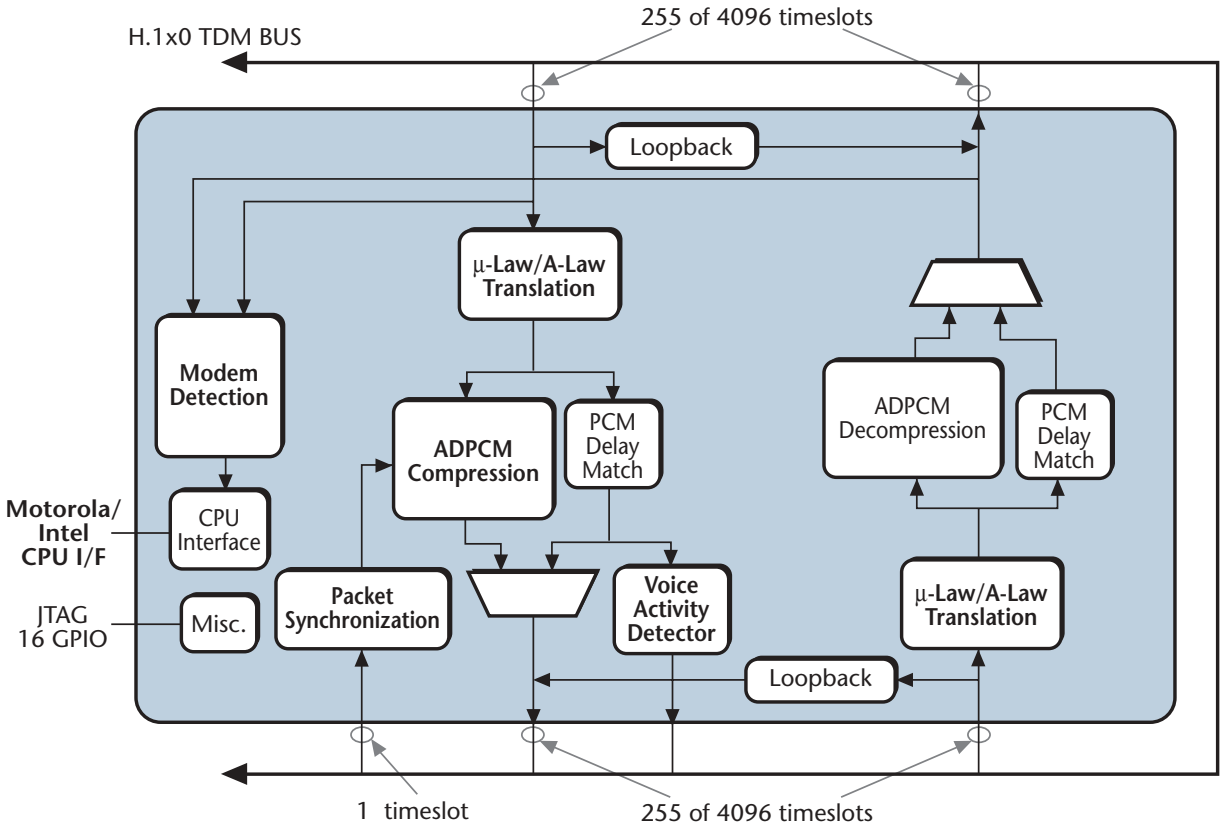
Support

In addition to the device itself, Octasic provides a developers kit with: the ORCAD library elements, example schematics, and an operating system independent API.

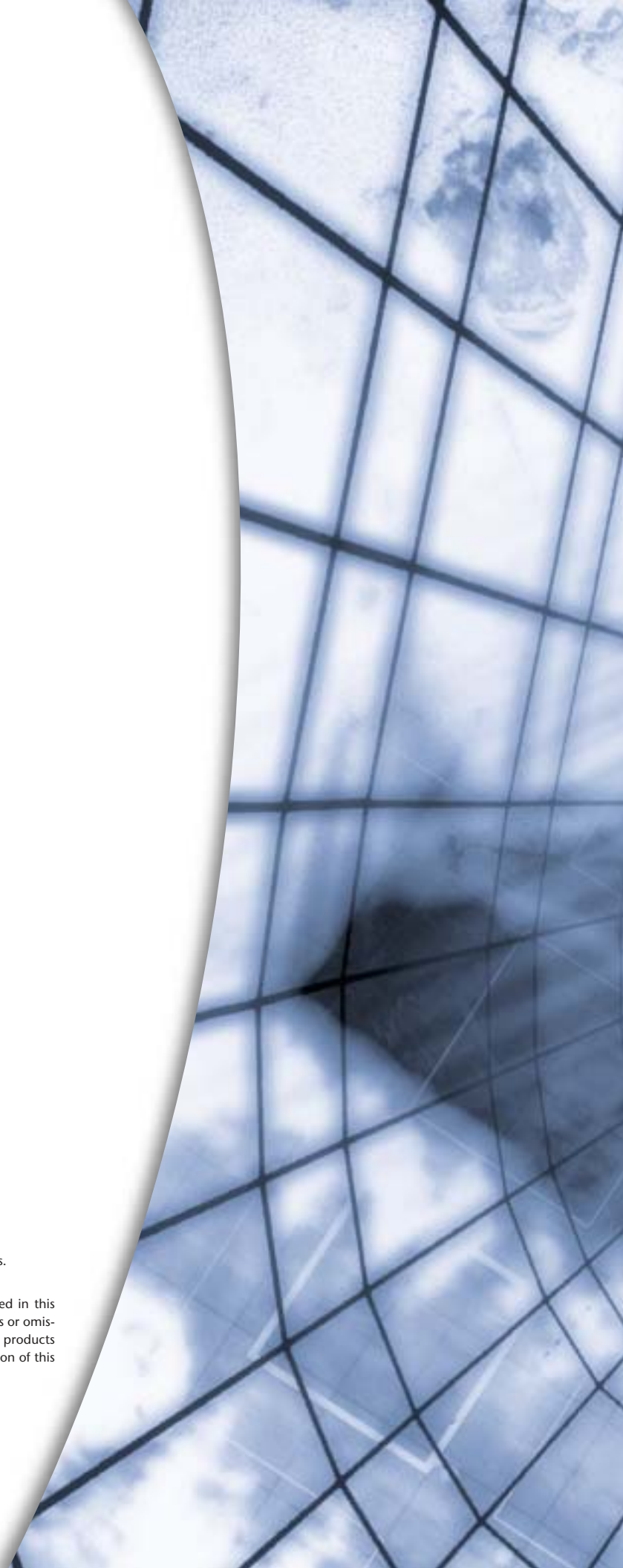
Benefits

- 255 channel full duplex ADPCM/ PCM CODEC
- Less than 4mW of power per channel
- 2100 Hz fax/modem detection with or without phase reversal
- Dynamic compression rate changes (16, 24, 32, 40, 64 kbps)
- H.100/H.110 slave compliant
- Full 4096 timeslot support
- Provides per channel PCM translation (A-law to/from µ-law)
- Asynchronous Intel/Motorola micro-processor control interface (8/16 bit Data)
- Read and write cache for fast accesses
- No external components required
- Device API available
- JTAG interface
- 3.3 V and 2.5V power supply
- Packaged in a 176 pin LQFP

OCT7102 BLOCK DIAGRAM



Ordering Information	
Order #	**Item**
OCT7102	OCT7102 with API License



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