
12-Bit 80MSPS 0.18 μ m Analog-to-Digital Converter IP **nAD1280-18TS**

FEATURES

- 3.3V power supply
- 150 μ V input referred noise
- Low power (250mW @ 3.3V and 80MSPS)
- Compact area (2.47mm²)
- Frequency dependent biasing
- Single ended input
- 1X-2X gain input stage
- Low input capacitance
- Two power saving idle modes
- TSMC Imaging process: 4 metal layers

GENERAL DESCRIPTION

The nAD1280-18TS is a compact, high-speed, low power 12-bit monolithic analog-to-digital converter, implemented in the TSMC imaging 0.18 μ m CMOS process with MiM capacitor and thick oxide options, and 4 metal layers. The converter includes a single ended to differential low-noise input stage, with 1X or 2X gain, making it ideal for imaging applications. Using internal references, the full scale range is 0-1V in 2X mode and 0-2V in 1X mode. The full scale range can be reduced by using external references. It operates from a single 3.3V supply. The bias current level for the ADC is automatically adjusted based on the clock input frequency. Hence, the power dissipation of the device is continuously minimised for the current operation frequency.

The nAD1280-18TS has a pipelined architecture - resulting in low input capacitance. Digital error correction of the 11 most significant bits ensures good linearity for input frequencies approaching Nyquist. The nAD1280-18TS is compact. The core occupies less than 2.5mm² of die. The differential architecture makes it insensitive to substrate noise. Thus it is ideal as a mixed signal ASIC macro cell.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Supply voltage		2.95	3.3	3.6	V
P _D	Power dissipation	80MSPS		250		mW
DNL	Differential nonlinearity	f _{IN} =0.9991MHz			±0.5	LSB
INL	Integral nonlinearity	f _{IN} =0.9991MHz			TBD	LSB
V _n rms	Input referred noise	1X-mode		250	400	μ V
V _n rms	Input referred noise	2X-mode		150	200	μ V

Table 1: Quick reference data

PRODUCT SPECIFICATION



nAD1280-18TS: 12 Bit 80 MSPS 0.18 μ m 3.3V ADC IP

ELECTRICAL SPECIFICATIONS

(At $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, Sampling Rate = 80MHz, Input frequency = 10MHz, Differential input signal, 50% duty cycle clock and 300nF Reference decoupling unless otherwise noted)

Symbol	Parameter (condition)	TestLev.	Min.	Typ.	Max.	Units
DC Accuracy						
DNL	Differential Nonlinearity $f_{IN} = 0.9991\text{ MHz}$			± 0.5		LSB
INL	Differential Nonlinearity $f_{IN} = 0.9991\text{ MHz}$			TBD		LSB
V_{OS}	Midscale offset			± 1		%FS
ϵ_G	Gain Error			± 2		%FS
Dynamic Performance						
V_{nrms}	Input referred noise (1X-mode)			250	400	μV
V_{nrms}	Input referred noise (2X mode)			150	200	μV
Analog Input						
V_{FSR}	Input Voltage Range (1X-mode)			2		V
V_{FSR}	Input Voltage Range (2X-mode)			1		V
C_{INA}	Input Capacitance (1X-mode)			1.8		pF
C_{INA}	Input Capacitance (1X-mode)			3.5		pF
	Input signal attenuation			TBD		dB
Reference Voltages						
V_{REFI01}	Internal reference voltage on ref[0]			1.15		V
V_{REFI11}	Internal reference voltage on ref[1]			2.15		V
	Internal reference voltage drift			100		ppm/ $^\circ\text{C}$
V_{REFI01}	Negative Input Voltage (external ref)			1.15		V
V_{REFI11}	Positive Input Voltage (external ref)			2.15		V
V_{RR}	Reference input voltage range			1		V
Switching Performance						
$F_{S\max}$	Maximum Conversion Rate		80			MSPS
$F_{S\min}$	Minimum Conversion Rate			15		MSPS
	Pipeline Delay			7		Clocks
t_{AP}	Aperture delay, IP		0.7	1	1.5	ns
t_h	Output hold time, IP (max 0.2 pF load)		1.5	2	3.5	ns
t_d	Output delay time, IP (max 0.2 pF load)		2	3	4.5	ns
Digital Inputs						
V_{IL}	Logic "0" voltage				0.25	V
V_{IH}	Logic "1" voltage		$AV_{DD}-0.25$			V
I_{IL}	Logic "0" current ($V_i=V_{SS}$)				± 10	μA
I_{IH}	Logic "1" current ($V_i=V_{DD}$)				± 10	μA
C_{IND}	Input Capacitance			0.03	0.1	pF
Digital Outputs						
V_{OL}	Logic "0" voltage ($I = 2\text{ mA}$)			0.1	0.25	V
V_{OH}	Logic "1" voltage ($I = 2\text{ mA}$)		$85\% OV_{DD}$	$90\% OV_{DD}$		V
Power Supply						
V_{DD}	Supply voltage		3.0	3.3	3.6	V
I_{DD}	Supply current (except digital output)			755		mA
V_{SS}	Supply voltage			GND		
P_D	Power dissipation active 15 MSPS			TBD		mW
P_D	Power dissipation active 80 MSPS			250		mW
P_D	Power dissipation Power Down Mode			TBD		μW
P_D	Power dissipation Standby Mode			TBD		mW
t_{start}	Start-up time from Power down			TBD		ms
t_{start}	Start-up time from Stand By			TBD		clock cycles
T	Junction operating temperature		-40		+125	$^\circ\text{C}$

Table 2: Electrical specifications



PIN FUNCTIONS AND PLACEMENT

Signals	Pads	Functions	X-coordinate	Y-coordinate	Metal-layer
GAIN_CTRL	1	1X/2X gain setting	337	1466	2
BITO(11:0)	12	Output bits	854,829,804,779, 755,230,705,680, 655,630,605,580	1466	2
OR_FLAG	1	Overflow-flag	880	1466	2
CLK	1	Clock	904	1466	2
REF_SEL	1	Disabling internal references	920	1466	2
PDBUS(2:0)	3	Powerdown control	952,944,936	1466	2
BSC(1:0)	1	Bias current control	969,984	1466	2
VDD_DIG	1	Digital power	1661-1683	0	2,3,Top
REF(1:0)	2	Reference voltages	1595,1572	0	3
AVSS	2	Common ground	875-1525	0	3,Top
AVDD	2	Analog ground	0-870	0	3,Top
IN_REF	1	Negative input	56	0	2
IN	1	Input signal	50	0	2

Table 3: Pin functions and placement

IP BLOCK LAYOUT

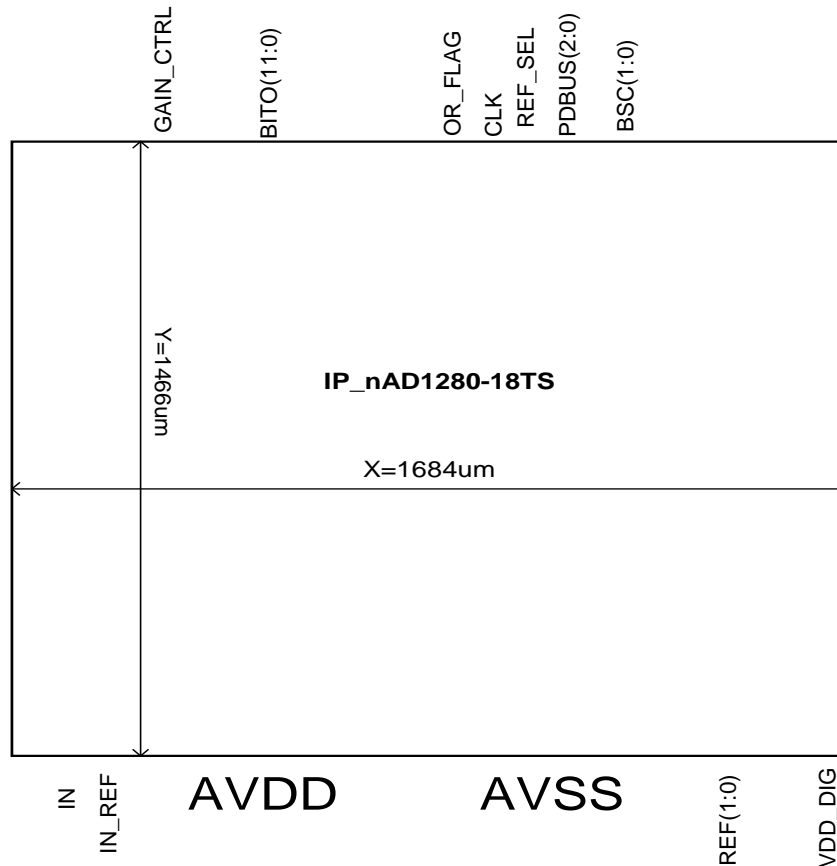


Figure 1: Size and pin placement for nAD1280-18TS IP



FUNCTIONAL BLOCK DIAGRAM

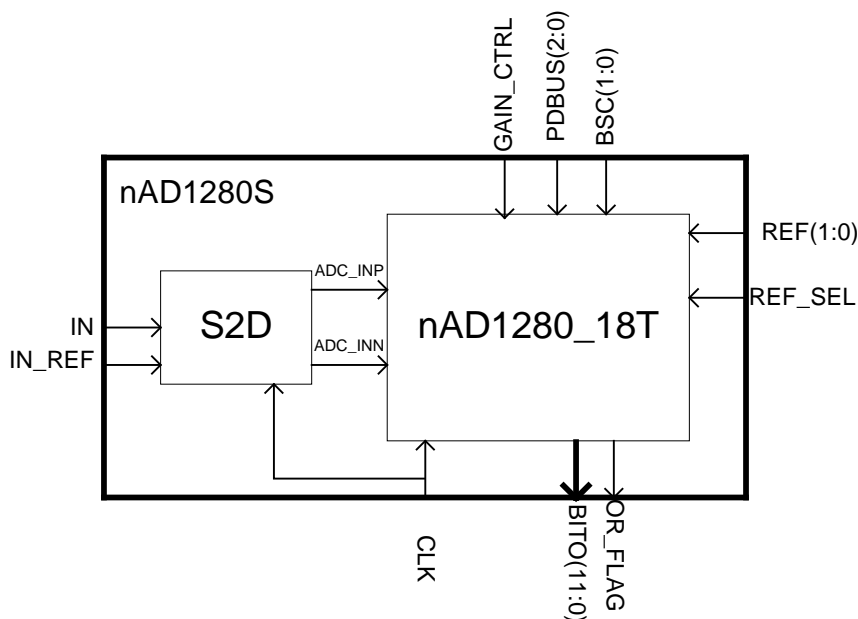


Figure 2: Functional Block diagram nAD1280-18TS

MODES OF OPERATION

The ADC has four different modes of operation, controlled as described in Table 4:

Mode of operation	Digital control and clock settings		
	BSC(1:0)	PDBUS(2:0)	CLOCK
Active	HIGH,HIGH	LOW,LOW,LOW	Running
Standby	LOW,LOW	HIGH,LOW,HIGH	Running
Power down	LOW,LOW	HIGH,HIGH,HIGH	Stopped

Table 4: Control settings for ADC operational modes

Active mode

In the active mode, the ADC is fully functional.

A performance versus power consumption trade off can be made by adding or subtracting 12.5% of the pipeline bias current with the bias1 and bias0 pins:

BSC(1:0)	CURRENT
01	-12.5%
10	+12.5%
11	Typical

Idle modes

In the two idle modes, the ADC is not functional. The different modes are distinguished primarily by power consumption and start-up time. Start-up time is defined as the time it takes for the ADC to reach full performance in active mode



when switched from an idle mode. Refer to ‘Electrical Specifications’ for power consumption and start-up times for the different modes.

While the start-up times for standby is constant, the start-up time in power down mode will be proportional to Off-Chip REF(1:0) decoupling. The amount of decoupling on the REF(1:0) will have impact on the performance.

TIMING DIAGRAM

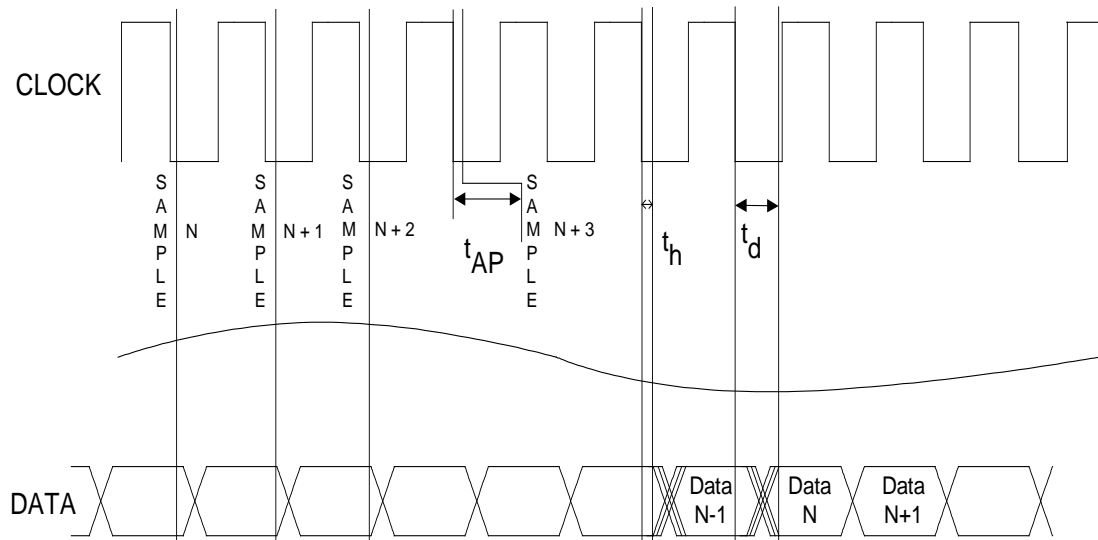


Figure 3: Timing diagram

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 5: Definitions

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.



APPLICATION INFORMATION

References

Reference voltages are generated internally for an input range of 1V/2V in 2X/1X gain mode respectively. The reference voltages can be set externally by setting the REF_SEL pin high. When this is chosen: use an appropriate operation amplifier to drive the voltages on pins REF(1:0). A design example can be found in the Evaluation Board user Guide. Externally generated reference voltages connected to REF(1:0) should be symmetrical around AVDD/2. The input full scale range can be defined between $\pm 0.5V$ and $\pm 0.5V$. Decoupling capacitors between the references and from each reference and to ground should be placed as close to the converter pins as possible using at least 300nF capacitors in parallel with smaller capacitors (e.g. 1nF).

Digital outputs

The digital output data appears in offset binary code at CMOS logic levels. Full-scale negative input results in output code 000...0. Full-scale positive input results in output code 111...1. Output data are available 7 clock cycles after the data are sampled. The analog input is sampled one aperture delay (t_{AP}) after the high to low clock transition. Output data should be sampled as shown in the timing diagram.

PCB layout and decoupling

A well designed PCB is necessary to get good spectral purity from any high performance ADC. A multilayer PCB with a solid ground plane is recommended for optimum performance. If the system has a split analog and digital ground plane, it is recommended that all ground pins on the ADC are connected to the analog ground plane. It is our experience that this gives the best performance. The power supply pins should be bypassed using 100nF in parallel with 1nF surface mounted capacitors as close to the package pins as possible. Analog and digital supply pins should be separately filtered.

Dynamic testing

Careful testing using high quality instrumentation is necessary to achieve accurate test results on high speed A/D-converters. It is important that the clock source and signal source has low jitter. A spectrally pure, low noise RF signal generator - such as the HP8662A or HP8644B is recommended for the test signal. Low pass filtering or band pass filtering of the input signal is usually necessary to obtain the required spectral purity (SFDR > 75dB). The clock signal can be obtained from either a crystal oscillator or a low-jitter pulse generator. Alternatively, a low-jitter RF-generator can be used as a clock source. At Nordic VLSI, the Marconi Instruments 2041A is used. The most consistent results are obtained if the clock signal is phase locked to the input signal. Phase locking allows testing without windowing of output data. A logic analyzer with deep memory - such as the HP16500-series, is recommended for test data acquisition.

PRODUCT SPECIFICATION



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ORDERING INFORMATION

Type number	Description	Price
nAD1280-18TS-IC	nAD1280-18TS sample in SSOP28 package (limited availability)	USD 50

Table 6: Ordering information

Product Specification. Revision Date: August 1st, 2002

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