Nordic VLSI ASA

12-Bit 30MSPS 0.18µm Analog-to-Digital Converter IP

nAD1230-18

FEATURES

- 1.8V power supply
- SNR typ 65dB for (f_{in} = 10MHz)
- Low power (35mW @ 1.8V and 30MSPS)
- Compact area (1.2mm^2)
- Frequency dependent biasing
- Differential input
- Low input capacitance
- Three power saving idle modes

APPLICATIONS

- Imaging
- Wireless communication
- WLAN/IEEE 802.11x
- DVB receivers
- Powerline communication
- Video products

GENERAL DESCRIPTION

The nAD1230-18 is a compact, high-speed, low power 12-bit monolithic analog-to-digital converter, implemented in the TSMC logic 0.18µm CMOS process. No mixed mode process options are needed. The converter includes a high bandwidth sample and hold. Using internal references, the full scale range is ±0.75V. The full scale range can be set between ±0.5V and ±0.75V using external references. It operates from a single 1.8V supply. Its low distortion and high dynamic range offers the performance needed for demanding imaging, multimedia, telecommunications and instrumentation applications. The bias current level for the ADC is automatically adjusted based on the clock input frequency. Hence, the power dissipation of the device is continuously minimised for the current operation frequency.

The nAD1230-18 has a pipelined architecture - resulting in low input capacitance. Digital error correction of the 11 most significant bits ensures good linearity for input frequencies approaching Nyquist. The nAD1230-18 is compact. The core occupies 1.2mm^2 of die area. The fully differential architecture makes it insensitive to substrate noise. Thus it is ideal as an mixed mode IP in a SoC design.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		1.6	1.8	2.0	V
P_D	Power dissipation (30 MSPS)	Except digital output drivers		35		mW
DNL	Differential nonlinearity	f_{IN}=0.9991MHz		±0.5		LSB
INL	Integral nonlinearity	f_{IN}=0.9991MHz		±1.5		LSB
SNR	Signal to noise ratio	f_{IN}=10MHz	62	65		dB
SFDR	Spurious free dynamic range	f_{IN}=10MHz		70		dB

Table 1: Quick reference data

ELECTRICAL SPECIFICATIONS

(At T_A = 25°C, V_{DD} = 1.8V, Sampling Rate = 30MHz, Input frequency = 10MHz, Differential input signal, 50% duty cycle clock and 300nF Reference decoupling unless otherwise noted)

Symbol	Parameter (condition)	Test Level	Min.	Typ.	Max.	Units
	DC Accuracy					
DNL	Differential Nonlinearity					
	f_{IN} = 0.9991 MHz	IV		±0.5		LSB
INL	Integral Nonlinearity					
	f_{IN} = 0.9991 MHz	IV		±1.5		LSB
V_{OS}	Midscale offset			± 1		%FS
CMRR	Common Mode Rejection Ratio			-59		dB
ε_G	Gain Error			±1		%FS
	Dynamic Performance					
SNR	Signal to Noise Ratio (without harmonics)					
	f_{IN} = 10 MHz	IV	62	65		dBFS
	f_{IN} = 40 MHz [1)]	IV	60	63		dBFS
	f_{IN} = 72 MHz [1)]	IV	56	60		dBFS
SINAD	Signal to Noise and Distortion Ratio					
	f_{IN} = 10 MHz	IV		64		dBFS
SFDR	Spurious Free Dynamic Range					
	f_{IN} = 10 MHz	IV		70		dB
	f_{IN} = 40 MHz	IV		63		dB
	f_{IN} = 72 MHz	IV		50		dB
	Analog Input					
V_{FSR}	Input Voltage Range (differential)	IV		±0.75		V
V_{CMI}	Analog input common mode voltage	IV	0.8	0.9	1.0	V
C_{INA}	Input Capacitance (from each input to ground)			2.2		pF
	Input signal attenuation @ 70MHz			0.35		dB
	Reference Voltages					
V_{REFN}	Internal reference voltage on pin 10	IV		0.525		V
V_{REFP}	Internal reference voltage on pin 11	IV		1.275		V
	Internal reference voltage drift				100	ppm/°C
V_{REFN}	Negative Input Voltage (external ref)	IV		0.525		V
V_{REFP}	Positive Input Voltage (external ref)	IV		1.275		V
V_{RR}	Reference input voltage range [2)]	IV		0.75		V
V_{CM}	Common mode voltage output	IV		0.9		V
	Switching Performance					
$F_{S\ max}$	Maximum Conversion Rate	IV	80	105		MSPS
$F_{S\ min}$	Minimum Conversion Rate			10	15	MSPS
	Pipeline Delay	IV		7		Clocks
t_{AP}	Aperture delay, IP	V		0.9		ns
t_h	Output hold time, IP (0.1 – 0.8 pF load)	V		1		ns
t_d	Output delay time, IP (0.1 - 0.8 pF load)	V		2		ns
t_{AP}	Aperture delay, with bonding pad	V		1.0		ns
t_h	Output hold time, with bonding pad	V		1.0		ns
t_d	Output delay time, with bonding pad	V		4.0		ns
	Digital Inputs					
V_{IL}	Logic “0” voltage	IV			0.4	V
V_{IH}	Logic “1” voltage	IV	AV_{DD} –0.4			V
I_{IL}	Logic “0” current (V_I=V_{SS})	IV			±10	μA
I_{IH}	Logic “1” current (V_I=V_{DD})	IV			±10	μA
C_{IND}	Input Capacitance	IV		0.03	0.1	pF

(table continued on next page)

[1)] Requires 1ps clock source jitter, and 1.5ps total on-chip jitter.

[2)] See Figure 5.

	Digital Outputs					
V_{OL}	Logic "0" voltage (I = 2 mA)	IV		0.2	0.4	V
V_{OH}	Logic "1" voltage (I = 2 mA)	IV	85% OV_{DD}	90% OV_{DD}		V
	Power Supply					
V_{DD}	Supply voltage	V	1.6	1.8	2.0	V
I_{DD}	Supply current (except digital output)	IV		27.8		mA
V_{SS}	Supply voltage			GND		
P_D	Power dissipation (except digital output) (active 10 MSPS)	IV		12		mW
P_D	Power dissipation (except digital output) (active 30 MSPS)	IV		35		mW
P_D	Power dissipation (except digital output) Power Down Mode	IV		70		μW
P_D	Power dissipation (except digital output) Sleep Mode	IV		3		mW
P_D	Power dissipation (except digital output) Standby Mode	IV		12		mW
t_{start}	Start-up time from Power down			1.3		ms
t_{start}	Start-up time from Sleep mode			2		μs
t_{start}	Start-up time from Stand By			8		clock cycles
OV_{DD}	Output driver supply voltage		1.6	1.8	3.6	V
T	Junction operating temperature		-40		+125	°C

Table 2: Electrical specifications

Test Levels

Test Level I: 100% production tested at +25°C
Test Level II: 100% production tested at +25°C and sample tested at specified temperatures
Test Level III: Sample tested only
Test Level IV: Parameter is guaranteed by design and characterization testing
Test Level V: Parameter is typical value only
Test Level VI: 100% production tested at +25°C. Guaranteed by design and characterization testing for industrial temperature range

ABSOLUTE MAXIMUM RATINGS

Supply voltages

V_{DD}..... - 0.2V to +2.2V
OV_{DD}..... - 0.2V to 3.6V

Temperatures

Operating Temperature….-40 to +125°C
Storage Temperature.. - 65 to +125°C

Input voltages

Analog In ..... - 0.2V to V_{DD} + 0.2V
Digital In..... - 0.2V to 3.6V
REF_P..... - 0.2V to V_{DD} + 0.2V
REF_N ..... - 0.2V to V_{DD} + 0.2V
CLOCK..... - 0.2V to 3.6V

Note: Stress above one or more of the limiting values may cause permanent damage to the device.

PIN FUNCTIONS

Pin Name	Description
INP, INN	Differential input signal pins. Common mode voltage: V_{CMI} (See Electrical specifications)
REFP, REFN	Reference pins (output/bypass). Bypass with 300nF capacitors close to the pins. (See Application Information)
BSCALE(1:0)	Power consumption scaling (See Modes of operation)
OPM(1:0)	Operating mode and control pins. (See Modes of operation)
CLOCK	ADC Clock
VCM	Common mode voltage output
BITO[11:0]	Digital outputs (MSB to LSB)
OVR	Over-Range flag
EXTREF	Disables internal voltage references when high. External voltages must be applied to REFN and REFP.
VDD	Digital power
AVDD	Analog power
AVSS	Analog and digital ground

Table 3: Pin functions

IP BLOCK LAYOUT

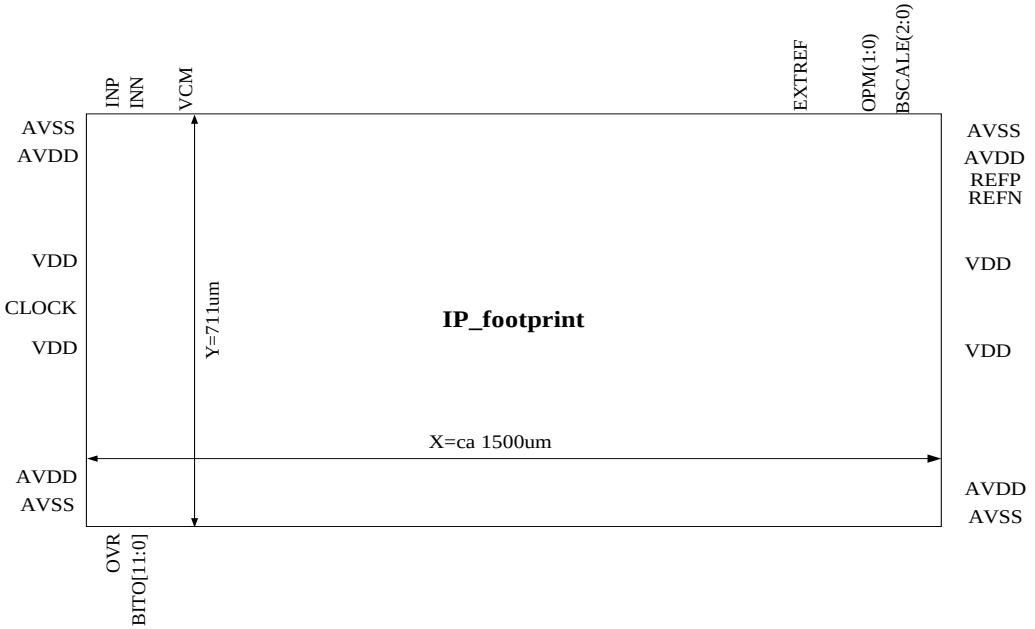

Figure 1: Size and pin placement for nAD1230-18 IP

FUNCTIONAL BLOCK DIAGRAM

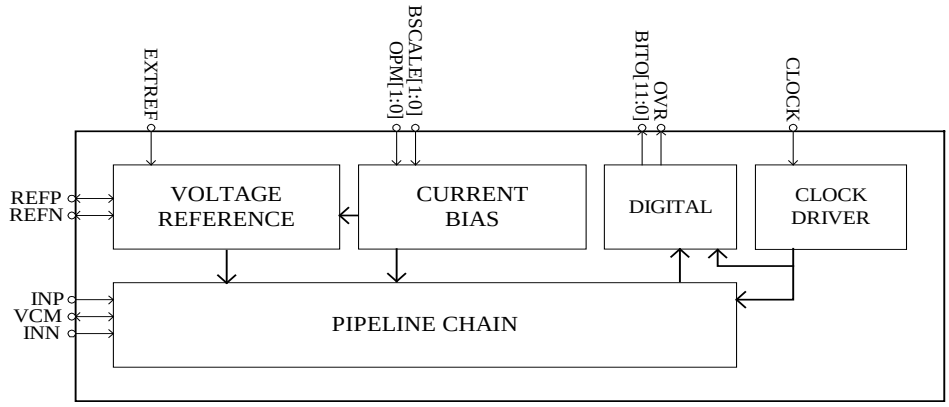

Figure 2: Functional Block diagram nAD1230-18

MODES OF OPERATION

The ADC has four different modes of operation, controlled as described in *Table 4*:

Mode of operation	**OPM control settings**	
	OPM[1]	**OPM[0]**
Active	HIGH	HIGH
Standby	HIGH	LOW
Sleep	LOW	HIGH
Power down	LOW	LOW

Table 4: Control settings for ADC operational modes

Active mode

In the active mode, the ADC is fully functional.
A performance versus power consumption trade off can be made by adding or subtracting 12.5% of the pipeline bias current with the bscale[1:0] bus:

BSCALE[1]	BSCALE[0]	CURRENT
1	0	-12.5%
0	1	+12.5%
1	1	Typical

Idle modes

In the three idle modes, the ADC is not functional. The different modes are distinguished primary by power consumption and start-up time. Start-up time is defined as the time it takes for the ADC to reach full performance in active mode when switched from an idle mode. Refer to 'Electrical Specifications' for power consumption and start-up times for the different modes.
While the start-up times for standby and sleep modes are constant, the start-up time in power down mode will be proportional to Off-Chip REFP,REFN decoupling. The amount of decoupling on the REFP and REFN will have impact on the performance (see Characterization report).

TIMING DIAGRAM

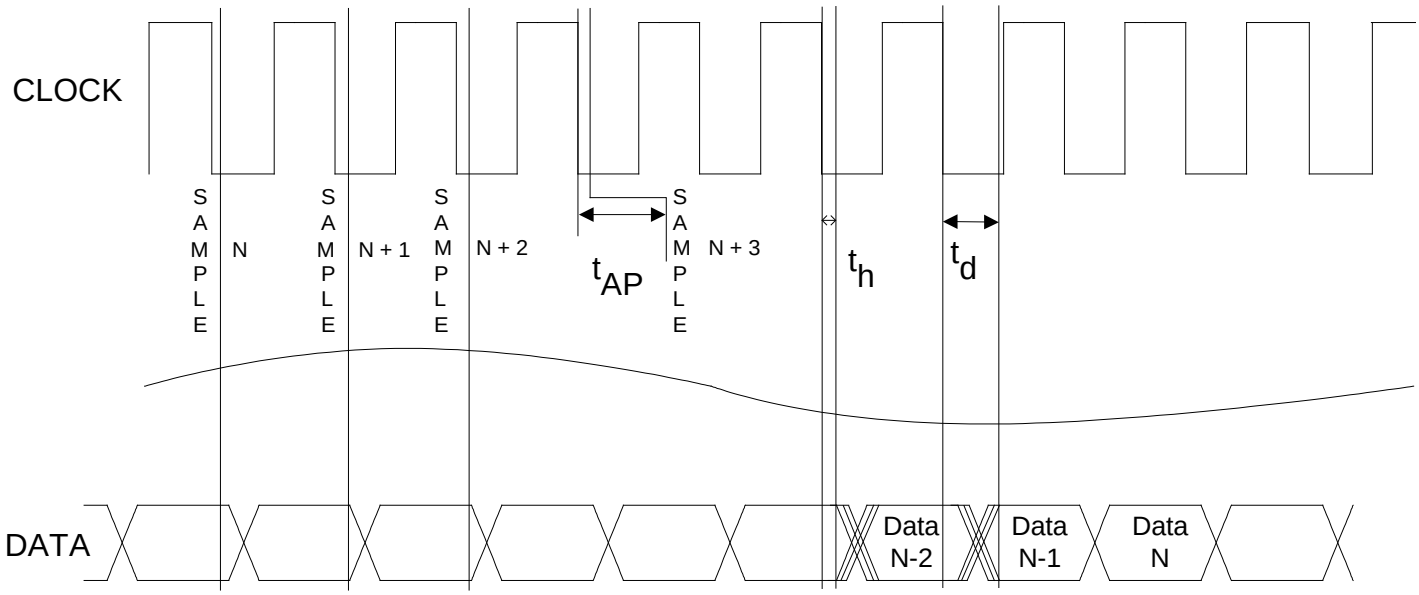

Figure 3: Timing diagram

INPUT SIGNAL RANGE

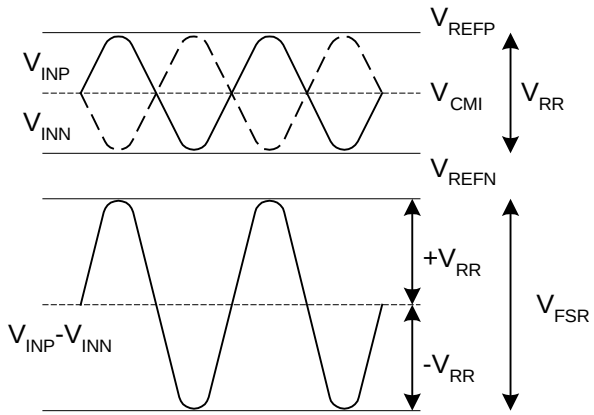

Figure 4: Definition of full scale range

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 5: Definitions

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

APPLICATION INFORMATION

References

The nAD1230-18 has a differential analog input. The input full scale range is equal to $\pm(V_{REFP}-V_{REFN})$ which is the voltage difference between the reference pins REFP and REFN. See *Figure 4* for details. Reference voltages are generated internally for a full scale range of ±0.75V. The reference voltages can be set externally by setting the EXTREF pin high. Use an appropriate operation amplifier to drive the voltages on pins REFP and REFN. A design example can be found in the Evaluation Board user Guide. Externally generated reference voltages connected to REFP and REFN should be symmetrical around 0.9V. The input full scale range can be defined between ±0.5V and ±0.75V. The references should be bypassed to ground as close to the converter pins as possible using at least 300nF capacitors in parallel with smaller capacitors (e.g. 1nF).

Analog input

The input of the nAD1230-18 can be configured in various ways - dependent upon whether a single ended or differential, AC- or DC-coupled input is wanted.

AC-coupled input is most conveniently implemented using a transformer with a center tapped secondary winding. The center tap is connected to the VCM pin as shown in figure 6. In order to obtain low distortion, it is important that the selected transformer does not exhibit core saturation at full-scale. Excellent results are obtained with the Mini Circuits T1-6T or T1-1T. Proper termination of the input is important for input signal purity. A small capacitor across the inputs attenuates kickback-noise from the sample and hold. Series resistors as shown in Figure 6 may be advantageous to improve linearity. The VCM-node should be bypassed to ground as closed to the converter pin as possible using 100nF capacitors in parallel with a small one.

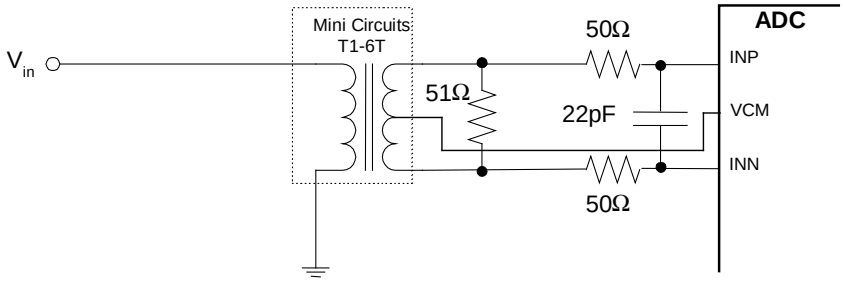

Figure 5: Example of AC coupled input using transformer configuration

If a DC-coupled single ended input is wanted, a solution based on operational amplifiers is usually preferred. Using the AD8138 single ended to differential amplifier gives excellent results. However, low cost operational amplifiers may be used if the requirements are less strict.

Clock

In order to preserve accuracy at high input frequency, it is important that the clock has low jitter and steep edges. Rise/fall times should be kept shorter than 2ns whenever

possible. Overshoot should be avoided. Low jitter is especially important when converting high frequency input signals. Jitter causes the noise floor to rise proportionally to input signal frequency. Jitter may be caused by crosstalk on the PCB. It is therefore recommended that the clock trace on the PCB is made as short as possible. Make sure that noise from the digital output bits does not couple into the clock power supply. The harmonic distortion of the ADC will in that case increase since the output bits are input signal dependent.
The SNR caused by clock jitter can be calculated by equation 1 where clock jitter is the only source of noise. This equation applies to any number of bits and sampling frequencies.

$$SNR = -20\log(2\pi \cdot f_{in} \cdot \varepsilon_{rms}) \quad (1)$$

ε_{rms} is the RMS value of the total system jitter measured in seconds. f_{in} is the input signal frequency.

Digital outputs

The digital output data appears in offset binary code at CMOS logic levels. Full-scale negative input results in output code 000...0. Full-scale positive input results in output code 111...1. Output data are available 6 clock cycles after the data are sampled. The analog input is sampled one aperture delay (t_{AP}) after the high to low clock transition. Output data should be sampled as shown in the timing diagram.

PCB layout and decoupling

A well designed PCB is necessary to get good spectral purity from any high performance ADC. A multilayer PCB with a solid ground plane is recommended for optimum performance. If the system has a split analog and digital ground plane, it is recommended that all ground pins on the ADC are connected to the analog ground plane. It is our experience that this gives the best performance. The power supply pins should be bypassed using 100nF in parallel with 1nF surface mounted capacitors as close to the package pins as possible. Analog and digital supply pins should be separately filtered.

Dynamic testing

Careful testing using high quality instrumentation is necessary to achieve accurate test results on high speed A/D-converters. It is important that the clock source and signal source has low jitter. A spectrally pure, low noise RF signal generator - such as the HP8662A or HP8644B is recommended for the test signal. Low pass filtering or band pass filtering of the input signal is usually necessary to obtain the required spectral purity (SFDR > 75dB). The clock signal can be obtained from either a crystal oscillator or a low-jitter pulse generator. Alternatively, a low-jitter RF-generator can be used as a clock source. At Nordic VLSI, the Marconi Instruments 2041A is used. The most consistent results are obtained if the clock signal is phase locked to the input signal. Phase locking allows testing without windowing of output data. A logic analyzer with deep memory - such as the HP16500-series, is recommended for test data acquisition.

DESIGN CENTER

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ORDERING INFORMATION

Type number	Description	Price
nAD1230-18-IC	nAD1230-18 sample in SSOP28 package (limited availability)	USD 50
nAD1230-18-EVB	nAD1230-18 evaluation board including characterisation report and user guide	USD 300

Table 6: Ordering information

Product Specification. Revision Date: October 15th, 2002