National Semiconductor

PRELIMINARY
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PC87308VUL SuperI/O Enhanced Sidewinder Plug and Play Compatible Chip, with a Floppy Disk Controller, a Keyboard Controller, a Real-Time Clock, Two UARTs, Full Infrared Support and an IEEE 1284 Parallel Port

General Description

The PC87308VUL is a single chip solution to the most commonly used ISA, EISA and Micro Channel peripherals. It incorporates in one fully Plug and Play (PnP) compatible chip, a Floppy Disk Controller (FDC), a Keyboard and mouse Controller (KBC), a Real-Time Clock (RTC), two full function UARTs, Universal Infrared (UIR) support, a full IEEE 1284 parallel port, three general purpose chip select signals that can be programmed for game port control, and a separate configuration register set for each module. It also provides support for power management and standard AT® address decoding for on-chip functions.

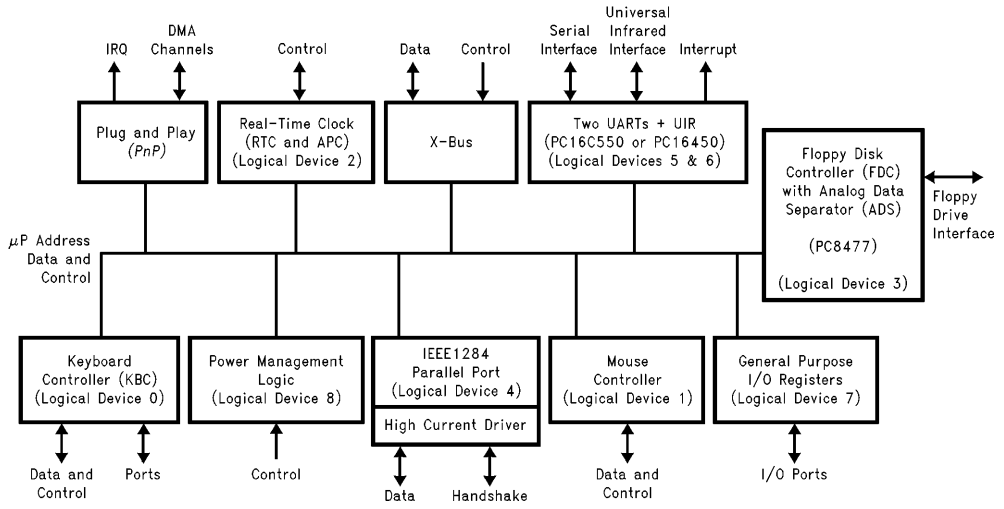
The PC87308VUL's Plug and Play (PnP) support conforms with the ''Plug and Play ISA Specification'' Version 1.0a, May 5, 1994.

The Universal Infrared (UIR) interface complies with the HP-SIR, SHARP-IR and IrDA-2 standards and supports all four basic protocols for TV remote circuitry (RC-5, RC-5 extended, RECS80 and NEC).

Features

- 100% compatibility with Plug and Play requirements specified in the ''Plug and Play ISA Specification'', ISA, EISA, and Micro Channel architectures. (Continued)

Block Diagram



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Features (Continued)

- A special Plug and Play module that includes;
  - — Flexible IRQs, DMAs and base addresses that meet the Plug and Play requirements of Microsoft's 1995 hardware design guide for Windows and Plug and Play ISA Revision 1.0A.
  - — Plug and Play ISA mode (with isolation mechanism—Wait for Key state)
  - — Motherboard Plug and Play mode
- A Floppy Disk Controller (FDC) that provides:
  - — A modifiable address that is referenced by a 16-bit programmable register
  - — Software compatibility with the PC8477, which contains a superset of the floppy disk controller functions in the μDP8473, the NEC μPD765A and the N82077
  - — 13 IRQ channel options
  - — Four 8-bit DMA channel options
  - — 16-byte FIFO
  - — Burst and non-burst modes
  - — A high-performance, internal, analog data separator that does not require any external filter components
  - — Support or standard 5.25″ and 3.5″ floppy disk drives
  - — Automatic media sense support
  - — Perpendicular recording drive support
  - — 3-mode Floppy Disk Drive (FDD) support
  - — Full support for IBM's® Tape Drive Register (TDR) implementation of PC-AT® and PS/2® drive types
- A Keyboard and Mouse Controller (KBC) with:
  - — A modifiable address that is referenced by a 16-bit programmable register, reported as a fixed address in resource data
  - — 13 IRQ options for the keyboard controller
  - — 13 IRQ options for the mouse controller
  - — An 8-bit microcontroller
  - — Software compatibility with the 8042AH and PC87911 microcontrollers
  - — 2 KB of custom-design program ROM
  - — 256 bytes of RAM for data
  - — 5 programmable dedicated open drain I/O lines for keyboard controller applications
  - — Asynchronous access to two data registers and one status register during normal operation
  - — Support for both interrupt and polling
  - — 93 instructions
  - — An 8-bit timer/counter
  - — Support for binary and BCD arithmetic
  - — Operation at 8 MHz, 12 MHz or 16 MHz (programmable option)
  - — Customizability using the PC87323VUL, which includes a RAM KBC, as a development platform for keyboard controller code for the PC87308VUL
- A Real-Time Clock (RTC) that has:
  - — A modifiable address that is referenced by a 16-bit programmable register
  - — 13 IRQ options with programmable polarity
  - — DS1287, MC146818 and PC87911 compatibility
  - — 242 bytes of battery backed up CMOS RAM in two banks
  - — Selective lock mechanism for the RTC RAM
  - — Battery backup up Century calendar in days, days of the week, months and years, with automatic leap-year adjustment
  - — Battery backed-up time of day in seconds, minutes and hours that allows a 12 or 24 hour format and adjustments for daylight savings time
  - — BCD or binary format for time keeping
  - — Three different maskable interrupt flags:
    - Periodic interrupts—At intervals from 122 μs to 500 ms
    - Time-of-day alarm—At intervals from once per second to once per day
    - Updated Ended Interrupt—Once per second upon completion of update
  - — Separate battery pin, 2.4V operation that includes an internal UL protection resistor
  - — 2 μA maximum power consumption during power down
  - — Double-buffer time registers
- An Advanced Power supply Control (APC) that controls the main power supply to the system, using open-drain output, as follows:
  Power turned on when:
  - — The RTC reaches a pre-determined date and time.
  - — A high to low transition occurs on the $\overline{RI}$ input signals of the UARTs.
  - — A ring pulse or pulse train is detected on the $\overline{RING}$ input signal.
  - — A SWITCH input signal indicates a Switch On event.

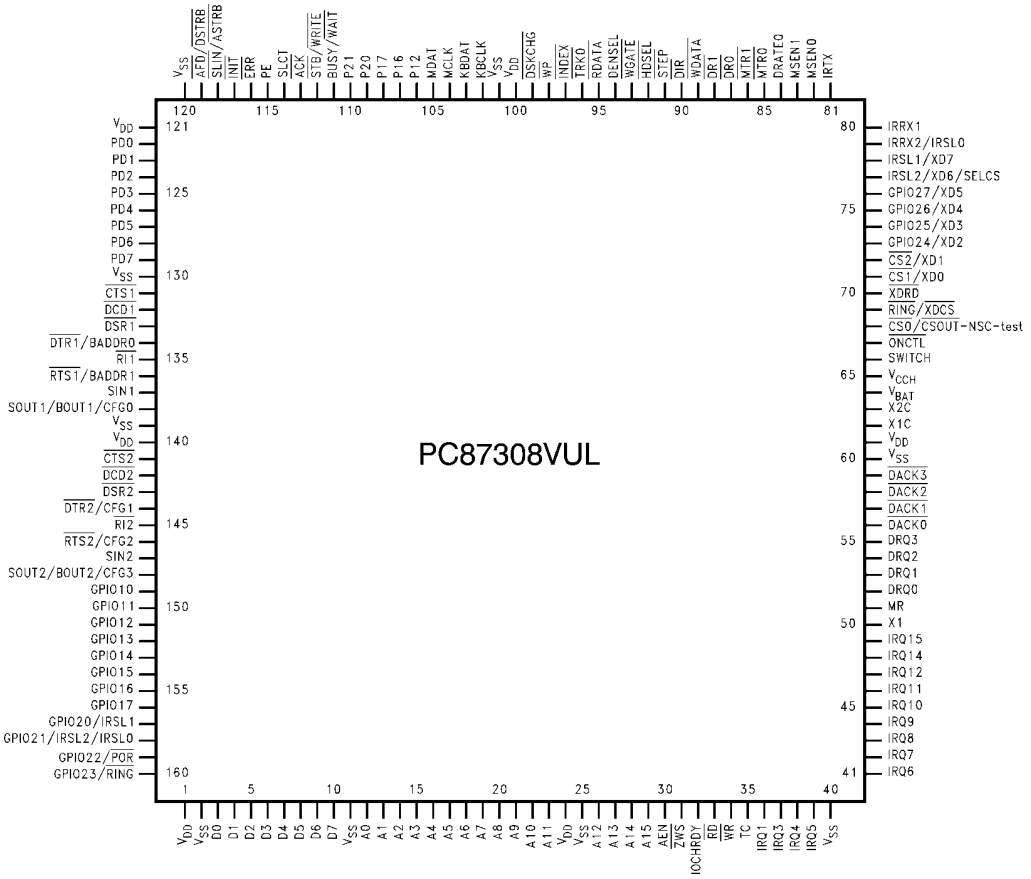
  Power turned off when:
  - — A SWITCH input signal indicates a Switch Off event.
  - — A Fail-safe event occurs (power-save mode detected but the system is hung up).
  - — Software turns power off.
- Two UARTs that provide:
  - — Software compatibility with the PC16550A and the PC16450
  - — A modifiable address that is referenced by a 16-bit programmable register
  - — 13 IRQ channel options
  - — Shadow register support for write-only bits
  - — Four 8-bit DMA options for UART2
- A Universal Infrared (UIR) interface on UART2 that supports TV remote circuitry and is compliant with:
  - — IrDA-2, including support for 4 Mbps and 1.15 Mbps baud rates
  - — HP-SIR
  - — ASK-IR option of SHARP-IR
  - — DASK-IR option of SHARP-IR
  - — Consumer remote control (TV Remote) mode

Features (Continued)

- A bidirectional parallel port that includes:
  - — A modifiable address that is referenced by a 16-bit programmable register
  - — Software or hardware control
  - — 13 IRQ channel options
  - — Four 8-bit DMA channel options
  - — Demand mode DMA support
  - — An Enhanced Parallel Port (EPP) that is compatible with the new version EPP 1.9, and is IEEE 1284 compliant
  - — An Enhanced Parallel Port (EPP) that also supports version EPP 1.7 of the Xircom specification.
  - — Support for an Enhanced Parallel Port (EPP) as mode 4 of the Extended Capabilities Port (ECP)
  - — An Extended Capabilities Port (ECP) that is IEEE 1284 compliant, including level 2
  - — Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
  - — Reduction of PCI bus utilization by supporting a demand DMA mode mechanism and a DMA fairness mechanism
  - — A protection circuit that prevents damage to the parallel port when a printer connected to it powers up or is operated at high voltages
  - — Output buffers that can sink and source 14 mA
- Three general purpose pins for three separate programmable chip select signals, as follows:
  - — Can be programmed for game port control
  - — The Chip Select 0 ($\overline{CS0}$) signal produces open drain output and is powered by the V_{CCH}
  - — The Chip Select 1 ($\overline{CS1}$) and 2 ($\overline{CS2}$) signals have push-pull buffers and are powered by the main V_{DD}
  - — Decoding of chip select signals depends on the address and the Address Enable (AEN) signals, and can be qualified using the Read ($\overline{RD}$) and Write ($\overline{WR}$) signals.
- 16 Single-Bit General Purpose I/O ports (GPIO):
  - — Modifiable addresses that are referenced by a 16-bit programmable reigster
  - — Programmable direction for each signal (input or output)
  - — Programmable drive type for each output pin (open-drain or push-pull)
  - — Programmable option for internal pull-up resistor on each input pin
  - — A back-drive protection circuit
- An X-bus data buffer that connects the 8-bit X data bus to the ISA data bus
- Clock source options:
  - — Source is a 32.768 kHz crystal-an internal frequency multiplier generates all the required internal frequencies
  - — Source may be either a 48 MHz or 24 MHz clock input signal
- Non-Volatile Memory (NVM) support via the Chip Select 0 ($\overline{CS0}$) signal that is powered by the V_{CCH}
- Enhanced Power Management, including:
  - — Special configuration registers for power down
  - — Reduced current leakage from pins
  - — Low-power CMOS technology
  - — Ability to shut off clocks to all modules
- General features include:
  - — All accesses to the SuperI/O chip activate a Zero Wait State ($\overline{ZWS}$) signal, except for accesses to the Enhanced Parallel Port (EPP) and to configuration registers
  - — Access to all configuration registers is through an Index and a Data register, which can be relocated within the ISA I/O address space
  - — 160-pin Plastic Quad Flatpack (PQFP) package

1.0 Pin Description

1.1 CONNECTION DIAGRAM



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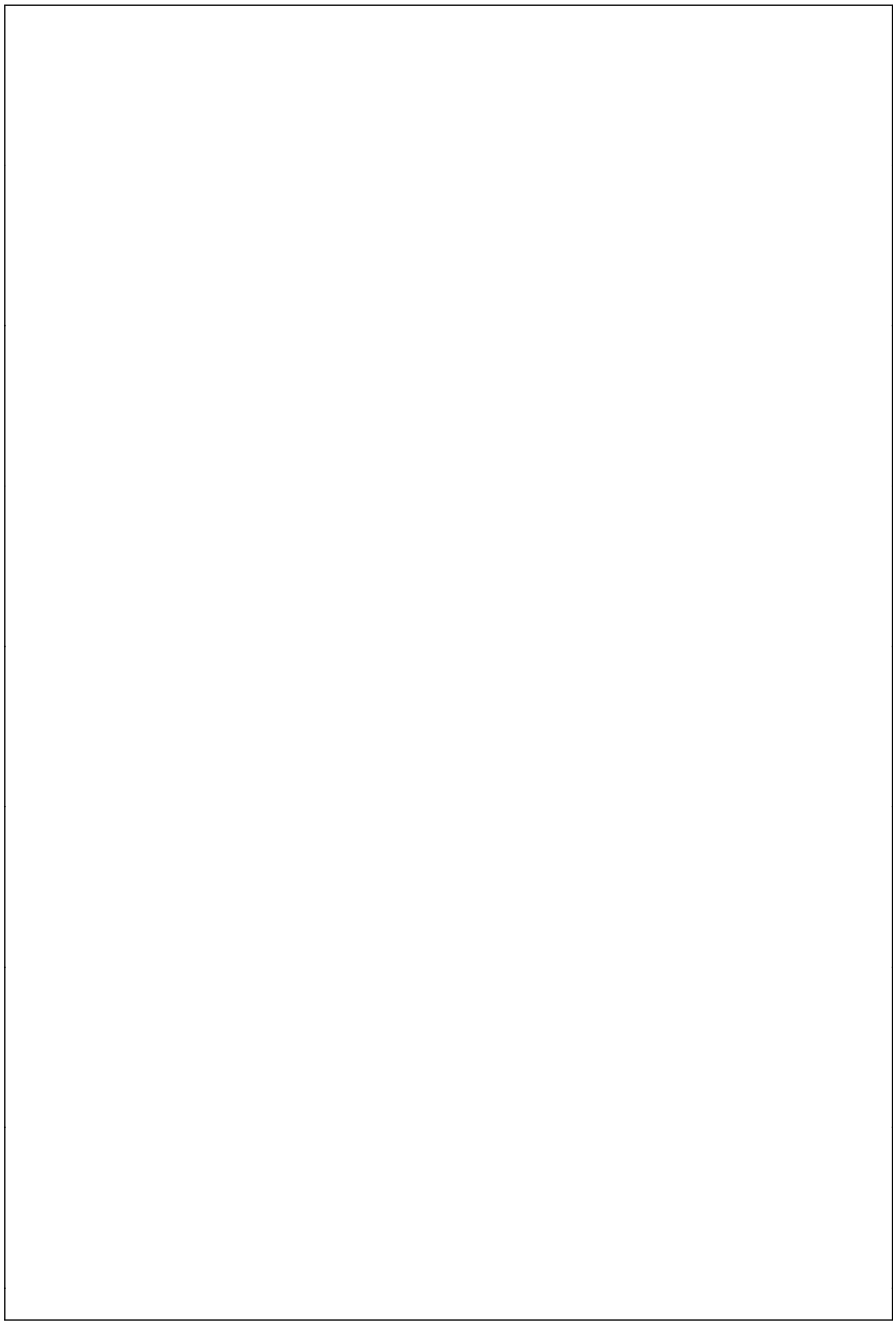
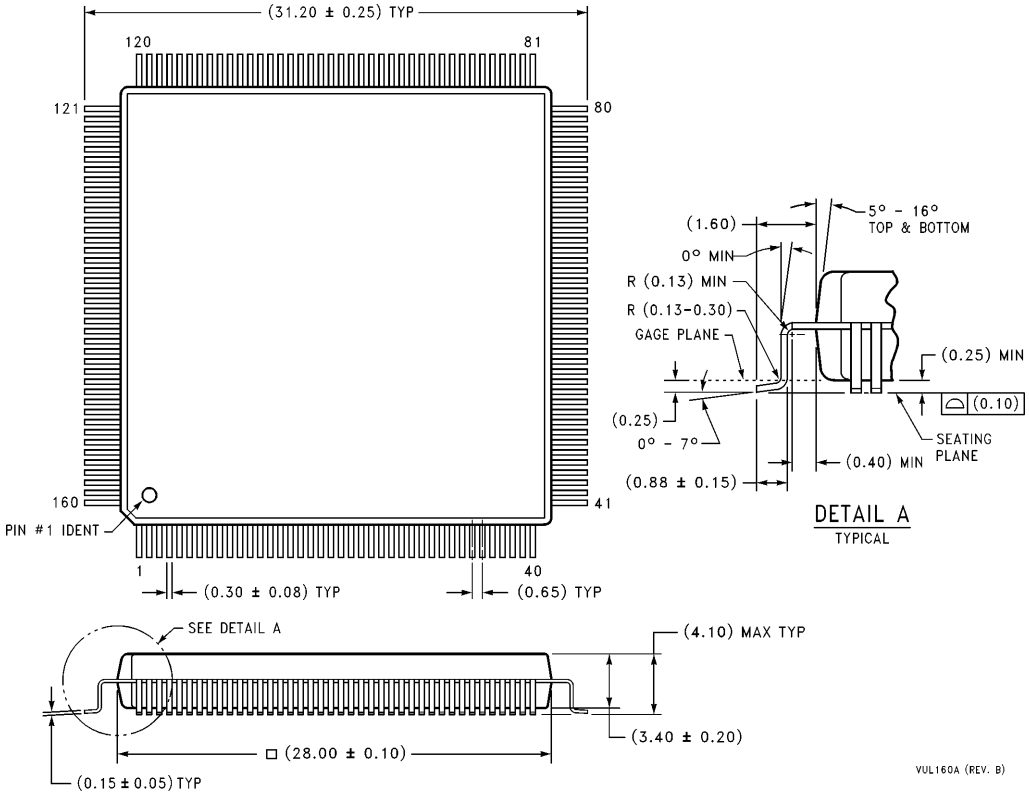


Physical Dimensions inches (millimeters)



Order Number PC87308VUL
NS Package VUL160A

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