

# CLC402

## Low-Gain Op Amp with Fast 14-Bit Settling

### General Description

The CLC402 is an operational amplifier designed for low-gain applications ( $\pm 1$  to  $\pm 8$ ), requiring fast, accurate settling and superior DC accuracy. Settling to 0.0025% in 25ns (32ns guaranteed over temperature), the CLC402 is ideal as the input amplifier in high accuracy (up to 14-bits) A/D systems. Unlike most other high-speed op amps, the CLC402 is free of thermally induced tails in the settling response.

The CLC402 is an upgrade to and pin compatible with the industry standard CLC400. Constructed using a unique, proprietary design and an advanced complementary bipolar process, it offers performance far beyond ordinary monolithic op amps. In addition, unlike many other high-speed op amps, the CLC402 offers both high performance and stability without the need for compensation circuitry – even at a gain of +1.

Supporting the CLC402's excellent pulse performance are improved DC characteristics. The CLC402's input offset voltage is typically 0.5mV and is guaranteed to be less than 1.6mV at +25°C. The input offset voltage drift is typically only  $3\mu\text{V}/^\circ\text{C}$ .

The CLC402 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC402AJP	-40°C to +85°C	8-pin plastic DIP
CLC402AJE	-40°C to +85°C	8-pin plastic SOIC
CLC402A8B	-55°C to +125°C	8-pin hermetic CERDIP, MIL-STD-833, Level B
CLC402ALC	-40°C to +85°C	dice
CLC402AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B

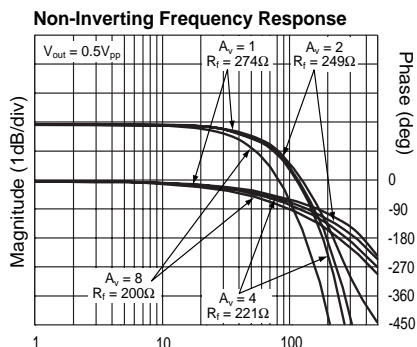
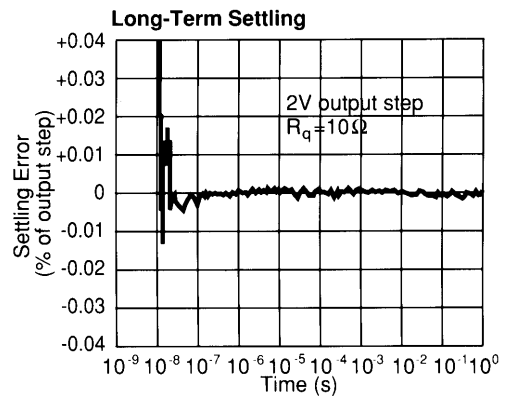
DESC SMD number: 5962-92033

### Features

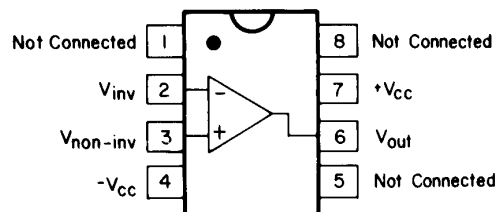
- 0.0025% settling in 25ns (32ns max)
- 0.5mV input offset voltage,  $3\mu\text{V}/^\circ\text{C}$  drift
- $\pm 1$  to  $\pm 8$  closed-loop gain range
- Low power, 150mW
- 0.01%/0.05° differential gain/phase

### Applications

- High-accuracy A/D systems (12-14 bits)
- High-accuracy D/A converters
- High-speed communications
- IF processors
- Video distribution



### Pinout DIP & SOIC



# CLC402 Electrical Characteristics ( $A_v = +2$ , $V_{cc} = \pm 5V$ , $R_L = 100\Omega$ , $R_f = 250\Omega$ ; unless specified)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS				UNITS	SYMBOL
			-40°C	+25°C	+85°C	+85°C		
Ambient Temperature	CLC402AJ	+25°C	-40°C	+25°C	+85°C			
<b>FREQUENCY DOMAIN PERFORMANCE</b>								
-3dB bandwidth	$V_{out} < 0.5V_{pp}$	195	>120	>130	>120	MHz	SSBW	
gain flatness <sup>2</sup>	$V_{out} < 5V_{pp}$	80	>50	>50	>50	MHz	LSBW	
peaking	$V_{out} < 0.5V_{pp}$	0	<0.4	<0.3	<0.4	dB	GFPL	
peaking	DC to 25MHz	0	<0.7	<0.5	<0.7	dB	GFPH	
rolloff	>25MHz	0.5	<1.0	<1.0	<1.0	dB	GFR	
linear phase deviation	DC to 50MHz	0.4	<1.2	<1.0	<1.2	°	LPD	
<b>TIME DOMAIN PERFORMANCE</b>								
rise and fall time	0.5V step	2.0	<2.9	<2.7	<2.9	ns	TRS	
	5V step	5.0	<8	<8	<8	ns	TRL	
settling time to $\pm 0.0025\%$	2V step	25	<32	<32	<32	ns	TS14	
$\pm 0.01\%$	2V step	18	<25	<25	<25	ns	TSP	
$\pm 0.1\%$	2V step	10	<15	<15	<15	ns	TSS	
overshoot	0.5V step	0	<10	<10	<10	%	OS	
slew rate		800	>500	>500	>500	V/ $\mu$ s	SR	
<b>DISTORTION AND NOISE PERFORMANCE</b>								
2nd harmonic distortion	2V <sub>pp</sub> , 20MHz	-50	<-38	<-43	<-43	dBc	HD2	
3rd harmonic distortion	2V <sub>pp</sub> , 20MHz	-60	<-53	<-53	<-50	dBc	HD3	
equivalent input noise								
noise floor	>1MHz	-157	<-155	<-155	<-155	dBm(1Hz)	SNF	
integrated noise	1MHz to 150MHz	40	<49	<49	<49	$\mu$ V	INV	
differential gain <sup>1</sup>		0.01	—	—	—	%	DG	
differential phase <sup>1</sup>		0.05	—	—	—	°	DP	
<b>STATIC, DC PERFORMANCE</b>								
*input offset voltage		0.5	<2.6	<1.6	<2.8	mV	VIO	
average temperature coefficient		3	<12	—	<12	$\mu$ V/°C	DVIO	
*input bias current	noninverting	10	<45	<25	<35	$\mu$ A	IBN	
average temperature coefficient		100	<250	—	<100	nA/°C	DIBN	
*input bias current	inverting	10	<50	<30	<40	$\mu$ A	IBI	
average temperature coefficient		100	<250	—	<100	nA/°C	DIBI	
power supply rejection ratio		68	>55	>60	>60	dB	PSRR	
common mode rejection ratio		65	>55	>60	>60	dB	CMRR	
*supply current	no load	15	<20	<20	<20	mA	ICC	
<b>MISCELLANEOUS PERFORMANCE</b>								
noninverting input	resistance	150	>50	>85	>85	k $\Omega$	RIN	
	capacitance	3.5	<5.5	<5.5	<5.5	pF	CIN	
output impedance	at DC	0.02	<0.1	<0.1	<0.1	$\Omega$	RO	
common mode input range		$\pm 3.0$	> $\pm 2.0$	> $\pm 2.5$	> $\pm 2.5$	V	CMIR	
output voltage range	no load	$\pm 3.5V$	> $\pm 3.0$	> $\pm 3.2$	> $\pm 3.2$	V	VO	
output current		$\pm 55$	> $\pm 25$	> $\pm 45$	> $\pm 45$	mA	IO	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

## Absolute Maximum Ratings

$V_{cc}$	$\pm 7V$
$I_{out}$	output is short circuit protected to ground, but, maximum reliability will be obtained if $I_{out}$ does not exceed...
	60mA
input voltage	$\pm V_{cc}$
junction temperature	+150°C
operating temperature range	
AJ:	-40°C to +85°C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10 sec
ESD rating (human body model)	2000V

## Miscellaneous Ratings

recommended gain range:	$\pm 1$ to $\pm 8$
<b>Notes:</b>	
* AJ	100% tested at +25°C.
note 1:	Differential gain and phase measured at $A_v = +2V$ , $R = 250\Omega$ , $R_L = 150\Omega$ , 1V <sub>pp</sub> equivalent video signal 0-100 IRE, 40 IRE <sub>pp</sub> , 0IRE = 0 volts, 75 $\Omega$ load and 3.58 MHz.

## Package Thermal Resistance

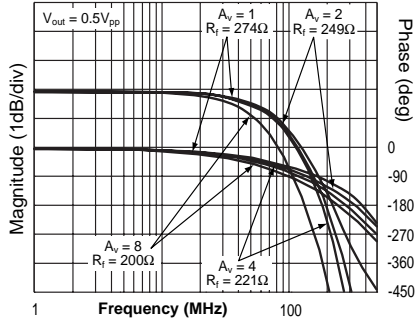
Package	$\theta_{JC}$	$\theta_{JA}$
AJP	70°C/W	125°C/W
AJE	65°C/W	145°C/W
CERDIP	45°C/W	135°C/W

## Reliability Information

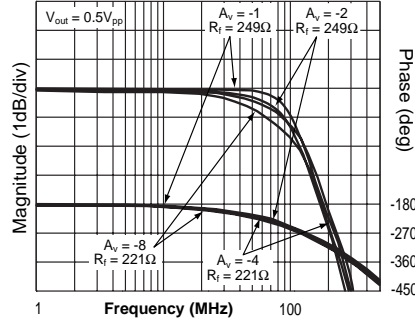
Transistor count	37
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# CLC402 Typical Performance Characteristics ( $\tau_A = 25^\circ$ , $A_V = +2$ , $V_{CC} = \pm 5V$ , $R_L = 100\Omega$ , $R_f = 250\Omega$ ; unless specified)

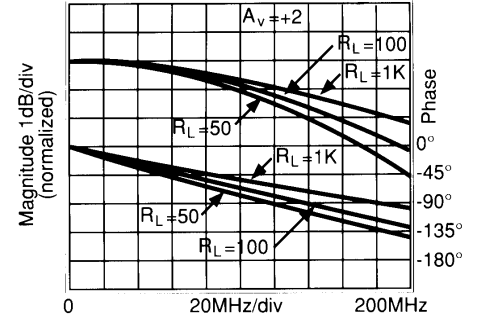
**Non-Inverting Frequency Response**



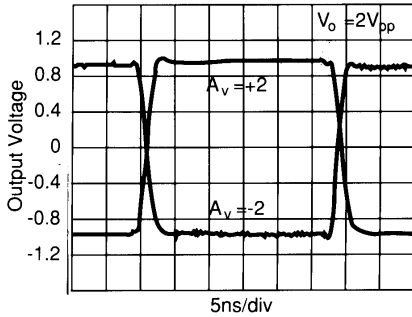
**Inverting Frequency Response**



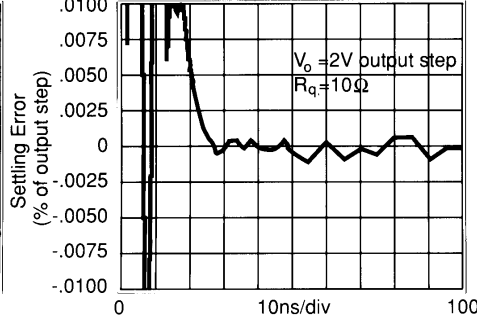
**Frequency Response vs. Load ( $R_L$ )**



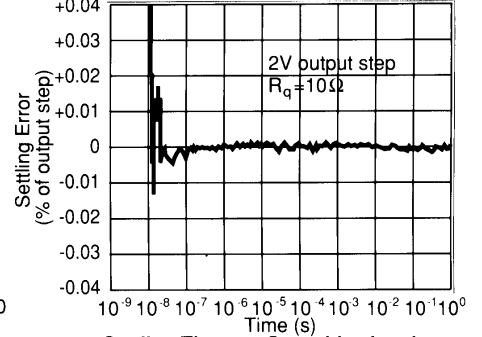
**Small Signal Pulse Response**



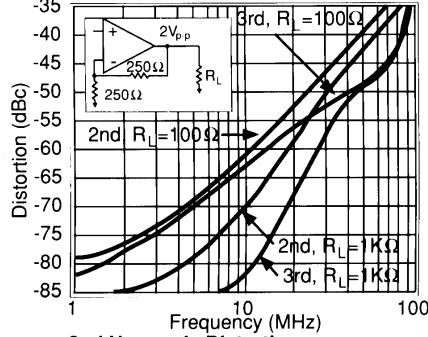
**Short Term Settling Response**



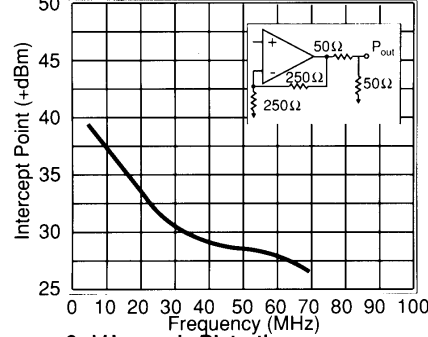
**Long-Term Settling**



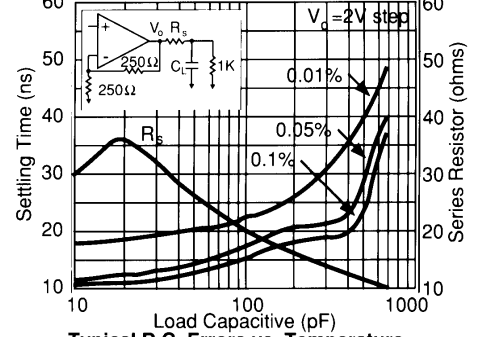
**Harmonic Distortion**



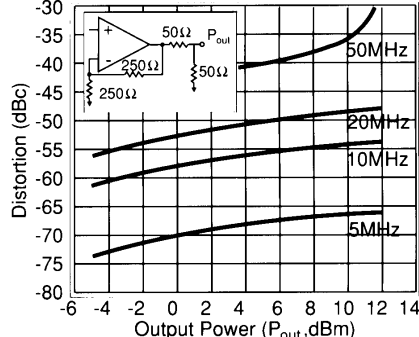
**2-Tone, 3rd Order Intermod. Intercept**



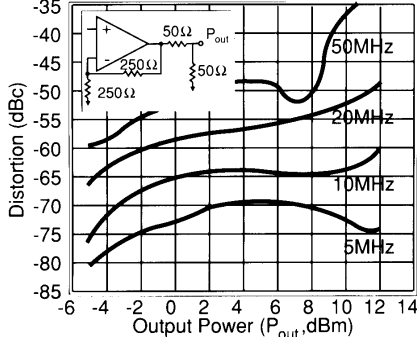
**Settling Time vs. Capacitive Load**



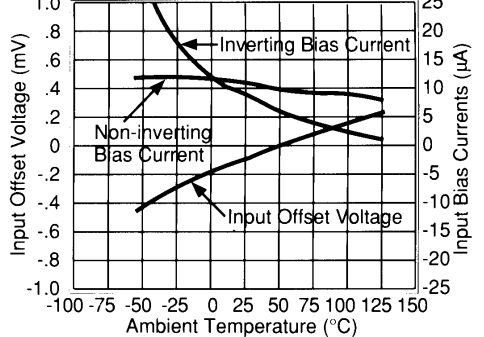
**2nd Harmonic Distortion**



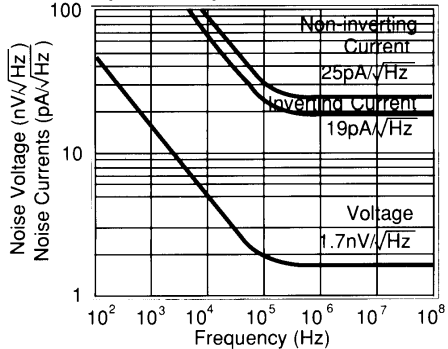
**3rd Harmonic Distortion**



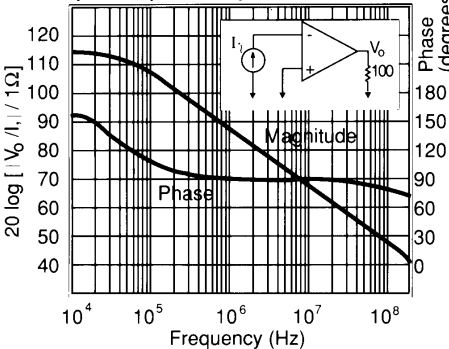
**Typical D.C. Errors vs. Temperature**



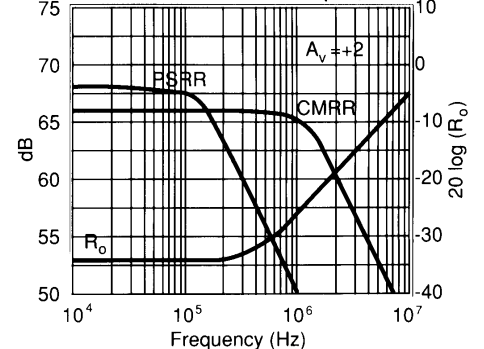
**Equivalent Input Noise**

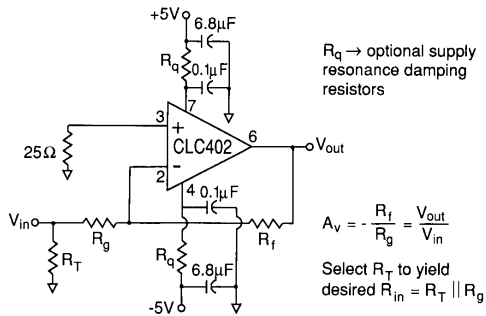


**Open-Loop Transimpedance Gain, Z(s)**



**CMRR, PSRR and Closed Loop  $R_o$**





**Figure 1: recommended inverting gain circuit**

**Feedback Resistor**

The CLC402 achieves its excellent pulse response by using the current feedback topology pioneered by Comlinear Corporation. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The CLC402 is optimized for use with a 250Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 discusses this in detail along with occasions where a different R<sub>f</sub> might be advantageous.

**Optimizing Settling Time**

The CLC402 is capable of extremely fast pulse settling times to very fine scale accuracies (.0025% in 25ns typical). It is also virtually free of any measurable thermal tail effects as shown in the long-term settling time plot on the previous page. Careful attention to parasitic effects is critical to achieving this level of performance.

Generally, open any ground and/or power planes around the device while providing an adjacent ground plane for the 0.1μF ceramic decoupling caps. These caps should be very near the power pins. Connecting the ground return point for the electrolytic capacitors near the load ground point is also very useful. Similarly, for non-inverting applications, connecting R<sub>g</sub> to ground near the input terminating resistor ground connection will improve performance. These suggestions become particularly pertinent for fastest settling to lower than 0.1% accuracies.

**Using Supply Resistors, R<sub>q</sub>**

Figures 1 and 2 show a series resistor in the supply leads between the electrolytic and ceramic capacitors. This optional resistor is intended to de-Q any self-resonance between those capacitors and the power supply trace inductance. Any large output voltage step into a significant load, either resistive or capacitive, will necessarily pull a current surge through the supply de-coupling capacitors. This can cause a very low level, high frequency ringing on the power supplies that may not be effectively rejected by the PSRR of the CLC402. This can, in turn, show up at the output as a ringing that will preclude high speed settling to very fine scale accuracies.

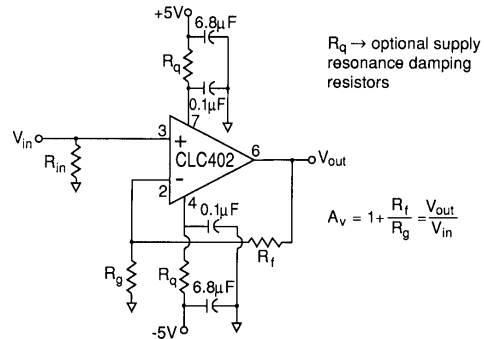
Adding R<sub>q</sub> will increase the amplitude of this signal at the supplies but will lower the frequency content to where the CLC402's PSRR can effectively reject it. An R<sub>q</sub> of 5 to 10Ω will yield excellent settling performance with minimal impact on other performance parameters.

**Driving Capacitive Loads**

Either parasitic or load capacitance directly on the output pin can quickly lead to unacceptable levels of ringing in the pulse response. Adding a series resistor, as shown in the plot of R<sub>s</sub> vs. C<sub>L</sub> on the previous page, will resolve this problem. Parasitic capacitances less than 2pF can be driven without the series resistor. See Application Note OA-15 for additional discussion.

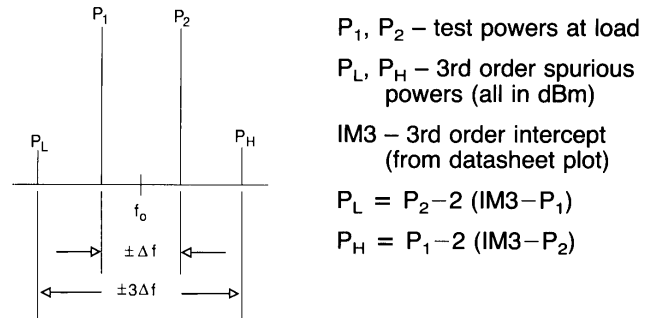
**Distortion Performance**

The distortion plots show the harmonic distortions and 3rd order intermodulation intercepts under a variety of load, power, and frequency conditions. Generally, going to higher



**Figure 2: recommended non-inverting gain circuit**

frequencies will degrade the distortion performance as the amplifier loop gain decreases. Further distortion improvements at low frequencies are observed when driving higher impedance loads. The 3rd order intermodulation intercept plot may be used to predict the 3rd order spurious levels given the power levels at the load for two closely spaced signal frequencies. Figure 3 shows the signal and spurious level definitions along with equations for predicting the spurious powers from the intercept value and the two signal powers.



**Figure 3: 3rd order spurious calculations**

**DC Accuracy and Noise**

The CLC402 offers an improved offset voltage over the comparable CLC400 low gain amplifier. The offset adjustment available on the CLC400 was therefore not included in this part. Figure 4 shows the output offset computational equation for the non-inverting configuration with an example using the typical bias current and offset specifications for Av = +2.

**Output Offset**

$$V_o = \left( \pm I_{bn} R_{in} \pm V_{io} \right) \left( 1 + \frac{R_f}{R_g} \right) \pm I_{bi} R_f$$

Example computation for Av = +2, R<sub>f</sub> = 250Ω

$$V_o = (\pm 10\mu A (50\Omega) \pm 0.5mV) (2) \pm 10\mu A (250\Omega) = \pm 3.5mV$$

**Figure 4: Output DC offset calculation**

This low output offset voltage is a marked improvement over earlier very high speed amplifiers. Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-7.

The equivalent input noise plot shows that the CLC402 offers a low 1.7nV/√Hz input noise voltage. A low non-inverting source impedance should be used for lowest noise performance due to the relatively high current noise at that input. See Application Note OA-12 for a full discussion of noise calculations for current feedback amplifiers.

**Printed Circuit Layout**

Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC402 are available. This board can be easily modified to include the R<sub>q</sub> resistors discussed above. Further layout suggestions may be found in Application Note OA-15.

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