N *ational Semiconductor*

74LVT16652
3.3V ABT 16-Bit Transceiver/Register
with TRI-STATE® Outputs

General Description

The LVT16652 consists of sixteen bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.
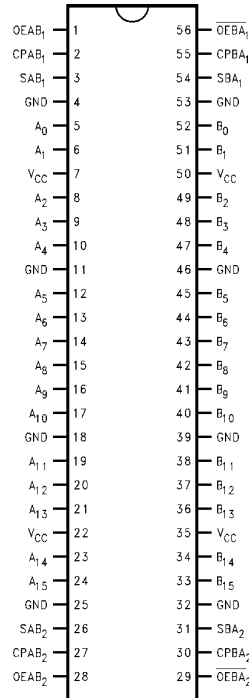
The transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16652 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

■ Input and output interface capability to systems at 5V V_{CC}

■ Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

■ Live insertion/extraction permitted

■ Power Up/Down high impedance provides glitch-free bus loading

■ Outputs source/sink -32 mA/$+64$ mA

■ Available in SSOP and TSSOP

■ Functionally compatible with the 74 series 16652

■ Latch-up performance exceeds 500 mA

Pin Names	Description
$A_0 - A_{16}$	Data Register A Inputs/ TRI-STATE Outputs
$B_0 - B_{16}$	Data Register B Inputs/ TRI-STATE Outputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
SAB_n, SBA_n	Select Inputs
$OEAB_n$, $\overline{OEBA}_n$	Output Enable Inputs

	SSOP EIAJ	TSSOP JEDEC
Order Number	74LVT16652MEA 74LVT16652MEAX	74LVT16652MTD 74LVT16652MTDX
NS Package Number	MS56A	MTD56

Connection Diagram

Pin Assignment for SSOP and TSSOP

$OEAB_1$	1	56	$\overline{OEBA}_1$
$CPAB_1$	2	55	$CPBA_1$
SAB_1	3	54	SBA_1
GND	4	53	GND
A_0	5	52	B_0
A_1	6	51	B_1
V_{CC}	7	50	V_{CC}
A_2	8	49	B_2
A_3	9	48	B_3
A_4	10	47	B_4
GND	11	46	GND
A_5	12	45	B_5
A_6	13	44	B_6
A_7	14	43	B_7
A_8	15	42	B_8
A_9	16	41	B_9
A_{10}	17	40	B_{10}
GND	18	39	GND
A_{11}	19	38	B_{11}
A_{12}	20	37	B_{12}
A_{13}	21	36	B_{13}
V_{CC}	22	35	V_{CC}
A_{14}	23	34	B_{14}
A_{15}	24	33	B_{15}
GND	25	32	GND
SAB_2	26	31	SBA_2
$CPAB_2$	27	30	$CPBA_2$
$OEAB_2$	28	29	$\overline{OEBA}_2$

TL/F/12024–1
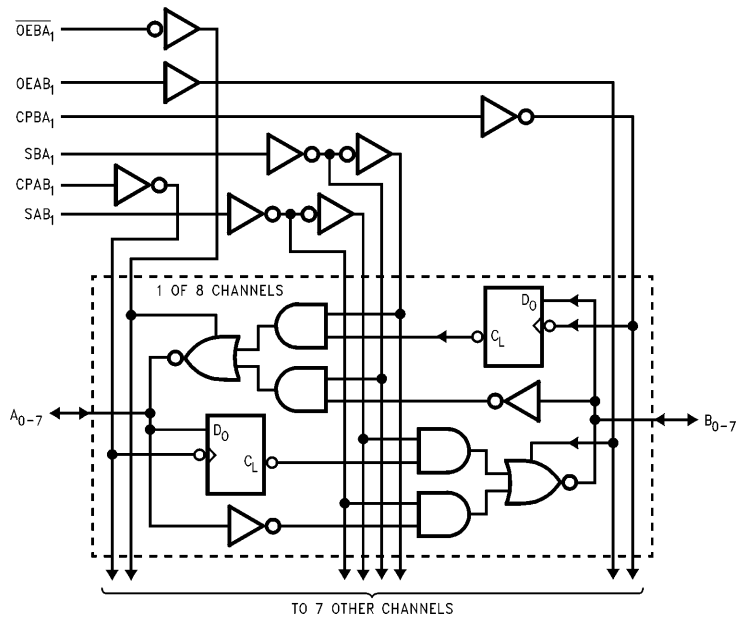
Logic Diagrams

TL/F/12024–2
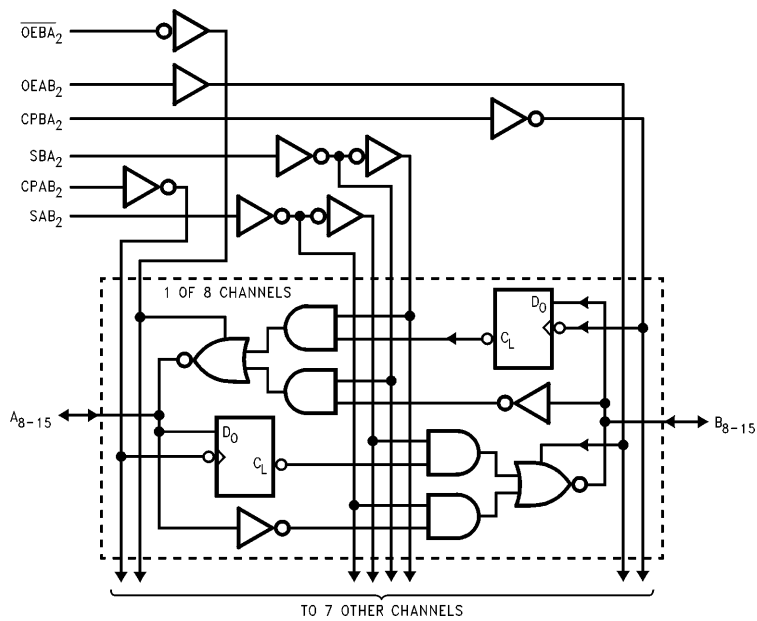
TL/F/12024–3

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB_n, SBA_n) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the LVT16652.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs ($CPAB_n$, $CPBA_n$) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling $OEAB_n$ and $\overline{OEBA}_n$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.
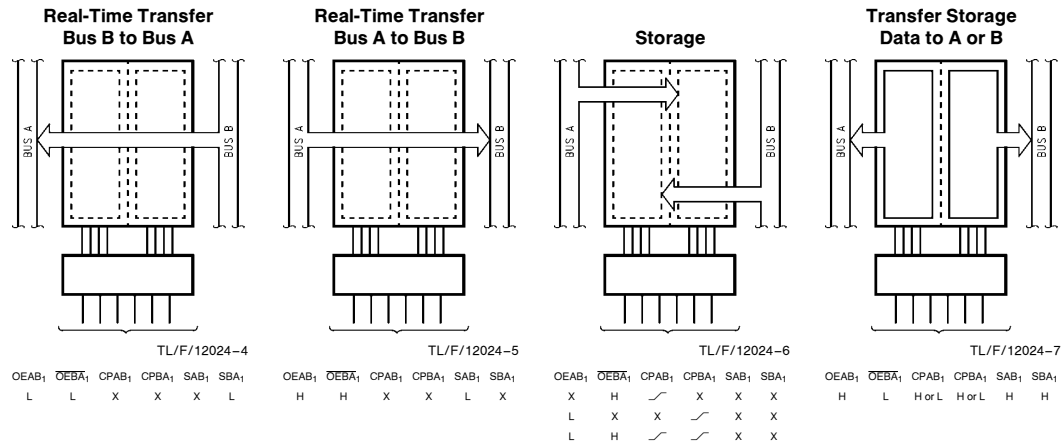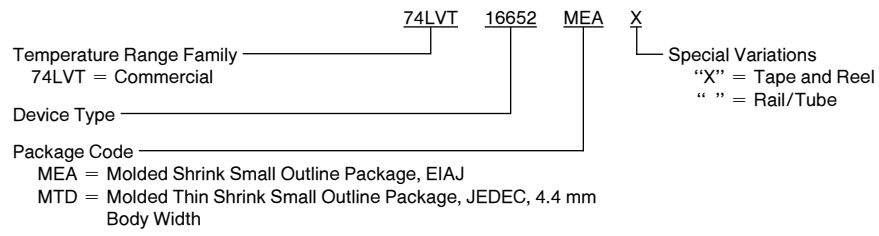
Real-Time Transfer Bus B to Bus A	Real-Time Transfer Bus A to Bus B	Storage	Transfer Storage Data to A or B

TL/F/12024–4 TL/F/12024–5 TL/F/12024–6 TL/F/12024–7

$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1
L	L	X	X	X	L

$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1
H	H	X	X	L	X

$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1
X	H	↗	X	X	X
L	X	X	↗	X	X
L	H	↗	↗	X	X

$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1
H	L	H or L	H or L	H	H

FIGURE 1

Truth Table (Note)

Inputs						Inputs/Outputs		Operating Mode
$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↗	↗	X	X	Input	Input	Store A and B Data
X	H	↗	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↗	↗	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↗	X	X	Not Specified	Input	Hold A, Store B
L	L	↗	↗	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level   L = LOW Voltage Level   X = Immaterial   ↗ = LOW to HIGH Clock Transition
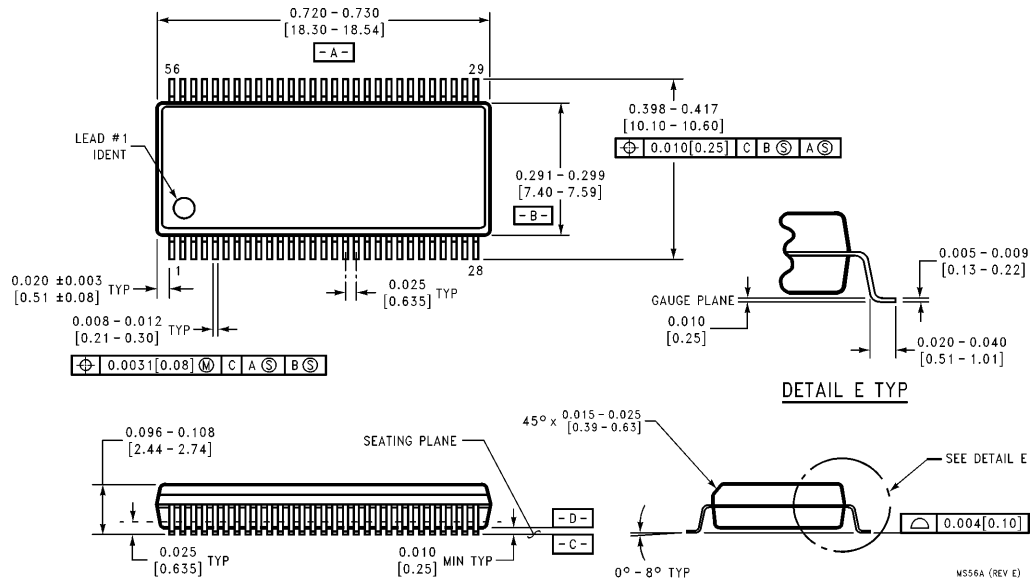
Note: The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs. This also applies to data I/O (A and B: 8–15) and #2 control pins.

74LVT16652 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:
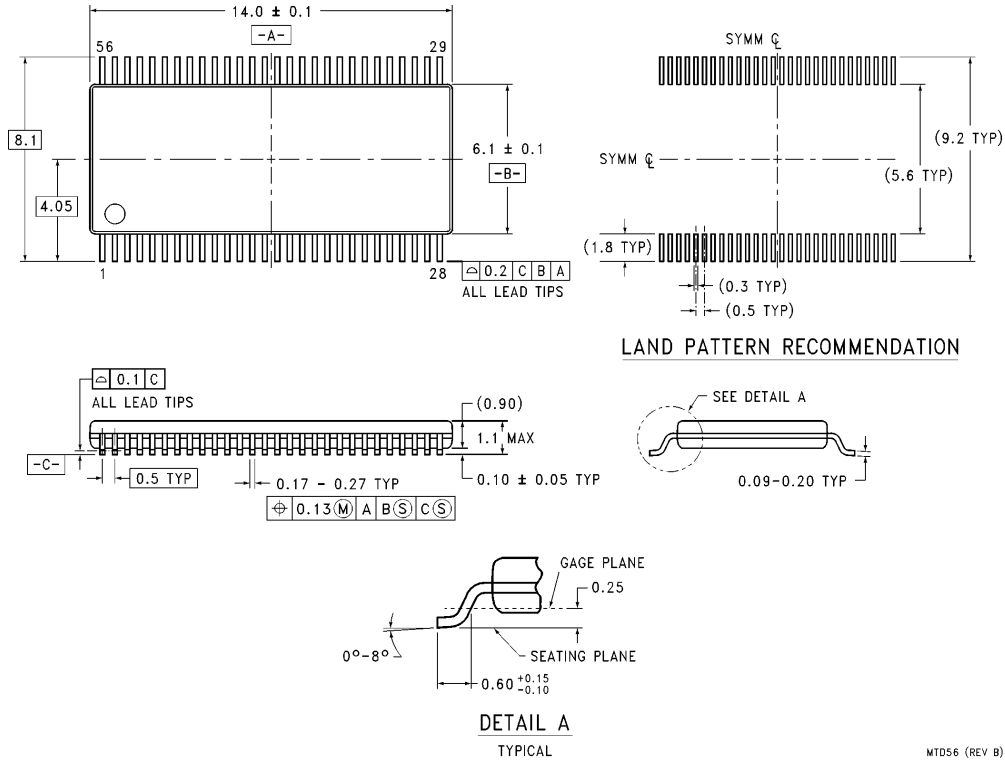
74LVT   16652   MEA   X

Temperature Range Family
    74LVT = Commercial

Device Type

Package Code
    MEA = Molded Shrink Small Outline Package, EIAJ
    MTD = Molded Thin Shrink Small Outline Package, JEDEC, 4.4 mm
        Body Width

Special Variations
    "X" = Tape and Reel
    " " = Rail/Tube

Physical Dimensions inches (millimeters) unless otherwise noted

0.720 – 0.730
[18.30 – 18.54]
– A –

56   29

LEAD #1
IDENT

0.398 – 0.417
[10.10 – 10.60]

⊕ 0.010[0.25] C B Ⓢ A Ⓢ

0.291 – 0.299
[7.40 – 7.59]
– B –

0.020 ±0.003
[0.51 ±0.08] TYP

1   28

0.025
[0.635] TYP

0.008 – 0.012
[0.21 – 0.30] TYP

⊕ 0.0031[0.08] Ⓜ C A Ⓢ B Ⓢ

0.005 – 0.009
[0.13 – 0.22]

GAUGE PLANE

0.010
[0.25]

0.020 – 0.040
[0.51 – 1.01]

DETAIL E TYP

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

45° x 0.015 – 0.025
[0.39 – 0.63]

SEE DETAIL E

– D –
– C –

0.025
[0.635] TYP

0.010
[0.25] MIN TYP

0° – 8° TYP

⊿ 0.004[0.10]

MS56A (REV E)

56-Lead Molded Shrink Small Outline Package, EIAJ
Order Number 74LVT16652MEA or 74LVT16652MEAX
NS Package Number MS56A

Physical Dimensions millimeters (Continued)

14.0 ± 0.1
-A-
56
29
8.1
6.1 ± 0.1
-B-
4.05
1
28
⌓ 0.2 C B A
ALL LEAD TIPS

SYMM ₵
SYMM ₵
(9.2 TYP)
(5.6 TYP)
(1.8 TYP)
(0.3 TYP)
(0.5 TYP)

LAND PATTERN RECOMMENDATION

⌓ 0.1 C
ALL LEAD TIPS
-C-
0.5 TYP
0.17 − 0.27 TYP
⌖ 0.13 Ⓜ A BⓈ CⓈ
(0.90)
1.1 MAX
0.10 ± 0.05 TYP

SEE DETAIL A
0.09−0.20 TYP

GAGE PLANE
0.25
0°–8°
SEATING PLANE
0.60 +0.15 −0.10

MTD56 (REV B)

DETAIL A
TYPICAL

56-Lead Molded Thin Shrink Small Outline Package, JEDEC, 6.1 mm Body Width
Order Number 74LVT16652MTD or 74LVT16652MTDX
NS Package Number MTD56

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