

54F/74F192

Up/Down Decade Counter with Separate Up/Down Clocks

General Description

The 'F192 is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Indi-

vidual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously override the clocks.

Features

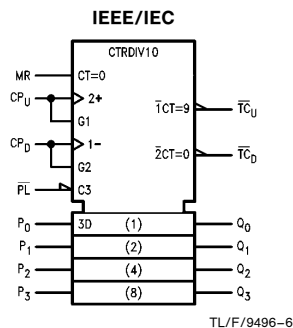
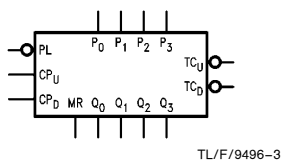
- Guaranteed 4000V minimum ESD protection

| Commercial | Military | Package Number | Package Description |
|-------------------|-------------------|----------------|---|
| 74F192PC | | N16E | 16-Lead (0.300" Wide) Molded Dual-In-Line |
| | 54F192DM (Note 2) | J16A | 16-Lead Ceramic Dual-In-Line |
| 74F192SC (Note 1) | | M16A | 16-Lead (0.150" Wide) Molded Small Outline, JEDEC |
| 74F192SJ (Note 1) | | M16D | 16-Lead (0.300" Wide) Molded Small Outline, EIAJ |
| | 54F192FM (Note 2) | W16A | 16-Lead Cerpack |
| | 54F192LM (Note 2) | E20A | 20-Lead Ceramic Leadless Chip Carrier, Type C |

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

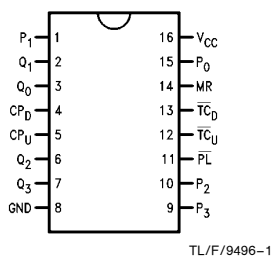
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMOB, FMOB and LMOB.

Logic Symbols

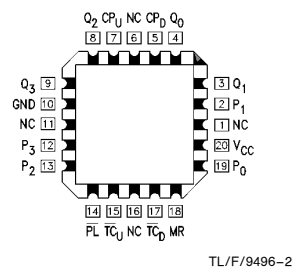


Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



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Unit Loading/Fan Out

| Pin Names | Description | 54F/74F | |
|--------------------------------|--|----------|---|
| | | U.L. | Input I _{IH} /I _{IL} |
| | | HIGH/LOW | Output I _{OH} /I _{OL} |
| CP _U | Count Up Clock Input (Active Rising Edge) | 1.0/3.0 | 20 μA/ -1.8 mA |
| CP _D | Count Down Clock Input (Active Rising Edge) | 1.0/3.0 | 20 μA/ -1.8 mA |
| MR | Asynchronous Master Reset Input (Active HIGH) | 1.0/1.0 | 20 μA/ -0.6 mA |
| PL | Asynchronous Parallel Load Input (Active LOW) | 1.0/1.0 | 20 μA/ -0.6 mA |
| P ₀ -P ₃ | Parallel Data Inputs | 1.0/1.0 | 20 μA/ -0.6 mA |
| Q ₀ -Q ₃ | Flip-Flop Outputs | 50/33.3 | -1 mA/20 mA |
| \overline{TC}_D | Terminal Count Down (Borrow) Output (Active LOW) | 50/33.3 | -1 mA/20 mA |
| \overline{TC}_U | Terminal Count Up (Carry) Output (Active LOW) | 50/33.3 | -1 mA/20 mA |

Functional Description

The 'F192 is an asynchronously presettable decade counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

The Terminal Count Up (\overline{TC}_U) and Terminal Count Down (\overline{TC}_D) outputs are normally HIGH. When the circuit has reached the maximum count state 9, the next HIGH-to-LOW transition of the Count Up Clock will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the \overline{TC}_D output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the \overline{TC} outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

The 'F192 has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load (\overline{PL}) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input (P₀-P₃) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or

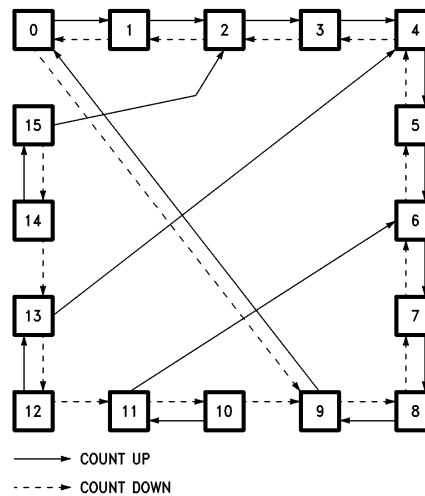
load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

Function Table

| MR | \overline{PL} | CP _U | CP _D | Mode |
|----|-----------------|-----------------|-----------------|----------------|
| H | X | X | X | Reset (Asyn.) |
| L | L | X | X | Preset (Asyn.) |
| L | H | H | H | No Change |
| L | H | ↗ | ↗ | Count Up |
| L | H | H | ↘ | Count Down |

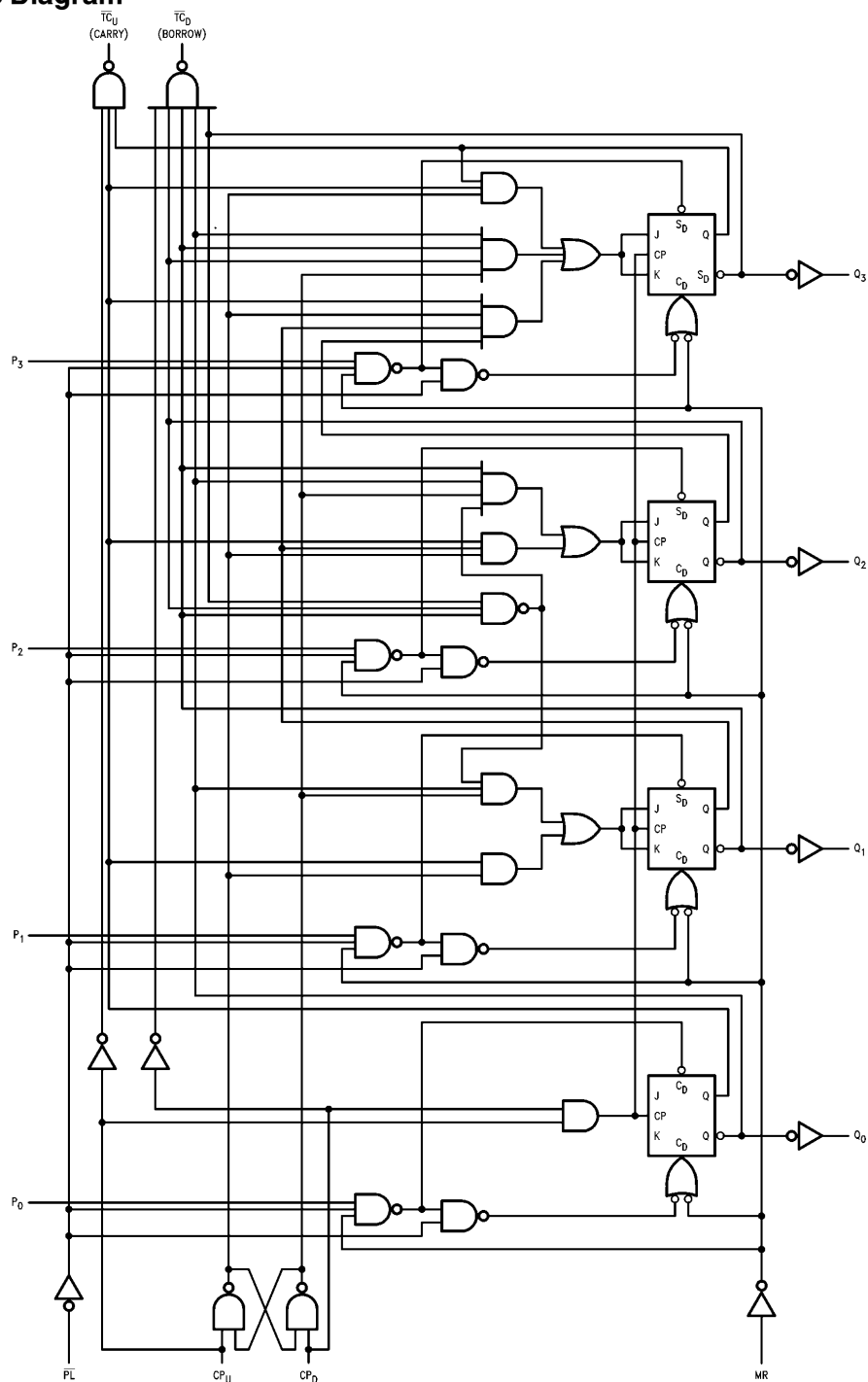
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Clock Transition

State Diagram



TL/F/9496-4

Logic Diagram



TL/F/9496-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|--------------------------|
| Storage Temperature | –65°C to +150°C |
| Ambient Temperature under Bias | –55°C to +125°C |
| Junction Temperature under Bias | –55°C to +175°C |
| Plastic | –55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | –0.5V to +7.0V |
| Input Voltage (Note 2) | –0.5V to +7.0V |
| Input Current (Note 2) | –30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | –0.5V to V _{CC} |
| TRI-STATE® Output | –0.5V to +5.5V |

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

| | |
|------------------------------|-----------------|
| Free Air Ambient Temperature | |
| Military | –55°C to +125°C |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Commercial | +4.5V to +5.5V |

DC Electrical Characteristics

| Symbol | Parameter | 54F/74F | | | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|--|-------------------|--------------|-------|-----------------|---|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | –1.2 | V | Min | I _{IN} = –18 mA |
| V _{OH} | Output HIGH Voltage | 54F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} | 2.5 2.5 2.7 | | V | Min | I _{OH} = –1 mA I _{OH} = –1 mA I _{OH} = –1 mA |
| V _{OL} | Output LOW Voltage | 54F 10% V _{CC} 74F 10% V _{CC} | | 0.5 0.5 | V | Min | I _{OL} = 20 mA I _{OL} = 20 mA |
| I _{IH} | Input HIGH Current | 54F 74F | | 20.0 5.0 | μA | Max | V _{IN} = 2.7V |
| I _{BVI} | Input HIGH Current Breakdown Test | 54F 74F | | 100 7.0 | μA | Max | V _{IN} = 7.0V |
| I _{CEX} | Output HIGH Leakage Current | 54F 74F | | 250 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 74F | 4.75 | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | 74F | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded |
| I _{IL} | Input LOW Current | | | –0.6 –1.8 | mA | Max | V _{IN} = 0.5V, Except CP _U , CP _D V _{IN} = 0.5V, CP _U , CP _D |
| I _{OS} | Output Short-Circuit Current | | –60 | –150 | mA | Max | V _{OUT} = 0V |
| I _{CCL} | Power Supply Current | | 38 | 55 | mA | Max | V _O = LOW |

AC Electrical Characteristics

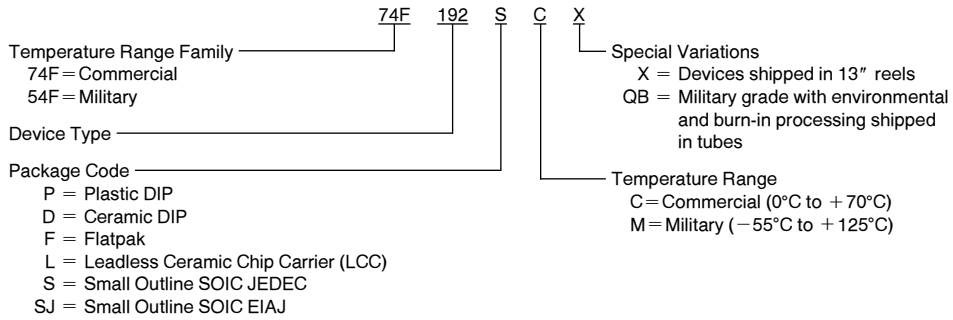
| Symbol | Parameter | 74F | | | 54F | | 74F | | Units |
|--------------------------------------|--|--|--------------|--------------|--|--------------|--|--------------|-------|
| | | $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ | | | $T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$ | | $T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$ | | |
| | | Min | Typ | Max | Min | Max | Min | Max | |
| f_{max} | Maximum Clock Frequency | 100 | 125 | | 75 | | 90 | | MHz |
| t_{PLH} t_{PHL} | Propagation Delay CP_U or CP_D to \overline{TC}_U or \overline{TC}_D | 4.0 3.5 | 7.0 6.0 | 9.0 8.0 | 4.0 3.5 | 10.5 9.5 | 4.0 3.5 | 10.0 9.0 | ns |
| t_{PLH} t_{PHL} | Propagation Delay CP_U or CP_D to Q_n | 4.0 5.5 | 6.5 9.5 | 8.5 12.5 | 4.0 5.5 | 10.0 14.0 | 4.0 5.5 | 9.5 13.5 | ns |
| t_{PLH} t_{PHL} | Propagation Delay P_n to Q_n | 3.0 6.0 | 4.5 11.0 | 7.0 14.5 | 3.0 6.0 | 8.5 16.5 | 3.0 6.0 | 8.0 15.5 | ns |
| t_{PLH} t_{PHL} | Propagation Delay PL to Q_n | 5.0 5.5 | 8.5 10.0 | 11.0 13.0 | 5.0 5.5 | 13.5 15.0 | 5.0 5.5 | 12.0 14.0 | ns |
| t_{PHL} | Propagation Delay MR to Q_n | 6.5 | 11.0 | 14.5 | 6.5 | 16.0 | 6.5 | 15.5 | ns |
| t_{PLH} | Propagation Delay MR to \overline{TC}_U | 6.0 | 10.5 | 13.5 | 6.0 | 15.0 | 6.0 | 14.5 | |
| t_{PHL} | Propagation Delay MR to \overline{TC}_D | 7.0 | 11.5 | 14.5 | 7.0 | 16.0 | 7.0 | 15.5 | |
| t_{PLH} t_{PHL} | Propagation Delay PL to \overline{TC}_U or \overline{TC}_D | 7.0 7.0 | 12.0 11.5 | 15.5 14.5 | 7.0 7.0 | 18.5 17.5 | 7.0 7.0 | 16.5 15.5 | ns |
| t_{PLH} t_{PHL} | Propagation Delay P_n to \overline{TC}_U or \overline{TC}_D | 7.0 6.5 | 11.5 11.0 | 14.5 14.0 | 7.0 6.5 | 16.5 16.5 | 7.0 6.5 | 15.5 15.0 | ns |

AC Operating Requirements

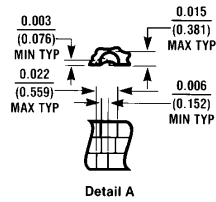
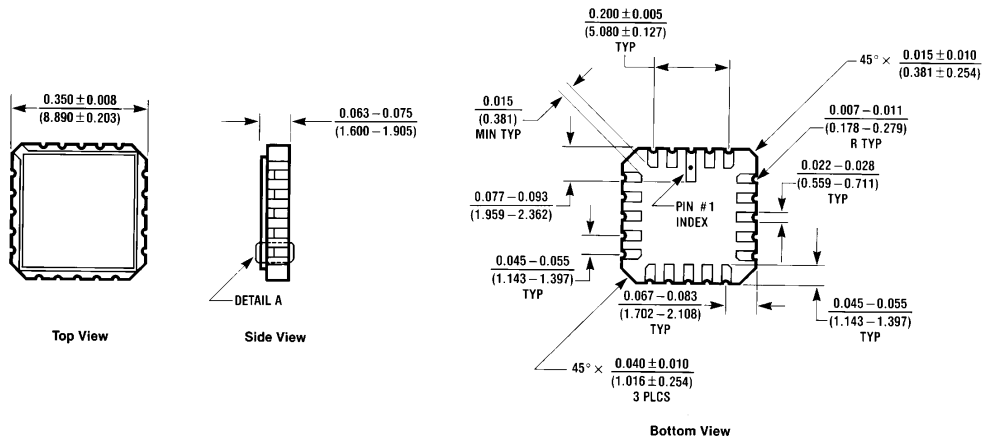
| Symbol | Parameter | 74F | | 54F | | 74F | | Units |
|----------------------|---|--|-----|----------------------------|-----|----------------------------|-----|-------|
| | | $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ | | $T_A, V_{CC} = \text{Mil}$ | | $T_A, V_{CC} = \text{Com}$ | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_s(H)$ $t_s(L)$ | Setup Time, HIGH or LOW P_n to \overline{PL} | 4.5 4.5 | | 6.0 6.0 | | 5.0 5.0 | | ns |
| $t_h(H)$ $t_h(L)$ | Hold Time, HIGH or LOW P_n to \overline{PL} | 2.0 2.0 | | 2.0 2.0 | | 2.0 2.0 | | |
| $t_w(L)$ | \overline{PL} Pulse Width, LOW | 6.0 | | 7.5 | | 6.0 | | ns |
| $t_w(L)$ | CP_U or CP_D Pulse Width, LOW | 5.0 | | 7.0 | | 5.0 | | ns |
| $t_w(L)$ | CP_U or CP_D Pulse Width, LOW (Change of Direction) | 10.0 | | 12.0 | | 10.0 | | ns |
| $t_w(H)$ | \overline{MR} Pulse Width, HIGH | 6.0 | | 6.0 | | 6.0 | | ns |
| t_{rec} | Recovery Time \overline{PL} to CP_U or CP_D | 6.0 | | 8.0 | | 6.0 | | ns |
| t_{rec} | Recovery Time MR to CP_U or CP_D | 4.0 | | 4.5 | | 4.0 | | ns |

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

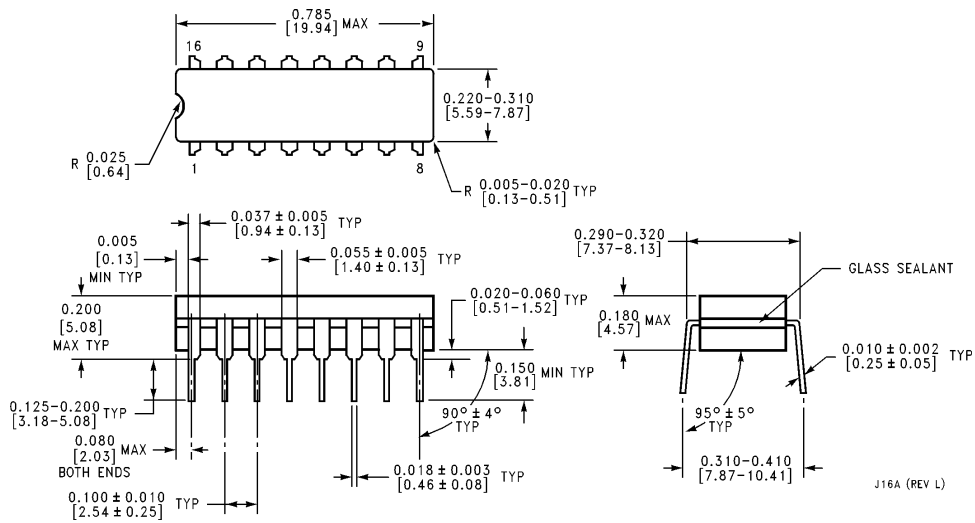


Physical Dimensions inches (millimeters)



20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

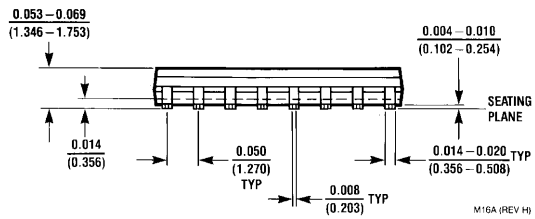
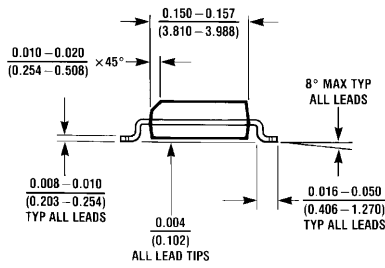
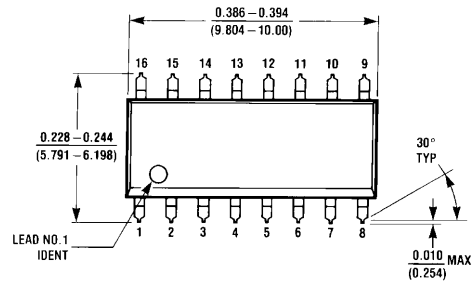
E20A (REV D)



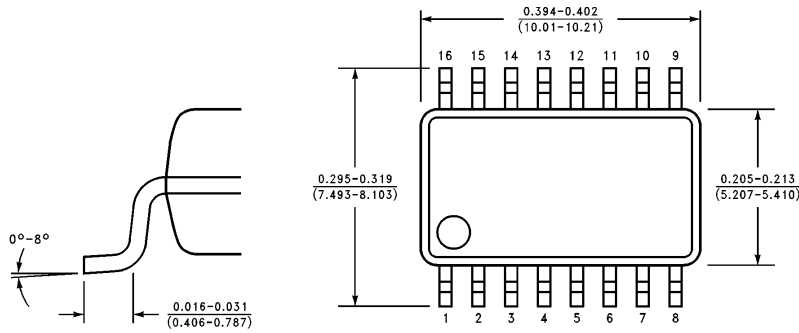
16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

J16A (REV L)

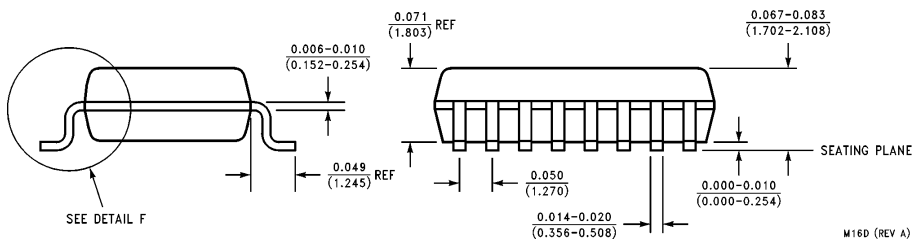
Physical Dimensions inches (millimeters) (Continued)



**16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A**

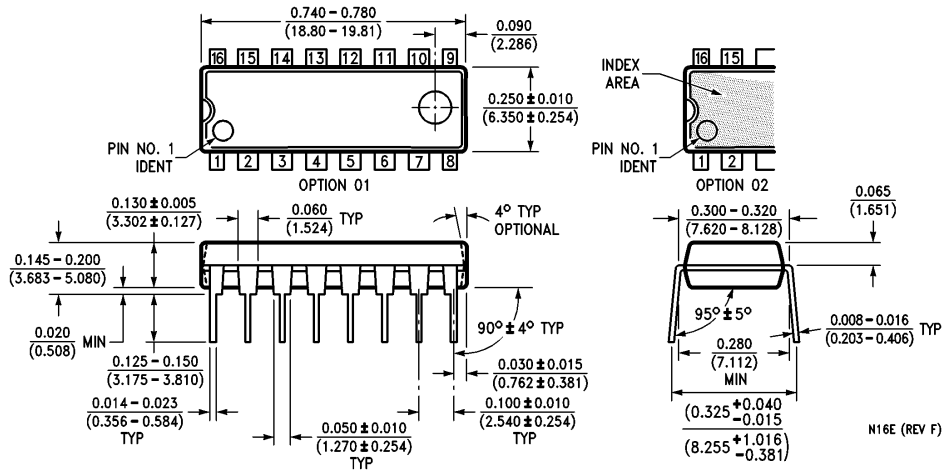


DETAIL F



**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D**

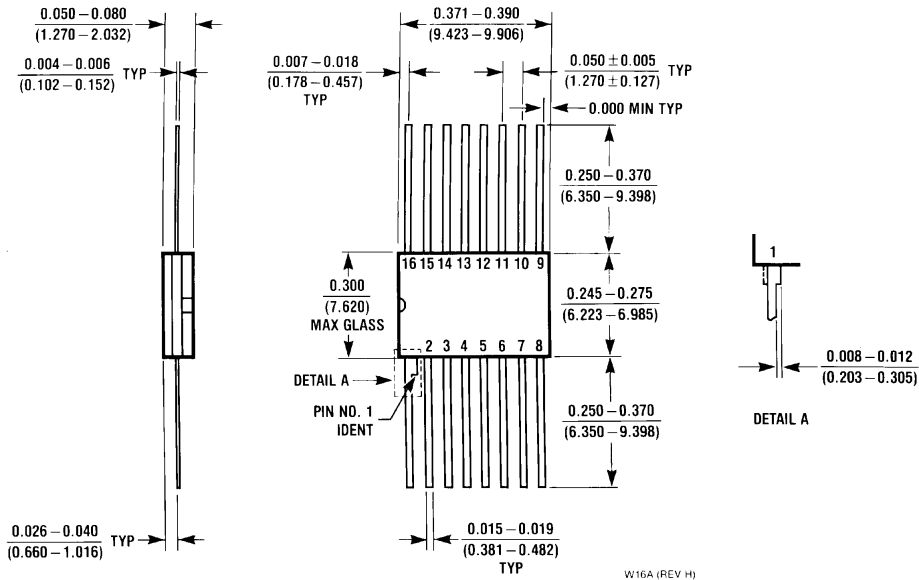
Physical Dimensions inches (millimeters) (Continued)



16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

N16E (REV F)

Physical Dimensions inches (millimeters) (Continued)



**16-Lead Ceramic Flatpak (F)
NS Package Number W16A**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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